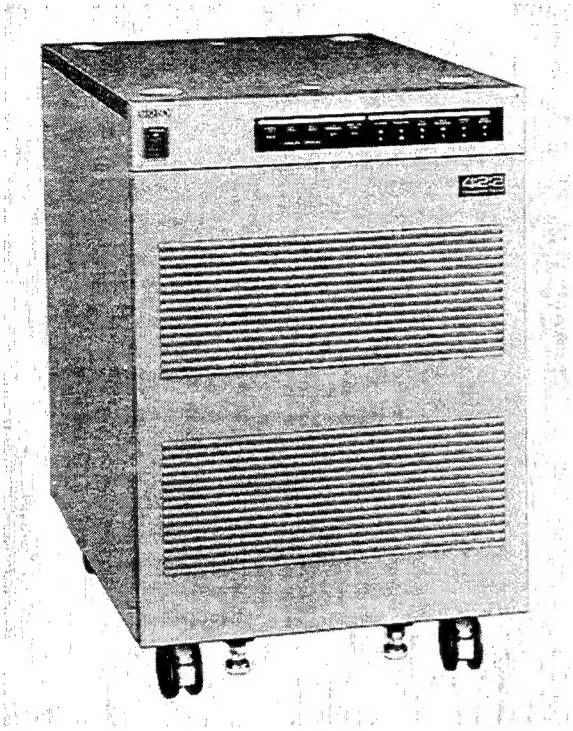
SONY

DIGITAL SIGNAL PROCESSOR

# DVPC-1000



4:2:2

Component Digital

MAINTENANCE MANUAL

Volume 1 1st Edition (Revised 3)

Serial No. 10001 and Higher

# SAFETY CHECK-OUT

After correcting the original service problem, perform the following safety checks before releasing the set to the customer:

Check the metal trim, "metallized" knobs, screws, and all other exposed metal parts for AC leakage. Check leakage as described below.

## LEAKAGE TEST

The AC leakage from any exposed metal part to earth ground and from all exposed metal parts to any exposed metal part having a return to chassis, must not exceed 3.5 mA. Leakage current can be measured by any one of three methods.

1. A commercial leakage tester, such as the Simpson 229 or RCA WT-540A. Follow the manufacturers' instructions to use these instruments.
2. A battery-operated AC milliammeter. The Data Precision 245 digital multimeter is suitable for this job.
3. Measuring the voltage drop across a resistor by means of a VOM or battery-operated AC voltmeter. The "limit" indication is 5.25V, so analog meters must have an accurate low-voltage scale. The Simpson 250 and Sanwa SH-63Trd are examples of a passive VOM that is suitable. Nearly all battery operated digital multimeters that have a 20V AC range are suitable. (See Fig. A)

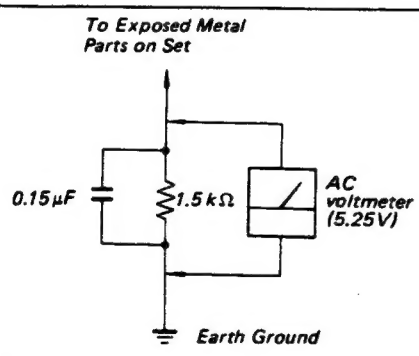



*Fig. A. Using an AC voltmeter to check AC leakage.*

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## A. BLOCK DIAGRAMS

### CARD RACK


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VA-45 Board; Video A/D, D/A Converter . . . . . A-9
PG-13 Board; Pulse Generator . . . . . A-16
IF-139 Board; TTP Interface . . . . . A-15
AU-86 Board; Audio Input . . . . . A-19
AE-06 Board; Audio Outer Encoder . . . . . A-23
VE-12 Board; Video Outer Encoder . . . . . A-27
IE-17 Board; Inner Encoder . . . . . A-31
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FM-09 Board; Frame Memory . . . . . A-51
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SY-70 Board; SYNC/ID Extractor . . . . . A-59
IV-14 Board; Video & Audio I/O . . . . . A-63
IV-20 Board; Video I/O . . . . . A-63(a)
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AT-45 Board; Audio Line Amplifier . . . . . A-66


Volume-2


B. SCHEMATIC DIAGRAMS & BOARD LAYOUT

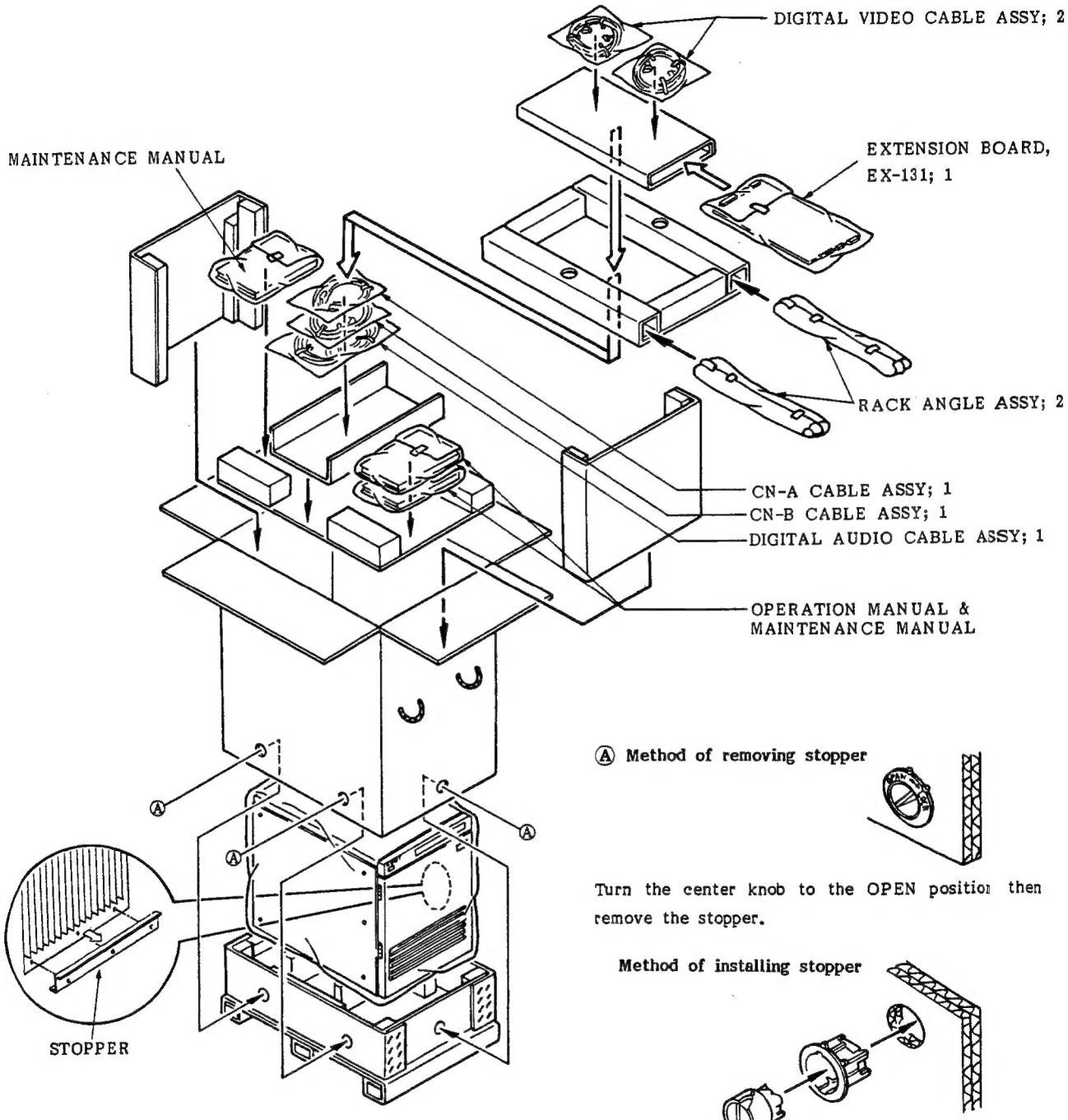
C. SEMICONDUCTOR PIN ASSIGNMENTS

D. REPLACEABLE PARTS & OPTIONAL FIXTURE

E. CHANGED PARTS

# SECTION 1
# INSTALLATION

## 1-1. UNPACKING AND REPACKING



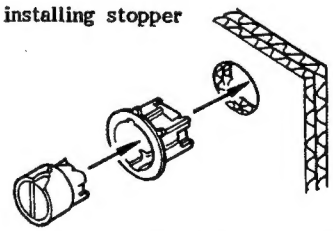

Note: A stopper has been mounted in the card rack at the factory to prevent the plug-in boards from comming off in transit.
Usually, the stopper is not necessary, however, it should be mounted again when transporting to a distant place.

**Ⓐ Method of removing stopper**



Turn the center knob to the OPEN position then remove the stopper.

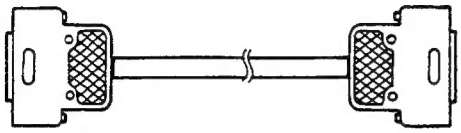
**Method of installing stopper**



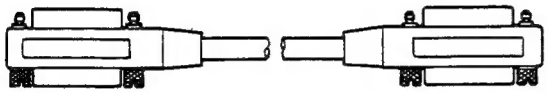
Hold the stopper with the OPEN protrusion facing directly upward, then insert it into the hole in the carton. Next, hold the center knob so that it is facing directly upward, then insert the stopper and turn it to the LOCK position.

## 1-2. ACCESSORIES SUPPLIED

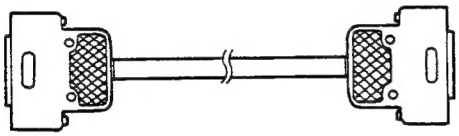
CN-A cable assy: 1
Cable for connecting DVPC-1000 to DVR-1000: 50-core cable, length 1 m



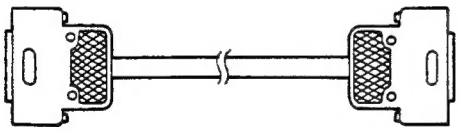
CN-B cable assy: 1
Cable for connecting DVPC-1000 to DVR-1000: 24-core cable, length 1 m



Digital video cable assy: 2
Digital video input/output cable: 25-core cable, length 10 m



Digital audio cable assy: 1
Digital audio input/output cable: 15-core, length 10 m

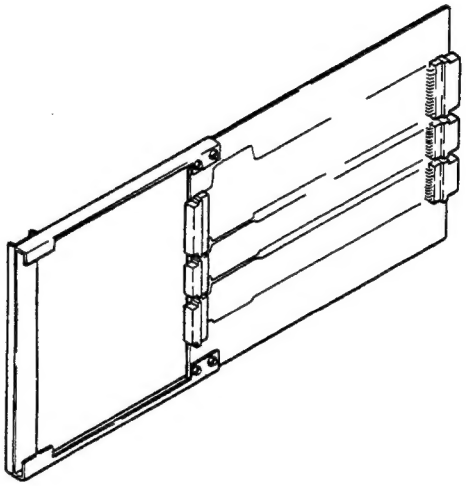


Rack angle assy: 2
Used for rack-mounting the unit.

Operation manual
English version is provided with the USA/Canadian model. English version, French version and German version are provided with the European model.

Maintenance manual
Vol-1 and Vol-2 are provided with the unit.

Extension board: EX-131: 1
Used for checking or repairing the main printed circuit boards contained in the card rack.



## 1-3. POWER REQUIREMENT

### 1-3-1. Capacity of AC Power Source

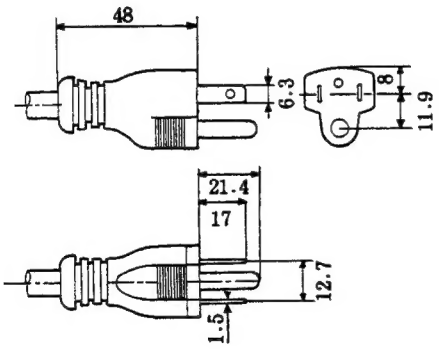
| | |
|---|---|
| Line Voltage | 90 to 132 V or 198 to 264 V |
| Mains supply frequency | 50 Hz or 60 Hz |
| Power consumption | 850 W max |

The supply voltage setting can be changed using the voltage selector switch on the front of the power supply unit. The above power is consumed during normal operation. When the unit is first switched ON, however, a maximum surge current of between 14 and 16 A will flow. The AC supply must therefore be capable of supplying this surge current otherwise the power supply breaker on the AC supply side may trip, or the power supply inside the DVPC-1000 may not operate.

### 1-3-2. Power Cord

Approx. 3 m in length (For J,UC)
Approx. 2.5 m in length (For EK)

For UC




For EK

**Note:** Obtain an AC plug and install it on the end of the cable.

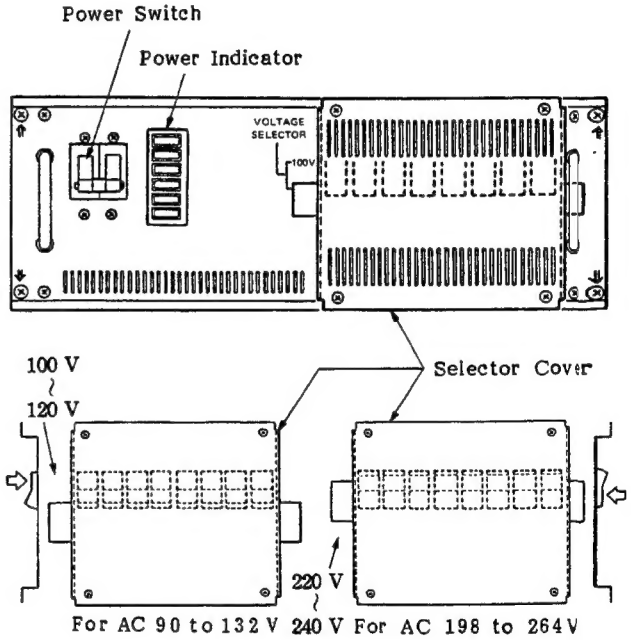
UNIT: mm

### 1-3-3. Setting of Voltage Selector

The voltage selector should be set as follows in accordance with the line input voltage.
90 to 132 V .... Set to "100-120 V".
198 to 264 V ... Set to "220-240 V".

If the voltage selector must be reset, remove the selector cover on the front panel, and eight rocker switches will appear. Reset all rocker switches, turn the selector cover upside down and reseat it.

<FRONT VIEW>



### 1-3-4. Ventilation and Heat Sink

The two fans which are located at the rear panel of the power unit and the three fans which are located at the connector panel are used for air-cooling. Therefore, if either the intake or exhaust at the top, bottom, left or right side should clog or the fans should stop, the power unit may be damaged. If the protective covers on the power unit are opened for maintenance or other activities, be sure not to operate the power unit for a long time without cooling.
If the temperature sensor in the power supply section of the unit operates, the buzzer in the power supply unit will sound and also the LED (ALARM) on the front panel of the power supply unit will flash.

### 1-3-5. DC Output Indication

The DC output indication LEDs (Green) on the front panel of the power unit are lit when all DC voltages, i.e., +5 V, -5 V, +18 V, -18 V and Fan are output normally.

## 1-4. INSTALLATION CONDITIONS

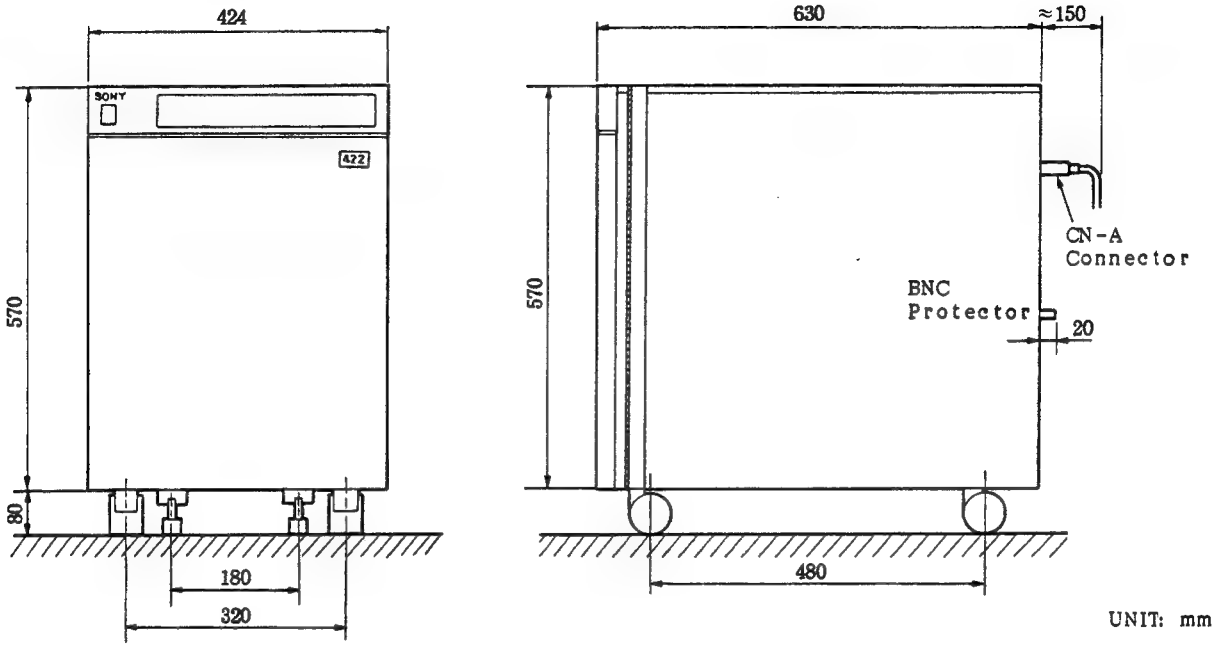
| | |
|---|---|
| Operating temperature | +5 C to +40 C |
| Storage temperature | -20 C to +60 C |
| Humidity | 20% to 80% (noncondensing) |

Install the DVPC-1000 on a firm, level surface, and set the adjusters on the underside of the unit.
The total weight when the DVR-1000 is installed on the DVPC-1000 is about 150 Kg.

Do not install the unit in the following locations:
- Exposed to direct sunlight or powerful lighting
- In a dusty location
- In a location which is subjected to vibration
- In a powerful electric or magnetic field
- In a location which is generated to electric noise
- In a location which is generated to static electricity noise

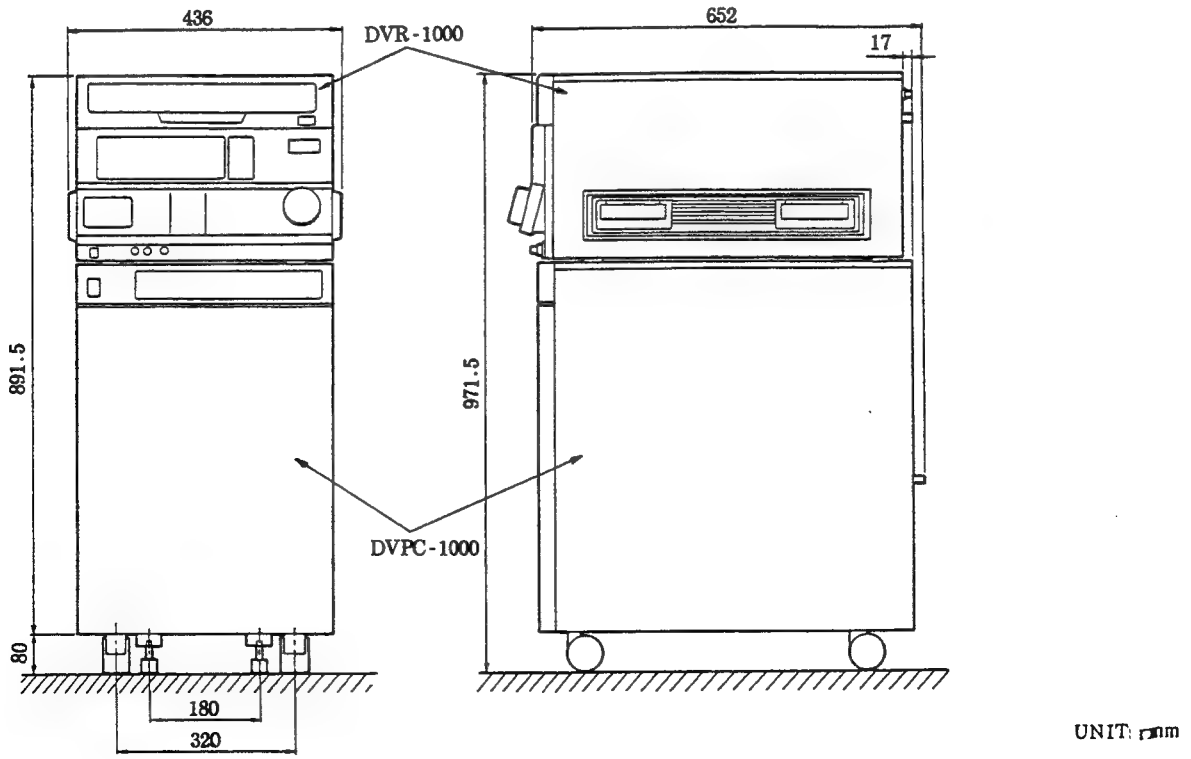
## 1-5. INSTALLATION SPACE

(1) External Dimensions




UNIT: mm

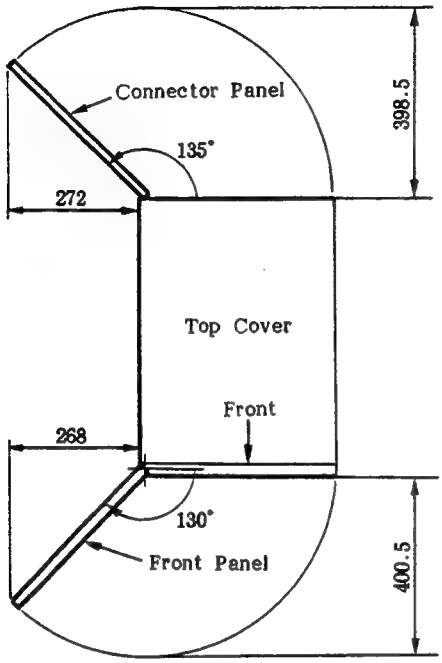
(2) External Dimensions: When installing DVR-1000 on the DVPC-1000




UNIT: mm

(3) Working Space: When opening Front Panel and Connector Panel

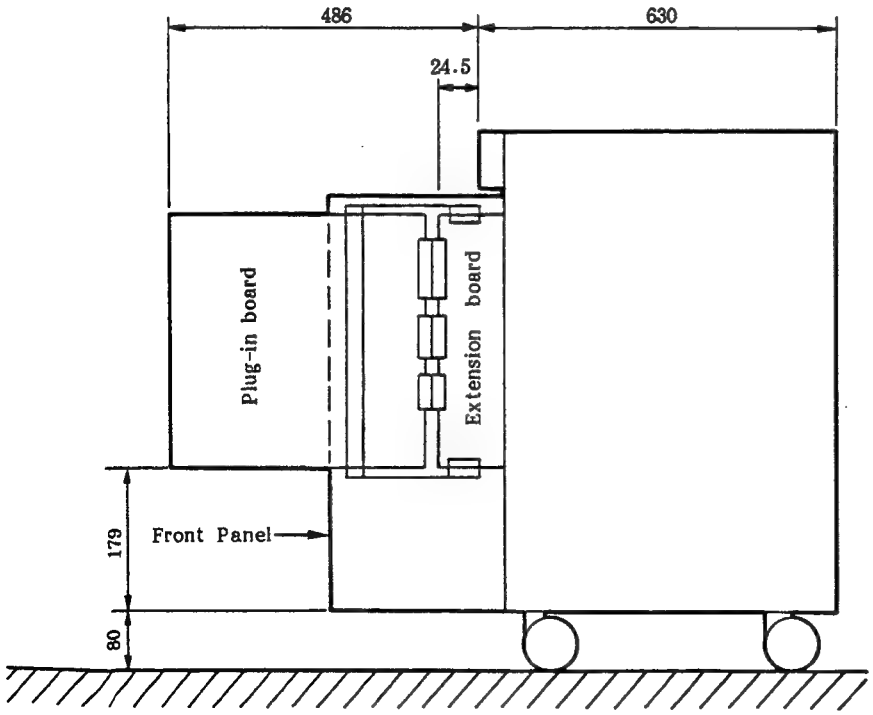
<TOP VIEW>




UNIT: mm

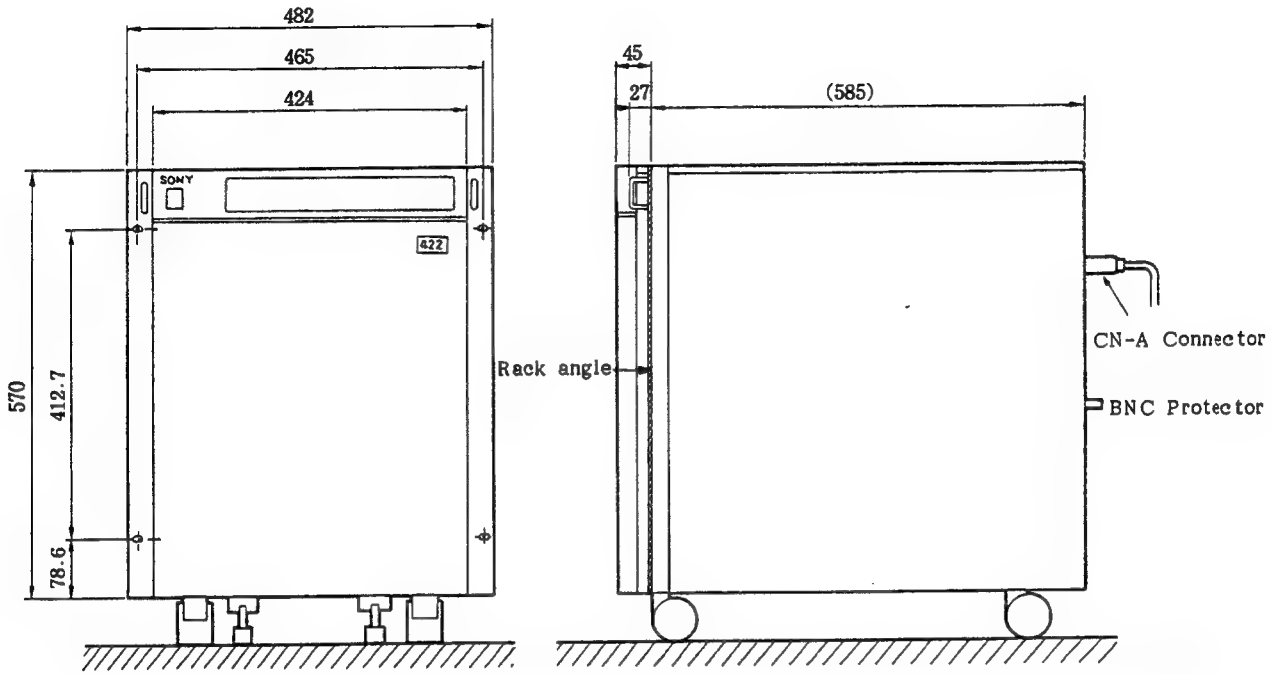
(4) Working Space: When using Extension board

<SIDE VIEW>




UNIT: mm

(5) Working Space: When rack-mounting

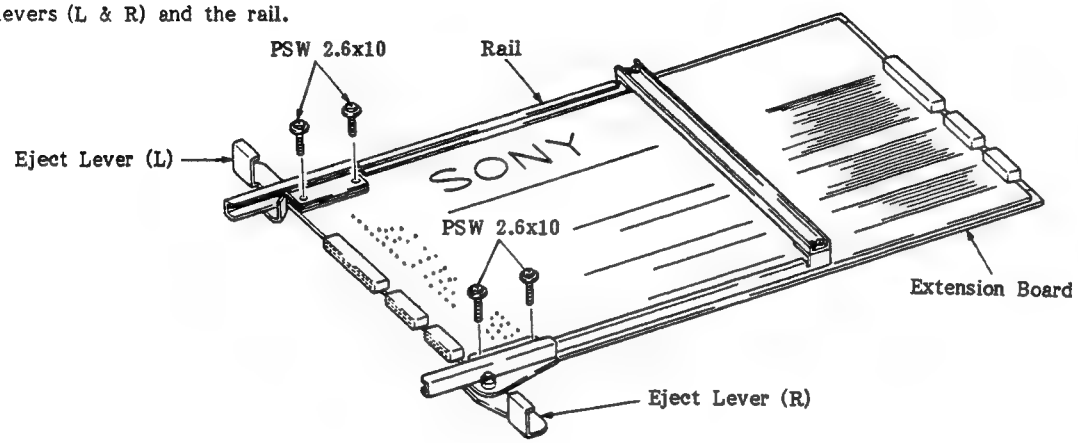



UNIT: mm

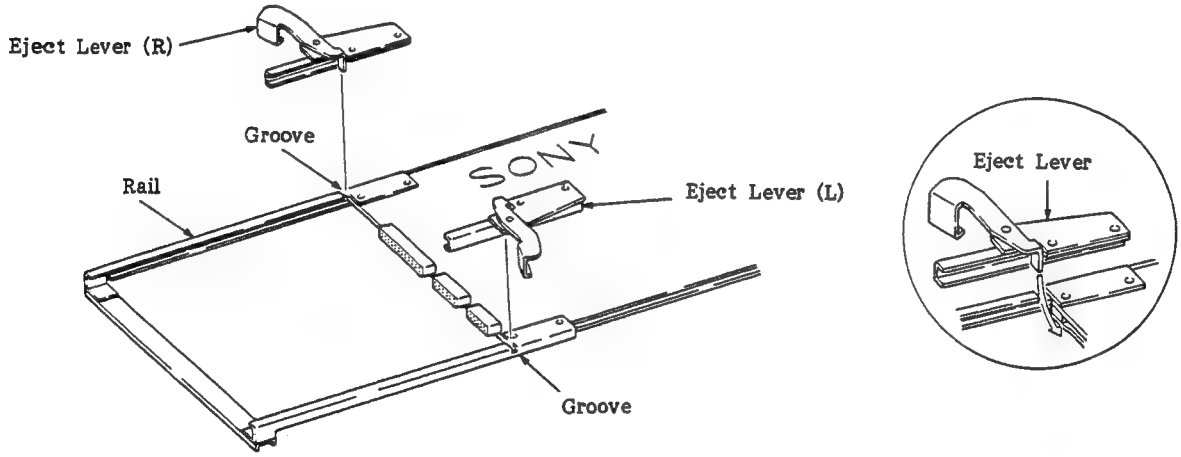
## 1-6. METHOD OF ASSEMBLING EXTENSION BOARD

Before installing extension board EX-131, it is necessary to remove the EXT bracket as shown in the figure below.

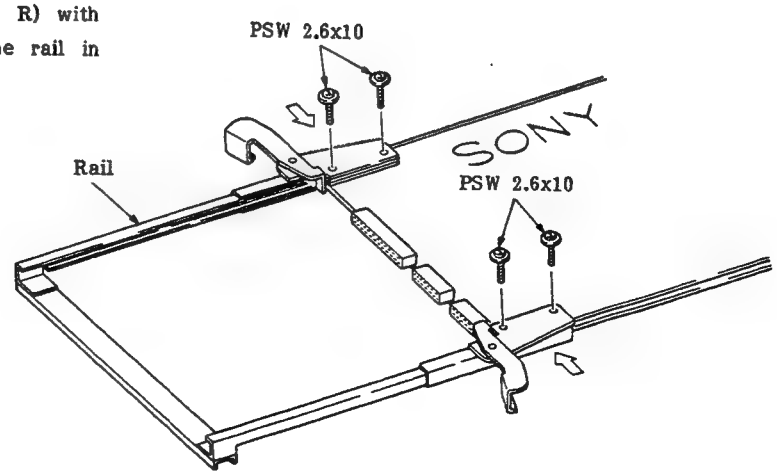
1. Remove the four screws which secure the eject levers (L & R) and the rail.




2. Place the ral on the extension board as shown in the figure.
3. Place the eject levers (L & R) so that the each tip of the levers are inserted in the grooves of the rail.

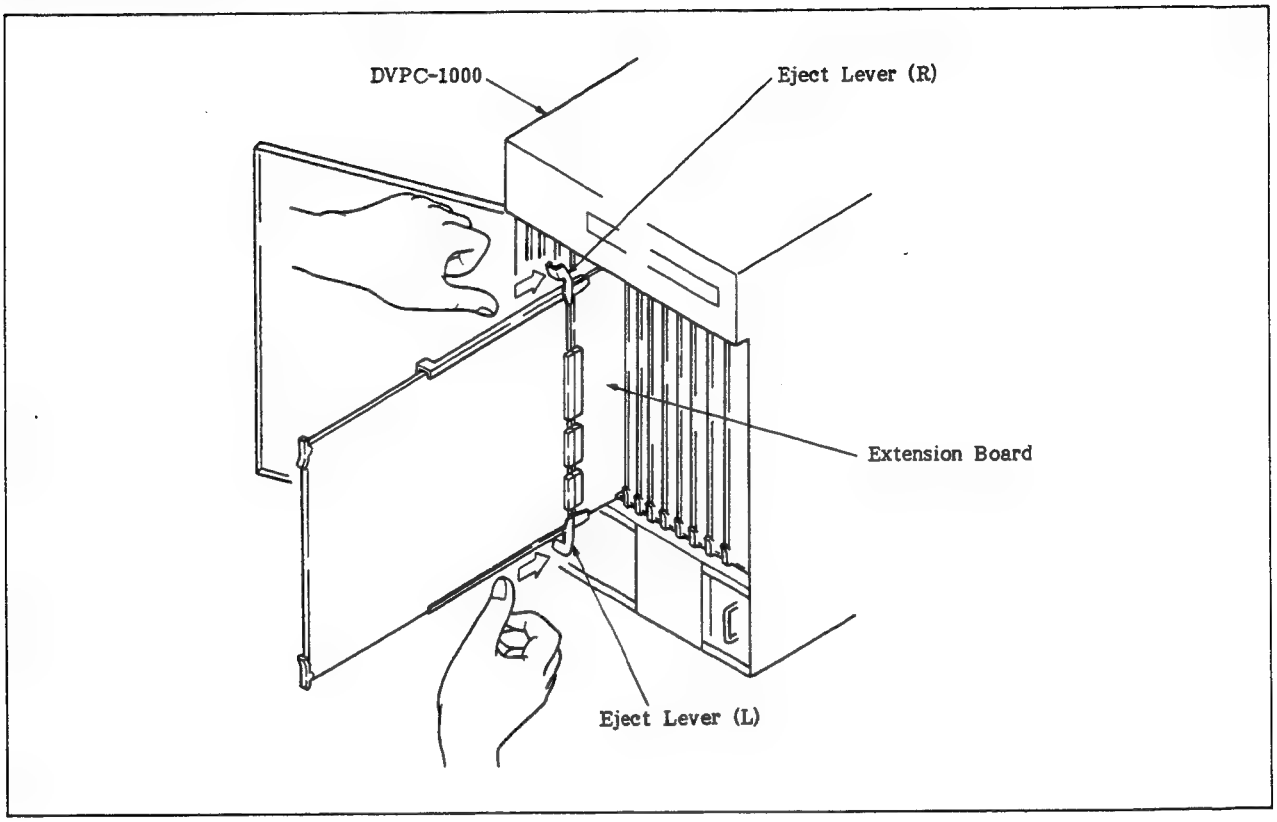



4. Secure the rail and the eject levers (L & R) with four screws (PSW 2.6x10), while pushing the rail in the direction of the arrows in the figure.



**PRECAUTIONS**

Press both the right and left eject levers evenly to remove the board that is set on the extension board.



## 1-7. RACK-MOUNTING

Prepare the following parts for rack-mounting.

Support Angle: 1 pair

Be sure to use the parts recommended by the rack maker.

Rack Mount Bracket: 1 pair

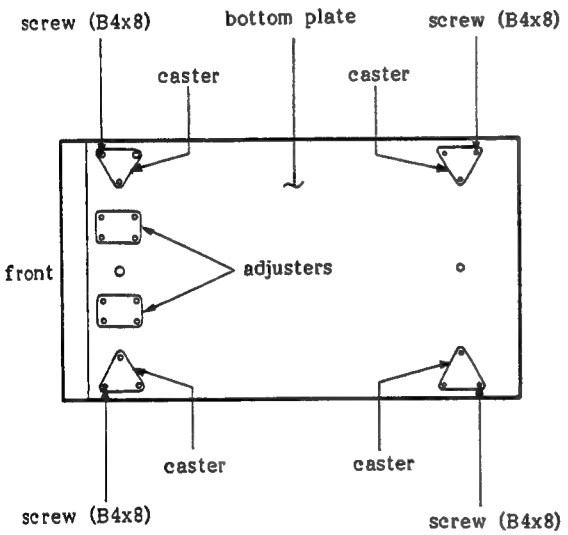
DVPC-1000 is equipped with 1 pair.

Screws and Nuts

To install the rack mount bracket, remove the screws from the DVPC-1000 and reuse them.

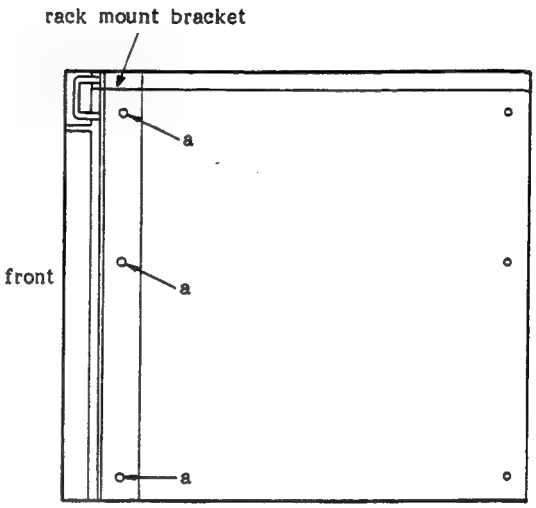
To install the other mounting parts, use the screws and nuts recommended by the rack maker.

1. Remove the four casters and two adjusters, as shown in the figure. Fix the bottom plate using the screws that were removed.




2. Remove the screws "a" clamping the outer panels (three screws each, denoted by "a" in figure), and install the rack mounting bracket (accessory).

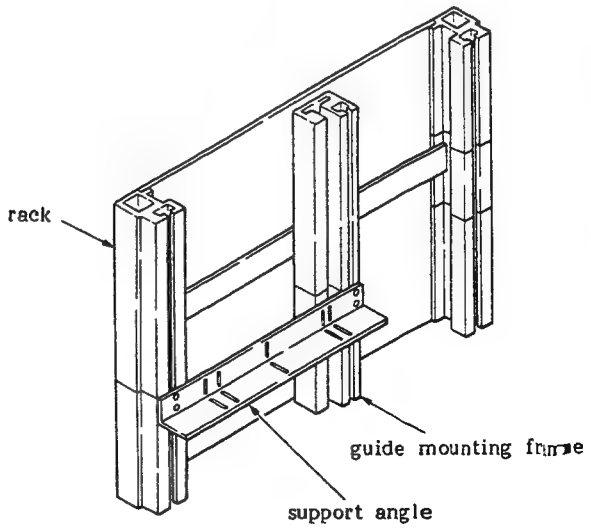
<SIDE VIEW>



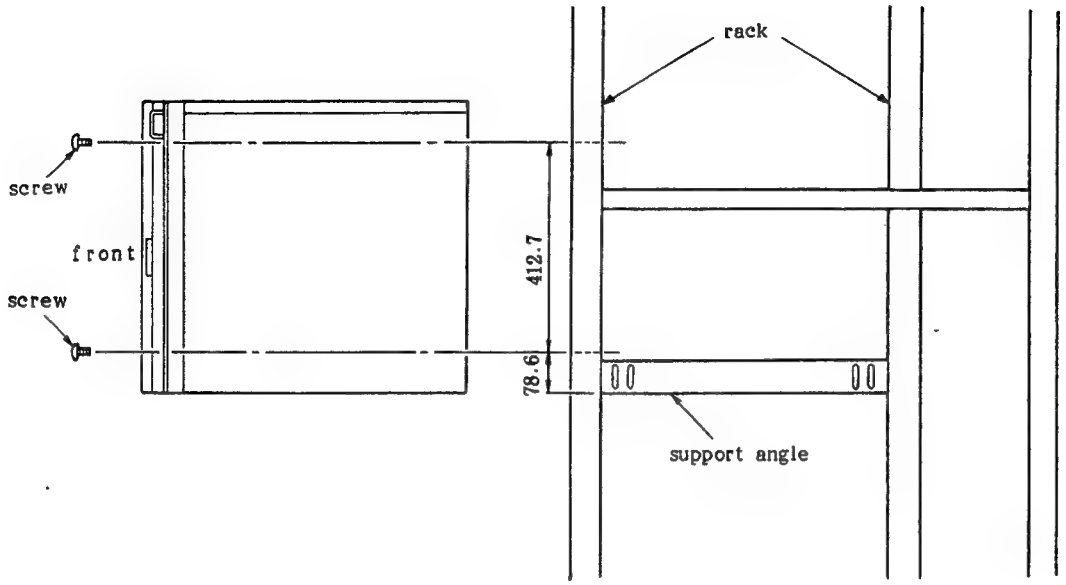

3. Install the support angle.

**Note:** Use the support angle, screws and nuts recommended by the rack maker. Depending on the rack used, a dedicated bracket and guide mounting frame may also be required. For details, consult with the rack maker. Also, the support angle used must be capable of adequately supporting the DVPC-1000.

The installation example shown in the figure below is for reference only. Depending upon the particular rack, the actual mounting may sometimes differ from the example.



4. Mount the DVPC-1000 on the rack.



## 1-8. INPUT/OUTPUT INTERFACE

### 1-8-1. Matching Connectors and Cables

| DVPC-1000 Connectors | | Matching Connector/Cables | |
|---|---|---|---|
| Used for | Type | Type | Sony Part No. |
| REFERENCE DIGITAL VIDEO IN | Dsub,25P,Female | DIGITAL VIDEO CABLE ASSY | 1-559-043-11(Note 1) |
| ANALOG VIDEO | BNC | BNC | |
| CF PULSE | BNC | BNC | |
| VIDEO DIGITAL INPUT | Dsub,25P,Female | DIGITAL VIDEO CABLE ASSY | 1-559-043-11(Note 1) |
| DIGITAL OUTPUT | Dsub,25P,Female | DIGITAL VIDEO CABLE ASSY | 1-559-043-11(Note 1) |
| AUDIO DIGITAL INPUT-2 | Dsub,15P,Female | DIGITAL AUDIO CABLE ASSY | 1-559-044-11(Note 2) |
| DIGITAL OUTPUT-2 | Dsub,15P,Female | DIGITAL AUDIO CABLE ASSY | 1-559-044-11(Note 2) |
| ADVANCE AUDIO OUT | Dsub,15P,Female | DIGITAL AUDIO CABLE ASSY | 1-559-044-11(Note 2) |
| VIDEO ANALOG INPUT-1(R/R-Y, G/Y,B/B-Y,SYNC) | BNC | BNC | |
| ANALOG OUTPUT-1(R/R-Y, G/Y,B/B-Y,SYNC) | BNC | BNC | |
| MONITOR OUT (R,G,B, SYNC) | BNC | BNC | |
| WFM(INPUT,OUTPUT, SYNCOUT) | BNC | BNC | |
| ANALOG INPUT-2 | Connector,12P Male | Connector,12P,Female | 1-562-159-00 |
| ANALOG OUTPUT-2 | Connector,12P Female | Connector,12P,Male | 1-560-995-00 |
| AUDIO DIGITAL INPUT-1 (CH-1/2,CH-3/4) | XLR,3P,Female | ECD-3C,-10C,-30C | Optional Accessory (Note 8) |
| DIGITAL OUTPUT-1 (CH-1/2,CH-3/4) | XLR,3P,Male | | |
| ANALOG INPUT (CH-1/2/3/4) | XLR,3P,Female | XLR,3P,Male | 1-508-084-00(Note 3) |
| ANALOG OUTPUT (CH-1/2/3/4) | XLR,3P,Male | XLR,3P,Female | 1-508-083-00(Note 4) |
| SPARE 1 | BNC | BNC | |
| 2 | BNC | BNC | |
| 3 | BNC | BNC | |
| TO VTR CN-A | Dsub,50P,Female | CN-A CABLE ASSY | 1-559-042-12(Note 5) |
| CN-B | GPIB(IEEE-488) | CN-B CABLE ASSY | 1-556-535-31(Note 6) |
| GPIB | GPIB(IEEE-488) | | (Note 7) |

(Note 1) Digital Video Input/Output cable. The length of the cable in 10 m.
Two cables are supplied to DVPC-1000.

(Note 2) Digital Audio Input/Output cable. The length of the cable in 10 m.
One cable is supplied to DVPC-1000.

(Note 3) Equivalent to CANNON XLR-3-12C.

(Note 4) Equivalent to CANNON XLR-3-11C.

(Note 5) Connected to the TTP part (DVR-1000). The length of the cable in 1 m.
One cable is supplied to DVPC-1000.

(Note 6) Connected to the TTP part (DVR-1000). The length of the cable in 1 m.
One cable is supplied to DVPC-1000. No other type of GPIB controller can be connected to this connector.

(Note 7) This connector is used to control the unit from an external equipment through the GPIB bus, but it is not used at present.

(Note 8) The lengths of the cable are 3 m, 10 m, and 30 m.

1-8-2. Input/Output Signal of the Connectors

① REFERENCE

| | |
|---|---|
| ANALOG VIDEO INPUT | Composite Sync; 75 ohms, 0.28 to 4.0 Vp-p<br>or Black Burst; 75 ohms |
| CF PULSE IN/OUT | TTL level, 50% Duty, 14.985 Hz (525)/6.25 Hz (625) |

② VIDEO

| | |
|---|---|
| ANALOG INPUT-1 | Y; 1.0 Vp-p, 75 ohms, Sync negative<br>R, G, B,/R-Y, B-Y; 0.7 Vp-p, 75 ohms<br>SYNC; Composite Sync; 75 ohms, 0.28 to 4.0 Vp-p<br>or Black Burst; 75 ohms |
| ANALOG OUTPUT-1 | Y; 1.0 Vp-p, 75 ohms, Sync negative<br>R, G, B,/R-Y, B-Y; 0.7 Vp-p, 75 ohms<br>SYNC; Composite Sync 75 ohms, 4.0 Vp-p |
| MONITOR OUT | R, G, B; 0.7 Vp-p, 75 ohms<br>SYNC; Composite Sync 75 ohms, 4.0 Vp-p (525)/2.0 Vp-p (625) |
| WFM | INPUT; CTL 0.2 to 1.0 Vp-p<br>RF ENVELOPE 0.2 to 1.0 Vp-p, 75 ohms<br>Either one of the values is selected by the DVR-1000 and inputted into the DVPC-1000.<br>OUTPUT; R/G/B 0.7 Vp-p, 75 ohms<br>WFM INPUT (CTL 0.2 to 1.0 Vp-p, 75 ohms / RF ENVELOPE 0.2 to 1.0 Vp-p, 75 ohms)<br>Either one of the values is selected in the DVR-1000 and DVPC-1000 outputted.<br>SYNC OUT; Composite Sync 75 ohms, 4.0 Vp-p |
| ANALOG INPUT-2 | Y; 1.0 Vp-p, 75 ohms, Sync negative<br>R-Y, B-Y; 0.7 Vp-p, 75 ohms |
| ANALOG OUTPUT-2 | Y; 1.0 Vp-p, 75 ohms, Sync negative<br>R-Y, B-Y; 0.7 Vp-p, 75 ohms |

③ AUDIO

DIGITAL INPUT-1 (CH-1/2, CH-3/4);
RS422 (Conforming to the AES/EBU format)

DIGITAL OUTPUT-1 (CH-1/2, CH-3/4);
RS422 (Conforming to the AES/EBU format)

ANALOG INPUT (CH-1/2/3/4);
+28 dBm to -10 dBm, reference level +4 dBm (J)/+8 dBm (UC, EK), HEAD ROOM 20 dB, 150 ohms/600 ohms/10k ohms switching possible, balanced

ANALOG OUTPUT (CH-1/2/3/4);
+14 dBm (J)/+8 dBm (UC, EK) reference, balanced, 37.5 ohms/150 ohms/600 ohms switching possible

### ④ REFERENCE DIGITAL VIDEO INPUT CONNECTOR

SMPTE Standard: Conforming to RP-125
EBU standard: Conforming to Tech 3246-E

| Pin No. | Signal | Spec | Description |
|---|---|---|---|
| 1 | REF VCK(+) | ECL | 27 MHz Clock; Differential Input |
| 14 | REF VCK(-) | ECL | |
| 2 | GND | | |
| 15 | GND | | |
| 3 | REF V7(+) | ECL | Digital Video Data; Differential Input |
| 16 | REF V7(-) | ECL | |
| 4 | REF V6(+) | ECL | |
| 17 | REF V6(-) | ECL | |
| 5 | REF V5(+) | ECL | |
| 18 | REF V5(-) | ECL | |
| 6 | REF V4(+) | ECL | |
| 19 | REF V4(-) | ECL | |
| 7 | REF V3(+) | ECL | |
| 20 | REF V3(-) | ECL | |
| 8 | REF V2(+) | ECL | |
| 21 | REF V2(-) | ECL | |
| 9 | REF V1(+) | ECL | |
| 22 | REF V1(-) | ECL | |
| 10 | REF V0(+) | ECL | |
| 23 | REF V0(-) | ECL | |
| 13 | Frame Ground | | |
| 11 | | | |
| 24 | | | |
| 12 | | | |
| 25 | | | |

### ⑤ VIDEO DIGITAL INPUT CONNECTOR

SMPTE Standard: Conforming to RP-125
EBU standard: Conforming to Tech 3246-E

| Pin No. | Signal | Spec | Description |
|---|---|---|---|
| 1 | EDI CK(+) | ECL | 27 MHz Clock; Differential Input |
| 14 | EDI CK(-) | ECL | |
| 2 | GND | | |
| 15 | GND | | |
| 3 | EDI 7(+) | ECL | Digital Video Data; Differential Input |
| 16 | EDI 7(-) | ECL | |
| 4 | EDI 6(+) | ECL | |
| 17 | EDI 6(-) | ECL | |
| 5 | EDI 5(+) | ECL | |
| 18 | EDI 5(-) | ECL | |
| 6 | EDI 4(+) | ECL | |
| 19 | EDI 4(-) | ECL | |
| 7 | EDI 3(+) | ECL | |
| 20 | EDI 3(-) | ECL | |
| 8 | EDI 2(+) | ECL | |
| 21 | EDI 2(-) | ECL | |
| 9 | EDI 1(+) | ECL | |
| 22 | EDI 1(-) | ECL | |
| 10 | EDI 0(+) | ECL | |
| 23 | EDI 0(-) | ECL | |
| 13 | Frame Ground | | |
| 24 | | | |
| 12 | | | |
| 25 | | | |
| 11 | | | |

### ⑥ VIDEO DIGITAL OUTPUT CONNECTOR

SMPTE Standard: Conforming to RP-125
EBU standard: Conforming to Tech 3246-E

| Pin No. | Signal | Spec | Description |
|---|---|---|---|
| 1 | EDO CK(+) | ECL | 27 MHz Clock; Differential Output |
| 14 | EDO CK(-) | ECL | |
| 2 | GND | | |
| 15 | GND | | |
| 3 | EDO 7(+) | ECL | Digital Video Data; Differential Output |
| 16 | EDO 7(-) | ECL | |
| 4 | EDO 6(+) | ECL | |
| 17 | EDO 6(-) | ECL | |
| 5 | EDO 5(+) | ECL | |
| 18 | EDO 5(-) | ECL | |
| 6 | EDO 4(+) | ECL | |
| 19 | EDO 4(-) | ECL | |
| 7 | EDO 3(+) | ECL | |
| 20 | EDO 3(-) | ECL | |
| 8 | EDO 2(+) | ECL | |
| 21 | EDO 2(-) | ECL | |
| 9 | EDO 1(+) | ECL | |
| 22 | EDO 1(-) | ECL | |
| 10 | EDO 0(+) | ECL | |
| 23 | EDO 0(-) | ECL | |
| 13 | Frame Ground | | |
| 24 | | | |
| 12 | | | |
| 25 | | | |
| 11 | | | |

### ⑦ AUDIO DIGITAL INPUT-2 CONNECTOR

Conforming to the AES/EBU format

| Pin No. | Signal | Spec | Description |
|---|---|---|---|
| 1 | Frame Ground | | |
| 2 | AD IN 1(+) | RS422 | Digital Audio CH-1 Input Data; Differential Input |
| 3 | AD IN 1(-) | RS422 | |
| 4 | GND | | |
| 5 | | | |
| 6 | AD IN 2(+) | RS422 | Digital Audio CH-2 Input Data; Differential Input |
| 7 | AD IN 2(-) | RS422 | |
| 8 | GND | | |
| 9 | AD IN 3(+) | RS422 | Digital Audio CH-3 Input Data; Differential Input |
| 10 | AD IN 3(-) | RS422 | |
| 11 | GND | | |
| 12 | | | |
| 13 | AD IN 4(+) | RS422 | Digital Audio CH-4 Input Data; Differential Input |
| 14 | AD IN 4(-) | RS422 | |
| 15 | GND | | |

## ⑧ AUDIO DIGITAL OUTPUT-2 CONNECTOR

Conforming to the AES/EBU format

| Pin No. | Signal | Spec | Description |
|---|---|---|---|
| 1 | Frame Ground | | |
| 2 | AD 0 1(+) | RS422 | Digital Audio CH-1 Output Data; |
| 3 | AD 0 1(-) | RS422 | Differential Output |
| 4 | GND | | |
| 5 | | | |
| 6 | AD 0 2(+) | RS422 | Digital Audio CH-2 Output Data; |
| 7 | AD 0 2(-) | RS422 | Differential Output |
| 8 | GND | | |
| 9 | AD 0 3(+) | RS422 | Digital Audio CH-3 Output Data; |
| 10 | AD 0 3(-) | RS422 | Differential Output |
| 11 | GND | | |
| 12 | | | |
| 13 | AD 0 4(+) | RS422 | Digital Audio CH-4 Output Data; |
| 14 | AD 0 4(-) | RS422 | Differential Output |
| 15 | GND | | |

## ⑨ AUDIO ADVANCE AUDIO OUTPUT CONNECTOR

Conforming to the AES/EBU format

| Pin No. | Signal | Spec | Description |
|---|---|---|---|
| 1 | Frame Ground | | |
| 2 | A ADV 1(+) | RS422 | Digital Audio CH-1 Output Data; |
| 3 | A ADV 1(-) | RS422 | Differential Output |
| 4 | GND | | |
| 5 | | | |
| 6 | A ADV 2(+) | RS422 | Digital Audio CH-2 Output Data; |
| 7 | A ADV 2(-) | RS422 | Differential Output |
| 8 | GND | | |
| 9 | A ADV 3(+) | RS422 | Digital Audio CH-3 Output Data; |
| 10 | A ADV 3(-) | RS422 | Differential Output |
| 11 | GND | | |
| 12 | | | |
| 13 | A ADV 4(+) | RS422 | Digital Audio CH-4 Output Data; |
| 14 | A ADV 4(-) | RS422 | Differential Output |
| 15 | GND | | |

⑩ CN-A CONNECTOR

| Pin No. | Signal | Spec | Description |
|---|---|---|---|
| 1 | PB A (X) | ECL | A-ch PB RF Signal |
| 18 | PB A (G) | | |
| 34 | PB A (Y) | ECL | |
| 2 | PB B (X) | ECL | B-ch PB RF Signal |
| 19 | PB B (G) | | |
| 35 | PB B (Y) | ECL | |
| 3 | PB C (X) | ECL | C-ch PB RF Signal |
| 20 | PB C (G) | | |
| 36 | PB C (Y) | ECL | |
| 4 | PB D (X) | ECL | D-ch PB RF Signal |
| 21 | PB D (G) | | |
| 37 | PB D (Y) | ECL | |
| 23 | REC A (Y) | ECL | A-ch REC RF Signal |
| 39 | REC A (X) | ECL | |
| 24 | REC B (Y) | ECL | B-ch REC RF Signal |
| 40 | REC B (X) | ECL | |
| 25 | REC C (Y) | ECL | C-ch REC RF Signal |
| 41 | REC C (X) | ECL | |
| 26 | REC D (Y) | ECL | D-ch REC RF Signal |
| 42 | REC D (X) | ECL | |
| 27 | REC CK (Y) | ECL | REC Clock |
| 43 | REC CK (X) | ECL | |
| 5 | FRP (+) | TTL | Reference Frame Pulse; Differential Output |
| 6 | FRP (-) | TTL | |
| 7 | AFP (+) | TTL | Reference Audio Frame Pulse; Differential Output |
| 8 | AFP (-) | TTL | |
| 9 | CFP (+) | TTL | Reference CF Pulse; Differential Output |
| 10 | CFP (-) | TTL | |
| 11 | DRP (+) | TTL | Reference Drum PG Pulse; Differential Output (Unused) |
| 12 | DRP (-) | TTL | |
| 13 | LSTD (+) | TTL("H"=525, "L"=625) | 525/625 Select Signal; Differential Output |
| 14 | LSTD (-) | TTL | |
| 28 | AFT (-) | TTL | PB Audio Frame Pulse; Differential Input |
| 44 | AFT (+) | TTL | |
| 29 | CFT (-) | TTL | PB CF Pulse; Differential Input |
| 45 | CFT (+) | TTL | |
| 15 | AMIX (X) | | Digital MIX Audio Signal |
| 31 | AMIX (G) | -20dBs | |
| 48 | AMIX (Y) | | |
| 16 | AMONI L (X) | | Digital Audio Monitor Signal (L) (The output Signal is selected by the function control panel.) |
| 32 | AMONI L (G) | -20dBs | |
| 49 | AMONI L (Y) | | |
| 17 | AMONI R (X) | | Digital Audio Monitor Signal (R) (The output Signal is selected by the function control panel.) |
| 33 | AMONI R (G) | -20dBs | |
| 50 | AMONI R (Y) | | |
| 22 | SPARE A (-) | | |
| 38 | SPARE A (+) | | |
| 30 | SPARE B (-) | | |
| 46 | SPARE B (+) | | |
| 47 | CASSIS GND | Frame GND | |

⑪ CN-B CONNECTOR

| Pin No. | Signal | Spec | Description |
|---|---|---|---|
| 1 | IFDI01 | TTL | 8 Bit Parallel Data Bus |
| 2 | IFDI02 | TTL | |
| 3 | IFDI03 | TTL | |
| 4 | IFDI04 | TTL | |
| 13 | IFDI05 | TTL | |
| 14 | IFDI06 | TTL | |
| 15 | IFDI07 | TTL | |
| 16 | IFDI08 | TTL | |
| 6 | IFDAV | TTL | Handshake Bus |
| 7 | IFNRFD | TTL | |
| 8 | IFNDAC | TTL | |
| 9 | IFIFC | TTL | Management Bus |
| 10 | IFSRQ | TTL | |
| 11 | IFATN | TTL | |
| 17 | IFREN | TTL | |
| 5 | IFEOI | TTL | |
| 12 | SHIELD | Frame GND | |
| 18 | IFDAV (G) | TTL | |
| 19 | IFNRFD (G) | GND | |
| 20 | IFNDAC (G) | GND | |
| 21 | IFIFC (G) | GND | |
| 22 | IFSRQ (G) | GND | |
| 23 | IFATN (G) | GND | |
| 24 | LOGIC GND | GND | |

⑫ GPIB CONNECTOR

| Pin No. | Signal | Spec | Description |
|---|---|---|---|
| 1 | IFDI01 | TTL | 8 Bit Parallel Data Bus |
| 2 | IFDI02 | TTL | |
| 3 | IFDI03 | TTL | |
| 4 | IFDI04 | TTL | |
| 13 | IFDI05 | TTL | |
| 14 | IFDI06 | TTL | |
| 15 | IFDI07 | TTL | |
| 16 | IFDI08 | TTL | |
| 6 | IFDAV | TTL | Handshake Bus |
| 7 | IFNRFD | TTL | |
| 8 | IFNDAC | TTL | |
| 9 | IFIFC | TTL | Management Bus |
| 10 | IFSRQ | TTL | |
| 11 | IFATN | TTL | |
| 17 | IFREN | TTL | |
| 5 | IFEOI | TTL | |
| 12 | SHIELD | Frame GND | |
| 18 | IFDAV (G) | TTL | |
| 19 | IFNRFD (G) | GND | |
| 20 | IFNDAC (G) | GND | |
| 21 | IFIFC (G) | GND | |
| 22 | IFSRQ (G) | GND | |
| 23 | IFATN (G) | GND | |
| 24 | LOGIC GND | GND | |

## 1-9. INITIAL SETTING OF SWITCHES AND JUMPERS

This sections describes the settings of the switches and jumpers required by the system configuration. For details on the functions of other switches and jumpers, refer to the section 2-5 "FUNCTION OF SWITCHES AND JUMPERS".

### 1-9-1. Video/Audio Input/Output Signal Selection

The video/audio input and output signals are selected by the switches inside the DVPC-1000 or by the control panel menu.

They are selected by the control panel menu when PR CONT (processor control mode) on the system setup sub menu is ON.

When PR CONT is OFF, they are selected by the following switches.

| | SELECTOR SWITCH |
|---|---|
| VIDEO INPUT<br>DIGITL/ANALOG<br>RGB/Y, R-Y, B-Y<br><br>BNC/MALTI | <br>VID IN SEL SW (S2/VE-12)<br>VID SEL RGB/Y, R-Y, B-Y SW (S4/PG-13)<br>VID SEL BNC/MULTI SW (S5/PG-13) |
| VIDEO OUTPUT<br>RGB/Y, R-Y, B-Y | <br>VID SEL RGB/Y, R-Y, B-Y SW (S3-5/PG-13) |
| AUDIO INPUT<br>DIGITAL/ANALOG<br><br>XLR/D-SUB | <br>AUD IN SEL DIG/ANA SW (S3/AU-86)<br>AUD IN SEL XLR/D-SUB SW (S2/AU-86) |
| REFERENCE INPUT | REF INPUT SEL DIG/ANA SW (S7/TG-28) |

**Note:** When PR CONT is ON, the "OFF" lamp of the PROC SW ENABLE indicator on the DVPC-1000 front panel lights; when PR CONT is OFF, the "ON" lamp lights.

### 1-9-2. Changing the Audio Input Impedances

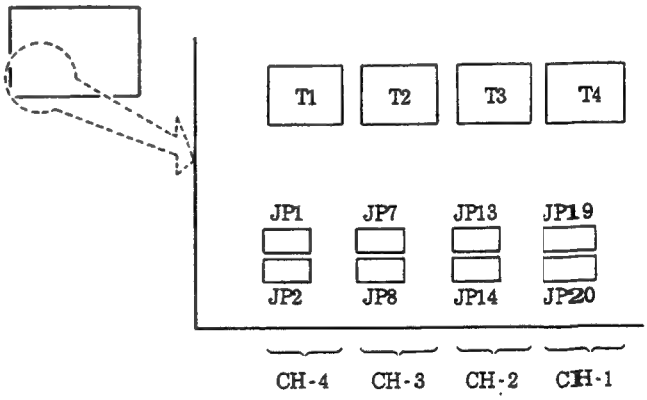
**IV-14 Board**

**JP1/2: Analog audio input impedance CH-4**
**JP7/8: Analog audio input impedance CH-3**
**JP13/14: Analog audio input impedance CH-2**
**JP19/20: Analog audio input impedance CH-1**

These jumpers select the analog audio input impedances. The line input impedances of analog audio channels 1, 2, 3 and 4 are set to 600 ohms when the unit is shipped. However they can be changed to 150 ohms or 10k ohms using the jumper plugs on the IV-14 board and the switches at the side of the ANALOG AUDIO INPUT connectors.

| INPUT IMPEDANCE | JUMPER PLUG | | | | REAR PANEL SWITCH |
|---|---|---|---|---|---|
| | CH-1 | CH-2 | CH-3 | CH-4 | EACH CHANNEL |
| | JP19/20 | JP13/14 | JP7/8 | JP1/2 | 600Ω/10kΩ |
| 10 kΩ | JP19 | JP13 | JP7 | JP1 | 10 kΩ |
| 600Ω | JP19 | JP13 | JP7 | JP1 | 600Ω |
| 150Ω | JP20 | JP14 | JP8 | JP2 | 600Ω |

IV-14 BOARD
—Component Side—



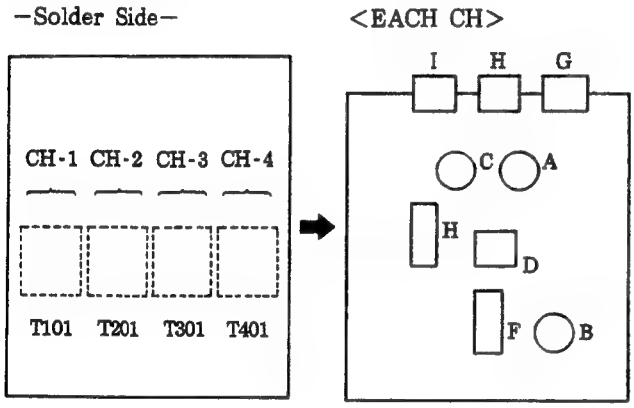
### 1-9-3. Changing the Audio Output Impedances

**AT-45 Board**

**A, B, C, D, E, F, G, H, I (soldered jumpers):**
**Analog audio output impedances**

These jumpers select the analog audio output impedances. The line output impedances of analog audio channels 1, 2, 3 and 4 are set to 600 ohms when the unit is shipped but they can be changed through the remodeling shown below to 37.5 ohms and 150 ohms.

AT-45 BOARD
—Solder Side—




| OUTPUT IMPEDANCE | TRACE (each channel) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | E | F | G | H | I |
| 600Ω | ⊐⊏ | ⊐⊏ | ⊐⊏ | □□ | □□ | □□ | □□ | □□ | □□ |
| 150Ω | ⊐✕ | ⊐⊏ | ⊐⊏ | ⊟⊟ | ⊟⊟ | □□ | □□ | □□ | □□ |
| 37.5Ω | ⊐✕ | ⊐✕ | ⊐✕ | ⊟⊟ | ⊟⊟ | ⊟⊟ | ⊟⊟ | ⊟⊟ | ⊟⊟ |

⊐⊏ ; Keep unchanged as shorted.
□□ ; Keep unchanged as open.
⊟⊟ ; Short (solder).
⊐✕ ; Open (cut trace).

### 1-9-4. Changing the Audio Input Levels

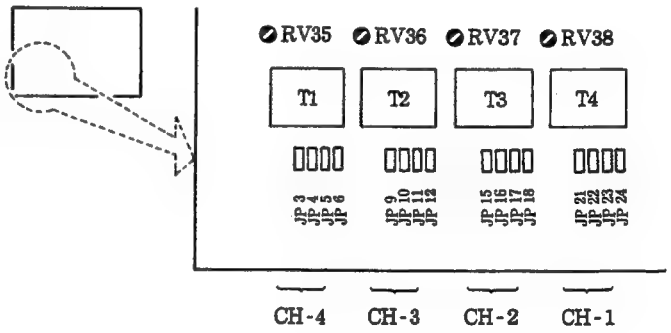
**IV-14 Board**

**JP3/4/5/6:** **Analog audio input level CH-4**
**JP9/10/11/12:** **Analog audio input level CH-3**
**JP15/16/17/18:** **Analog audio input level CH-2**
**JP21/22/23/24:** **Analog audio input level CH-1**

These jumpers select the analog audio input levels. The reference input levels of analog audio channels 1, 2, 3 and 4 are set to +4dBm (J)/+8dBm (UC, EK) when the unit is shipped. However they can be changed to between -6dBm and -20dBm using the variable resistors (RV35, RV36, RV37 and RV38) and jumper plugs on the IV-14 board.

| REFERENCE INPUT LEVEL | JUMPER PLUG | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | CH-1 | | CH-2 | | CH-3 | | CH-4 | |
| | JP23 24 | JP21 22 | JP17 18 | JP15 16 | JP11 12 | JP9 10 | JP5 6 | JP3 4 |
| +8 dBm to −6 dBm | JP23 | JP22 | JP17 | JP16 | JP11 | JP10 | JP5 | JP4 |
| −6 dBm to −20 dBm | JP24 | JP21 | JP18 | JP15 | JP12 | JP9 | JP6 | JP3 |

IV-14 BOARD
—Component Side—



### 1-9-5. Changing the Audio Output Levels

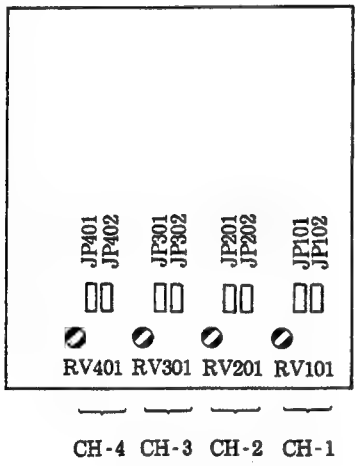
**AT-45 Board**

**JP101/102: Analog audio output level CH-1**
**JP201/202: Analog audio output level CH-2**
**JP301/302: Analog audio output level CH-3**
**JP401/402: Analog audio output level CH-4**

These jumpers select the analog audio output levels.
The reference output levels of the analog audio channels are set to +4dBm (J)/+8dBm (UC, EK) when the unit is shipped. However they can be changed to between -6dBm and -20dBm using the variable resistors (RV101, RV201, RV301 and RV401) and jumper plugs on the AT-45 board.

| REFERENCE OUTPUT LEVEL | JUMPER PLUG | | | |
|---|---|---|---|---|
| | CH-1 | CH-2 | CH-3 | CH-4 |
| | JP101/102 | JP201/202 | JP301/JP302 | JP401/402 |
| +8 dBm to −6 dBm | JP102 | JP202 | JP302 | JP402 |
| −6 dBm to −20 dBm | JP101 | JP201 | J301 | JP401 |

AT-45 BOARD
—Component Side—




### 1-9-6. 525/625 Line Standard Setting

SYSTEM SELECT switch S2/IF-139 is selected in accordance with the scanning line standard used by the configured system. The setting of this switch appears on the front panel.

**525:** When the 525/60 system is used.
**625:** When the 625/50 system is used.

### 1-9-7. Other

Check that the TEST SW S3/IF-139 is OFF before proceeding with the operation. When S3/IF-139 is OFF, the green lamp of the TEST MODE indicator on the DVPC-1000 front panel lights up.
For details on other switch and jumper settings, refer to the operation manual and maintenance manual and then the appropriate settings should be made as required.

## 1-10. INSTALLING DVR-1000 AND DVPC-1000 2 METERS OR MORE APART

Although DVR-1000 and DVPC-1000 are usually connected with a 1-meter CN-A cable, if they have to be installed at a distance of more than one meter apart, make the following modifications ① and ②. The distance between the two must be within 4 meters.

CN-A CABLE ASSY, 2m : 1-559-042-21
CN-A CABLE ASSY, 4m : 1-559-042-31

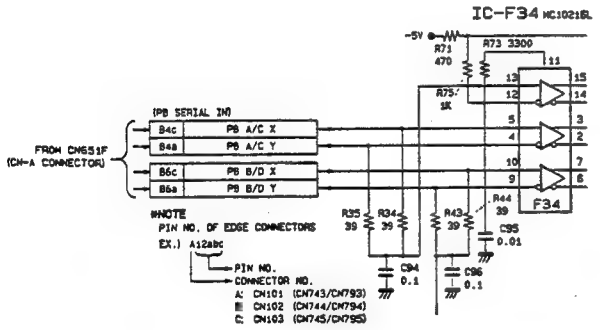
### ①Modification of the SY-70A and B boards

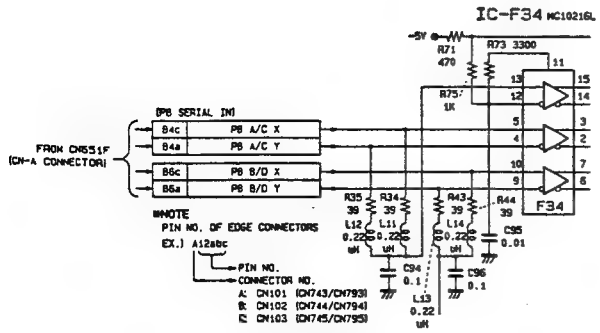
Object: DVPC-1000 (J) #10001-#10699
DVPC-1000 (UC) #10001-#10699
DVPC-1000 (EK) #10001-#10699

Step 1. Prepare two sets of the following parts.

| Ref.No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| L11 | 1-410-312-11 | S | INDUCTOR, 0.22 µH 20% |
| L12 | 1-410-312-11 | S | INDUCTOR, 0.22 µH 20% |
| L13 | 1-410-312-11 | S | INDUCTOR, 0.22 µH 20% |
| L14 | 1-410-312-11 | S | INDUCTOR, 0.22 µH 20% |

Step 2. Modify the SY-70A and B boards as follows.



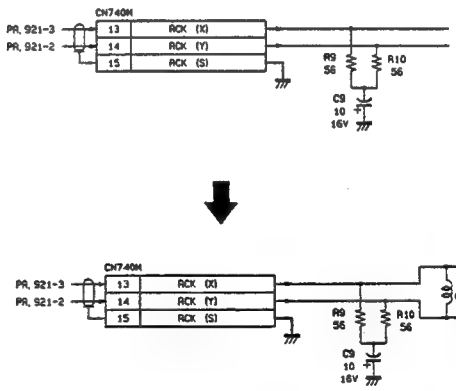

### ②Modification of the RF-15 board

Object: DVR-1000 (J) #10001-#10499
DVR-1000 (UC) #10001-#10499
DVR-1000 (EK) #10001-#10499

Step 1. Prepare the following parts.

| REf.No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| L3 | 1-410-312-11 | S | INDUCTOR, 0.22 µH 20% |
| L4 | 1-410-312-11 | S | INDUCTOR, 0.22 µH 20% |

Step 2. Modify the RF-15 board as follows.




Step 3. Adjust the RF signal system after modifications have been made.

# SECTION 2
# SERVICE INFORMATION

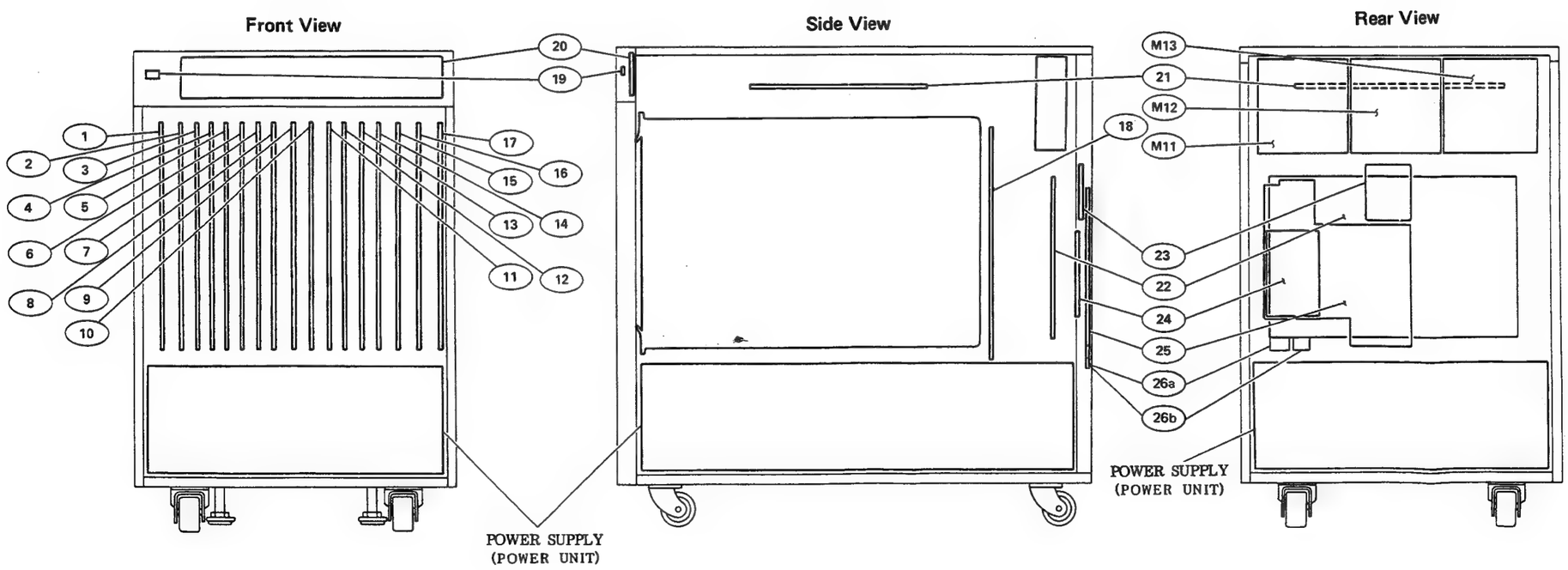
## 2-1. PRINCIPAL COMPONENT LOCATION

CARD RACK

| | | |
|---|---|---|
| 1 | AA-29 BORAD: | Audio A/D,D/A Converter |
| 2 | VA-45 BOARD: | Video A/D,D/A Converter |
| 3 | PG-13 BOARD: | Pulse Generator |
| 4 | IF-139 BOARD: | TTP Interface |
| 5 | AU-86 BOARD: | Audio Input |
| 6 | AE-06 BOARD: | Audio Outer Encoder |
| 7 | VE-12 BOARD: | Video Outer Encoder |
| 8 | IE-17 BOARD: | Inner Encoder |
| 9 | TG-28 BOARD: | Timing Generator |
| 10 | AN-01 BOARD: | Audio Concealment |
| 11 | AP-14 BOARD: | Audio Output Controll |
| 12 | VN-01 BOARD: | Video Concealment |
| 13 | FM-09 BOARD(A): | Frame Memory (C & D channels) |
| 14 | FM-09 BOARD(B): | Frame Memory (A & B channels) |
| 15 | CI-01 BOARD: | Inner Decoder |
| 16 | SY-70 BOARD(A): | SYNC/ID Extractor (C & D channels) |
| 17 | SY-70 BOARD(B): | SYNC/ID Extractor (A & B channels) |
| 18 | MB-132 BOARD: | Mother Board |

OTHERS (EXCEPT POWER SUPPLY)

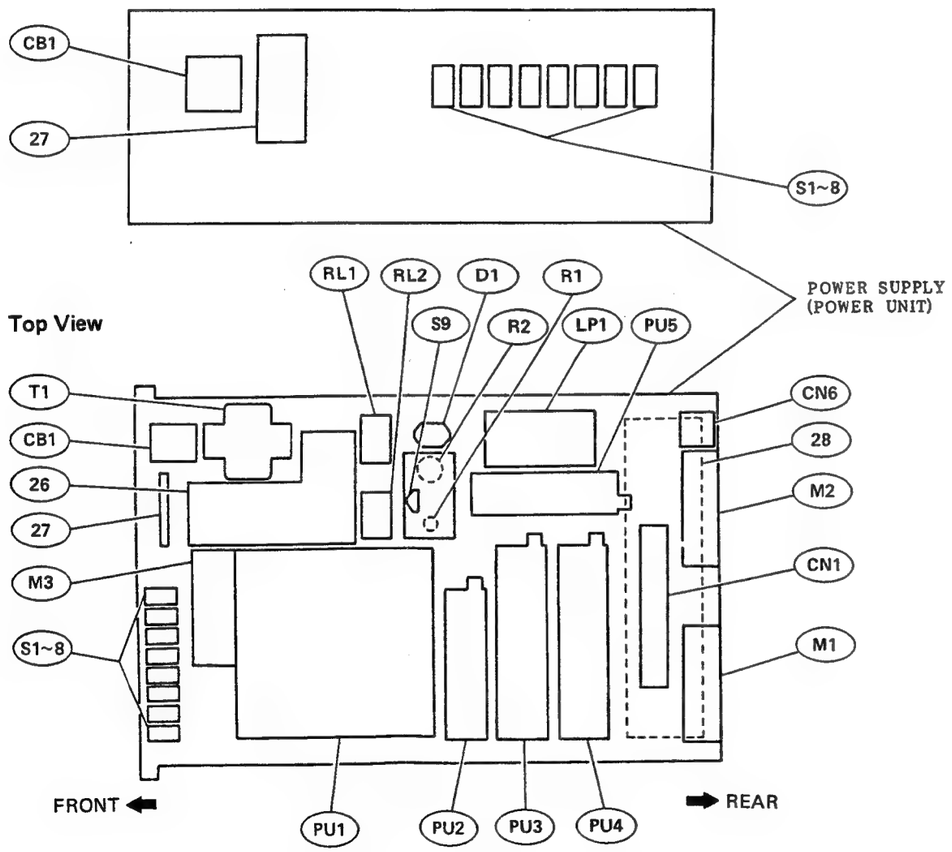
| | | |
|---|---|---|
| 19 | PE-18 BOARD: | Power Indicator |
| 20 | DP-60 BOARD: | Front Panel LED |
| 21 | AT-45 BOARD: | Audio Line Amplifier |
| 22 | IV-14 BOARD: | Video & Audio I/O |
| 23 | DS-18 BOARD: | D-SUB Board |
| 24 | CN-159 BOARD: | 75 ON/OFF Switch Board |
| 25 | CN-190 BOARD: | Terminater Board |
| 26a | CN-227 BOARD: | Multi Connector Board, Video Analog Input2 |
| 26b | CN-227 BOARD: | Multi Connector Board, Video Analog Output2 |
| M11 | MOTOR,FAN | |
| M12 | MOTOR,FAN | |
| M13 | MOTOR,FAN | |



POWER SUPPLY

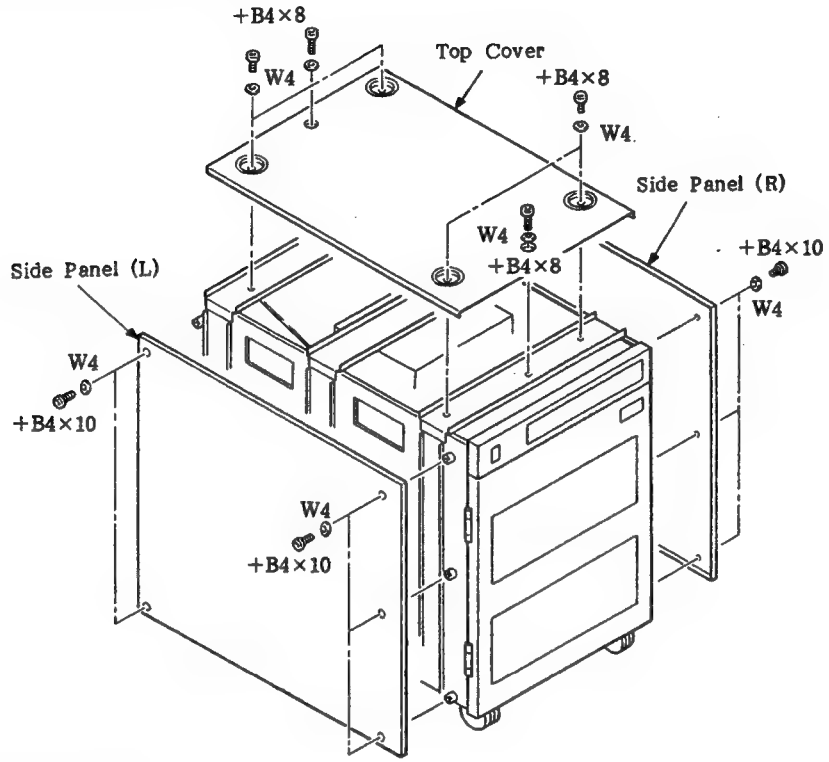
| | | |
|---|---|---|
| 26 | AC-69 BOARD: | Rush Current Protector |
| 27 | LE-51 BOARD: | LED Board |
| 28 | TX-12 BOARD: | Power Supply Relaying |
| CB1 | CIRCUIT BREAKER,250V 20A | |
| CN1 | TERMINAL BOARD,12P | |
| CN6 | TERMINAL BOARD,2P | |
| D1 | TRIAC FSM30C4 | |
| LP1 | LINE FILTER,LF-255PLP5 | |
| M1 | MOTOR,FAN | |
| M2 | MOTOR,FAN | |
| M3 | MOTOR,FAN | |
| PU1 | REGULATOR,SWITCHING +5V/1KW | |
| PU2 | REGULATOR,SWITCHING -5V/60W | |
| PU3 | REGULATOR,SWITCHING -18V/100W | |
| PU4 | REGULATOR,SWITCHING +18V/100W | |
| PU5 | REGULATOR,SWITCHING +12V/60W | |
| R1 | RESISTOR,WIREWOUND 10 15W | |
| R2 | RESISTOR,WIREWOUND 30 60W | |
| RL1 | RELAY,DC12V JH2a | |
| RL2 | RELAY,DC12V JH1a | |
| S1-8 | SWITCH (VOLTAGE SELECTOR) | |
| S9 | SWITCH,THERMAL,70-DEG | |
| T1 | TRANSFORMER,POWER | |

**Front View**



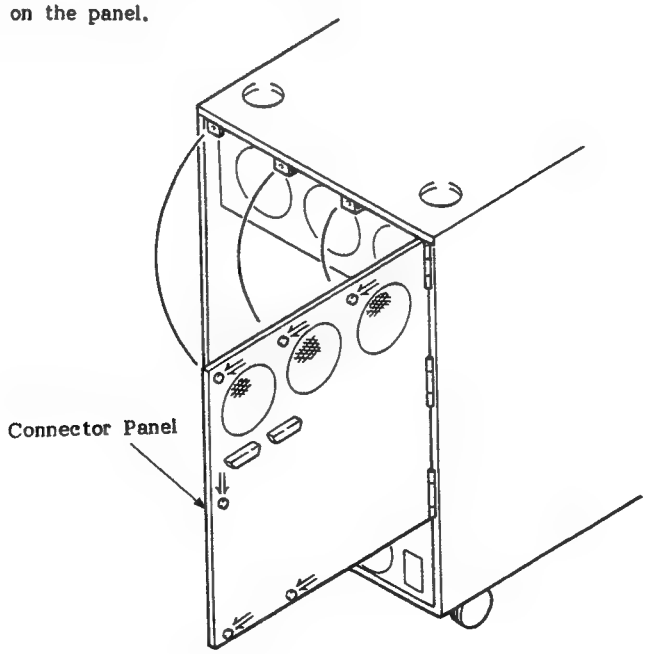
## 2-2. CABINET REMOVAL

### SIDE PANELS AND TOP COVER REMOVAL



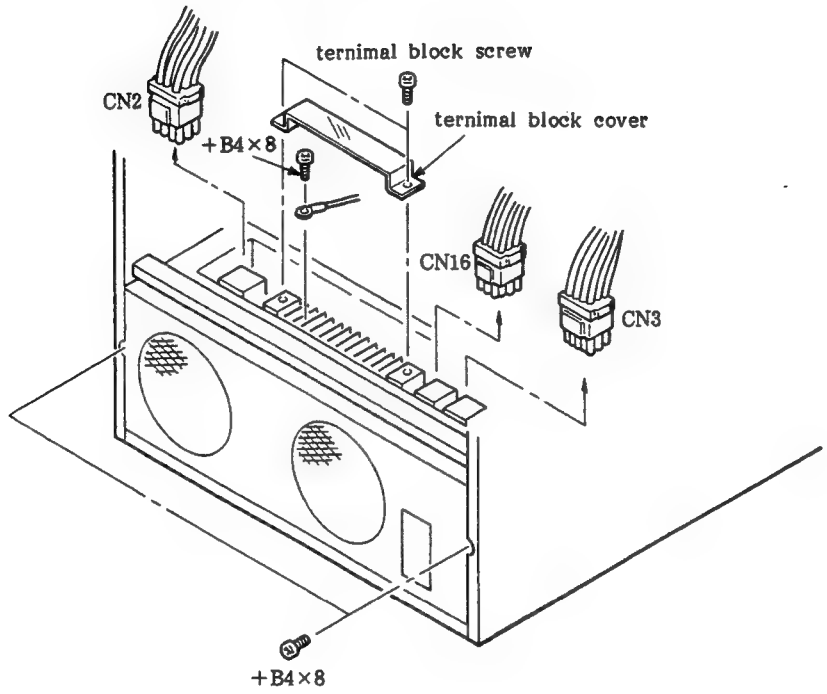

### OPENING OF CONNECTOR PANEL

Open connector panel after sufficiently loosening the screws marked with ⇒ on the panel.

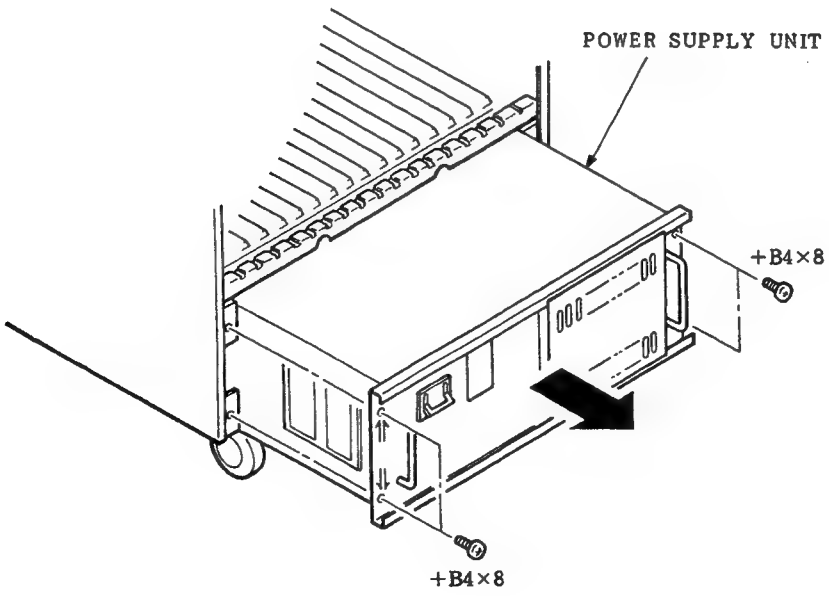


**Removing the power supply unit**

1. Remove the terminal block cover and also CN2, CN16, and CN3.
2. Disconnect the wiring from the terminal block.
3. Unscrew the two screws (at rear) fixing the power supply unit.




4. Unscrew the four screws (indicated by ⇑⇓ ) on the front of the power supply unit, then grasp the handles and remove the power supply unit in the direction of the arrow.

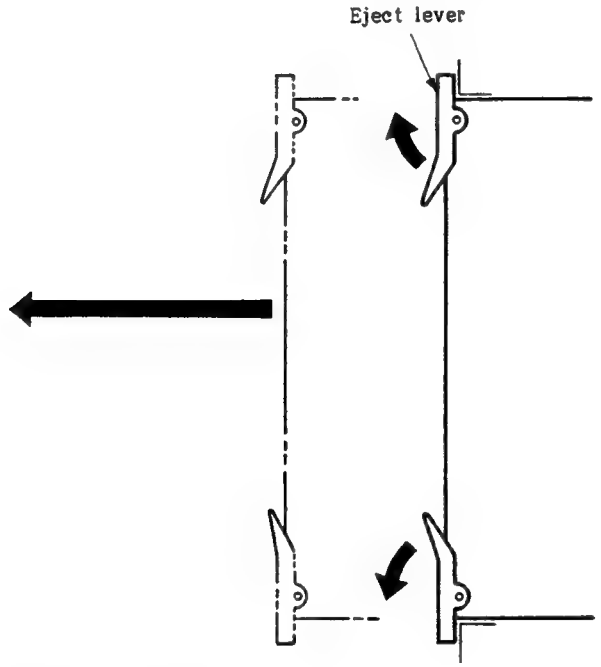


## 2-3. EXTRACTING & INSERTING PLUG-IN BOARDS

Before removing or inserting the plug-in board, turn the power switch OFF.

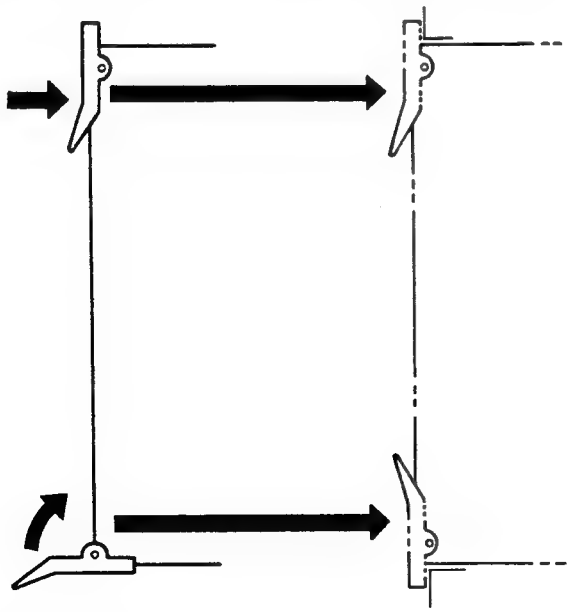
**Removing the Board**

Before removing the plug-in board from the connector, first push up the eject levers on the board. Do not try to pull the board by grasping any of the components on it.




**Inserting the Board**

Set the eject lever in the position shown, then insert the board.



## 2-4. NOTES ON REPAIR PARTS

### 2-4-1. Notes on Repair Parts

**(1) Safety Related Components Warning**

Components identified by shading marked with ⚠ on the schematic diagrams, exploded views and electrical spare parts list are critical to safe operation. Replace these components with Sony parts whose part numbers appear in this manual or in service bulletins and service manual supplements published by Sony.

**(2) Standardization of Parts**

Repair parts supplied from Sony Parts Center may not be always identical with the parts which actually in use due to "accommodating the improved parts and/or engineering changes" or "standardization of genuine parts".

This manual's exploded views and electrical spare parts list are indicating the part numbers of "the standardized genuine parts at present".

**(3) Change of Parts**

Regarding engineering parts changes, refer to Section E. "CHANGED PARTS".

**(4) Stock of Parts**

Parts marked with "o" SP (Supply Code) column of the spare parts list are not normally required for routine service work. Orders for parts marked with "o" will be processed, but allow for additional delivery time.

**(5) Units for Capacitors, Inductors and Resistors**

The following units are assumed in schematic diagrams, electrical parts list and exploded views unless otherwise specified:

Capacitors; µF
Inductors; µH
Resistors; ohm

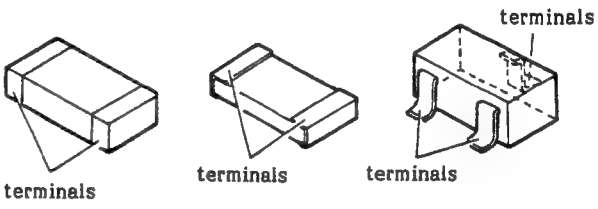
### 2-4-2. Replacement Procedure of Chip Parts

Required Tools

Soldering iron 20W;
If possible, use the soldering-iron tip heat-controller at 270 ± 10°C.
Braided wire;
SOLDER TAUL or equivalent
Sony Part No. 7-641-300-81
Solder; 0.6 mm dia. is recommended.
Tweezers

Soldering Conditions

Soldering iron temperature;
270 ± 10°C
Soldering time;
2 seconds per a pin



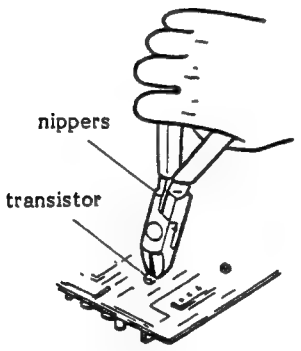

**Replacement of Resistor and Capacitor**

1. Place the soldering-iron tip onto the chip part and heat it up until the solder is melted. When the solder is melted, slide the chip part aside.
2. Make sure that there is no pattern peeling, damage and/or bridge around the desoldering positions.
3. After removing the chip part, presolder the area, in which the new chip part is to be placed, with a thin layer of solder.
4. Place new chip part in the desired position and solder both ends.

**CAUTION:** Do not use the chip part again once it has been removed.

**Replacement of Transistor and Diode**

1. Cut the terminals of the chip part with nippers.
2. Remove the leads cut as above.
3. Make sure that there is no pattern peeling, damage and/or bridge around the desoldering positions.
4. After removing the chip part, presolder the area, in which the new chip part is to be placed, with a thin layer of solder.
5. Place new chip part in the desired position and solder the terminals.




**Replacement of IC**

1. Using the braided wire, "SOLDER TAUL" Sony Part No. 7-641-300-81, remove the solder around the pins of the IC-chip to be removed.
2. While heating up the pins, remove the pins one by one using sharp-pointed tweezers.
3. Make sure that there is no pattern peeling, damage and/or bridge around the desoldering positions.
4. After removing the chip part, presolder the area, in which the new chip part is to be placed, with a thin layer of solder.
5. Place new chip part in the desired position and solder the pins.

**2-4-3. Replacing the Backup Battery**

The IF-139 board is provided with a RAM backup battery. When necessary, replace it using the procedure described below:
(When replacing the RAM backup battery, be sure to use the battery listed in SECTION D: "REPLACEABLE PARTS & OPTIONAL FIXTURES".)

(1) How to replace the battery

When the battery reaches the end of its life, the message "BACKUP ERROR" will be displayed on the control panel, and also the system error lamp on the control panel will light. In this case, switch the DVPC-1000 OFF, remove the IF-139 board, and replace the battery with a new one.

(2) After replacing the battery

① Confirm that the IF-139 board has been installed, then switch the DVPC-1000 ON.
② When the DVR-1000 is switched ON, the system error lamp on the contrl panel will light, and the error message "BACKUP ERROR" will appear on the screen.
(The backup data will be automatically initialized.)
③ Switch the DVPC-1000 OFF and then ON again, and confirm that the error message is not displayed.

Note: The "BACKUP ERROR" error message will appear when the battery on one of the boards shown below reaches the end of its life:
DVR-1000: SY-69 board.
DVPC-1000: IF-139 board
If the error message remains despite replacing the battery on one board with a new one, either the battery contact is faulty or the battery on the other board reaches the end of its life.

## 2-5. FUNCTION OF SWITCHES AND JUMPERS

### 2-5-1. Index of Switches and Jumpers

**AA-29 BOARD** — Section


S101: CH-1 ANALOG AUDIO INPUT LEVEL PRE/VAR SW.....2-5-2
S201: CH-2 ANALOG AUDIO INPUT LEVEL PRE/VAR SW.....2-5-2
S301: CH-3 ANALOG AUDIO INPUT LEVEL PRE/VAR SW.....2-5-2
S401: CH-4 ANALOG AUDIO INPUT LEVEL PRE/VAR SW.....2-5-2
S501: CH-1 ANALOG AUDIO OUTPUT LEVEL PRE/VAR SW.....2-5-2
S601: CH-2 ANALOG AUDIO OUTPUT LEVEL PRE/VAR SW.....2-5-2
S701: CH-3 ANALOG AUDIO OUTPUT LEVEL PRE/VAR SW.....2-5-2
S801: CH-4 ANALOG AUDIO OUTPUT LEVEL PRE/VAR SW.....2-5-2

CN111/112(JP101/102):
CH-1 FEEDBACK ON/OFF.....2-5-2
CN211/212(JP201/202):
CH-2 FEEDBACK ON/OFF.....2-5-2
CN311/312(JP301/302):
CH-3 FEEDBACK ON/OFF.....2-5-2
CN411/412(JP401/402):
CH-4 FEEDBACK ON/OFF.....2-5-2


**AE-06 BOARD** — Section


S1: AUDIO SEGMENT SIGNAL DELAY SW...2-5-7

CN1(JP1):
UPI TEST.....2-5-7
CN2: VERSION SELECT.....2-5-7


**AN-01 BOARD** — Section


S1-1: CONCEALMENT OFF SW.....2-5-11,3-6-5
S1-2: MUTE INHIBIT SW.....2-5-11,3-6-6
S1-3: BYPASS;DIGITAL AUDIO BYPASS SW..2-5-11,3-4
S1-4: Always set to off.
S1-5: Always set to off.
S1-6: Always set to off.
S1-7: Always set to off.
S1-8: Always set to off.
S2: MUTING TIME SW.....2-5-11
S3: MUTING DELAY SELECT SW.....2-5-11
S4: DIGITAL AUDIO OUTPUT DELAY SW (LSB).....2-5-11
S5: DIGITAL AUDIO OUTPUT DELAY SW (MSD).....2-5-11
S6: ADVANCE AUDIO DELAY SW (LSB)....2-5-11
S7: ADVANCE AUDIO DELAY SW (MSB)....2-5-11
S8: ADVANCE RETURN DELAY SW (LSB)...2-5-11
S9: ADVANCE RETURN DELAY SW (MSB)...2-5-11
S10: Not used.

JP1: UPI TEST.....2-5-11
JP2: ADVANCE AUDO MONITOR ON SW.....2-5-11,3-6-7
JP3: Always open.
JP4: AUDIO LEVEL +6dB/+12dB SELECT...2-5-11


**AP-14 BOARD** — Section


S1: ADVANCE RETURN DELAY(MSB).....2-5-12
S2: ADVANCE RETURN DELAY(LSB).....2-5-12
S3: PB AUDIO DELAY (MSB).....2-5-12
S4: PB AUDIO DELAY (LSB).....2-5-12

CN1(JP1):
UPI TEST .....2-5-12


**AT-45 BOARD** — Section


JP101/102:
CH-1 ANALOG AUDIO OUTPUT LEVEL..2-5-17
JP201/202:
CH-2 ANALOG AUDIO OUTPUT LEVEL..2-5-17
JP301/302:
CH-3 ANALOG AUDIO OUTPUT LEVEL..2-5-17
JP401/402:
CH-4 ANALOG AUDIO OUTPUT LEVEL..2-5-17


**AU-86 BOARD** — Section


S1: AUDIO TEST SIGNAL SELECT SW.....2-5-6,3-6-1
S2: AUDIO INPUT SELECT XLR/DSUB SW..2-5-6
S3: AUDIO INPUT SELECT DIG/ANA SW...2-5-6
S4-1: TEST SIGNAL ENABLE SW.....2-5-6,3-6-1
S4-2: Not used.
S4-3: CH-4 RECORD DATA SELECT SW.....2-5-6
S4-4: CH-3 RECORD DATA SELECT SW.....2-5-6
S4-5: CH-2 RECORD DATA SELECT SW.....2-5-6
S4-6: CH-1 RECORD DATA SELECT SW.....2-5-6
S4-7: CH-1/2 INPUT MODE SELECT MONO/STEREO SW.....2-5-6
S4-8: CH-3/4 INPUT MODE SELECT MONO/STEREO SW.....2-5-6
S5: DIGITAL AUDIO DELAY SW.....2-5-6

CN1(JP1):
UPI TEST.....2-5-6
CN2: VERSION SELECT.....2-5-6


**CI-01 BOARD** — Section


SW101-1: INNER CORECTION OFF SW.....2-5-15,3-5-7
SW101-2: AUDIO OUTER CORRECTION OFF SW.2-5-15,3-6-4
SW101-3: BYPASS-3 SW.....2-5-15,3-4
SW101-4: INTER CHANGE ON SW.....2-5-15
SW101-5: INNER DECODER BYPASS TEST.....2-5-15
SW101-6: SWAP TEST DIRECTION SW.....2-5-15,3-5-5
SW101-7: Not used.
SW101-8: Not used.

CN5: Always open.
CN6: UPI TEST.....2-5-15
CN7: SWAP TEST.....2-5-15,3-5-5


**FM-09A,B BOARD** — Section


S1-1: DE-SHUFFLING THROUGH SW.....2-5-14,3-5-3
S1-2: BYPASS-4 SW.....2-5-14,3-4
S1-3: TEMPORAL CONCEALMENT OFF SW.....2-5-14
S1-4: Not used.
S1-5: OUTER CORRECTION OFF.....2-5-14,3-5-7
S1-6: Not used.
S1-7: Not used.
S1-8: Not used.

S2-1: Always set to off.
S2-2: Always set to off.
S2-3: Always set to off.
S2-4: Always set to off.
S2-5: Always set to off.
S2-6: Always set to off.
S2-7: Always set to off.
S2-8: INHIBIT CH SELECT SW.....2-5-14,3-5-11

S3-1: Always set to off.
S3-2: FRAME MEMORY TEST SW.....2-5-14,3-5-8
S3-3: Always set to off.
S3-4: 1H DE-SHUFFLE MEMORY TEST SW....2-5-14,3-5-9
S3-5: Always set to off.
S3-6: Always set to off.
S3-7: OUTPUT DATA INHIBIT SW.....2-5-14,3-5-11
S3-8: Always set to off.

## (2-5-1. Index of Switches and Jumpers)


S4 to 9:
Not used.

CN5: UPI TEST.....2-5-14
CN6: TEST ENABLE.....2-5-14
CN7: Always open.
CN8: Always open.
CN9: Always open.
CN10: HEAD DE-INTERLEAVE FLAG TEST....2-5-14,3-5-10
CN11: Always open.
CN12: A/C-CH FRAME MEMORY READ INHIBIT.....2-5-14
CN13: BYPASS-4:A/C-CH DATA INPUT INHIBIT.....2-5-14
CN21: Always open.
CN22: B/D-CH FRAME MEMORY READ INHIBIT.....2-5-14
CN23: BYPASS 4:B/D-CH INPUT DATA INHIBIT.....2-5-14

**IE-17 BOARD** **Section**

S1-1: B/D-CH DELAY SW.....2-5-9
S1-2: B/D-CH DELAY SW.....2-5-9
S1-3: B/D-CH DELAY SW.....2-5-9
S1-4: B/D-CH DELAY SW.....2-5-9
S1-5: B/D-CH DELAY SW.....2-5-9
S1-6: B/D-CH DELAY SW.....2-5-9
S1-7: B/D-CH DELAY SW.....2-5-9
S1-8: B/D-CH DELAY SW.....2-5-9

S2-1: EE DELAY SW (525/60 SYSTEM).....2-5-9
S2-2: EE DELAY SW (525/60 SYSTEM).....2-5-9
S2-3: EE DELAY SW (525/60 SYSTEM).....2-5-9
S2-4: EE DELAY SW (525/60 SYSTEM).....2-5-9
S2-5: EE DELAY SW (525/60 SYSTEM).....2-5-9
S2-6: EE DELAY SW (525/60 SYSTEM).....2-5-9
S2-7: EE DELAY SW (525/60 SYSTEM).....2-5-9
S2-8: EE DELAY SW (525/60 SYSTEM).....2-5-9

S3-1: EE DELAY SW (625/50 SYSTEM).....2-5-9
S3-2: EE DELAY SW (625/50 SYSTEM).....2-5-9
S3-3: EE DELAY SW (625/50 SYSTEM).....2-5-9
S3-4: EE DELAY SW (625/50 SYSTEM).....2-5-9
S3-5: EE DELAY SW (625/50 SYSTEM).....2-5-9
S3-6: EE DELAY SW (625/50 SYSTEM).....2-5-9
S3-7: EE DELAY SW (625/50 SYSTEM).....2-5-9
S3-8: EE DELAY SW (625/50 SYSTEM).....2-5-9

CN1: SCRAMBLE INHIBIT.....2-5-9,3-5-4
CN2: COMPULSORY REC.....2-5-9
CN3: Always open. 2-5-9

**IF-139 BOARD** **Section**

S1: SYSTEM RESET SW .....2-5-5
S2: SYSTEM SELECT:525/625 SW.....2-5-5
S3: TEST ON/OFF SW.....2-5-5
S4: FREEZE SW.....2-5-5
S5: Not used.
S6: BOARD ID SW.....2-5-5

**IV-14 BOARD** **Section**

JP1/2: ANALOG AUDIO INPUT IMPEDANCE CH-4.....2-5-18
JP3/4/5/6: ANALOG AUDIO INPUT LEVEL CH-4...2-5-18
JP7/8: ANALOG AUDIO INPUT IMPEDANCE CH-3.....2-5-18
JP9/10/11/12: ANALOG AUDIO INPUT LEVEL CH-3...2-5-18
JP13/14: ANALOG AUDIO INPUT IMPEDANCE CH-2.....2-5-18
JP15/16/17/18: ANALOG AUDIO INPUT LEVEL CH-2...2-5-18
JP19/20: ANALOG AUDIO INPUT IMPEDANCE CH-1.....2-5-18
JP21/22/23/24: ANALOG AUDIO INPUT LEVEL CH-1...2-5-18

**PG-13 BOARD** **Section**

S1: AUDIO TEST SIGNAL SELECT SW.....2-5-4,3-6-1
S2-1: AUDIO MONITOR SELECT 1 SW.....2-5-4,3-6-2
S2-2: AUDIO MONITOR SELECT 2 SW.....2-5-4,3-6-2
S2-3: AUDIO EMPHASIS ON/OFF SW.....2-5-4
S2-4: AUDIO DE-EMPHASIS ON/OFF SW.....2-5-4
S2-5: AUDIO DIGITAL MIX CH-1 ON/OFF SW.....2-5-4
S2-6: AUDIO DIGITAL MIX CH-2 ON/OFF SW.....2-5-4
S2-7: AUDIO DIGITAL MIX CH-3 ON/OFF SW.....2-5-4
S2-8: AUDIO DIGITAL MIX CH-4 ON/OFF SW.....2-5-4
S3-1: BYPASS-6 SW.....2-5-4,3-4
S3-2: TEST-6:VIDEO TEST SIGNAL OUTPUT SW.....2-5-4,3-5-1
S3-3: BYPASS-7 SW.....2-5-4,3-4
S3-4: TEST-7:AUDIO TEST SIGNAL OUTPUT.2-5-4,3-6-1
S3-5: ANALOG VIDEO OUTPUT SELECT: RGB Y/R-Y/B-Y SW.....2-5-4
S3-6: PB BYPASS:INPUT CHECK SW.....2-5-4,3-4,3-6-2
S3-7: Not used.
S3-8: Not used.
S4: VIDEO INPUT SELECT :RGB/Y,R-Y, B-Y SW.....2-5-4
S5: VIDEO INPUT CONNECTOR SELECT BNC/MULTI SW.....2-5-4

CN1 (JP1/2): UPI TEST.....2-5-4

**SY-70A,B BOARD** **Section**

S1-1: A/C-CH DATA INHIBIT SW.....2-5-16,3-5-6
S1-2: B/D-CH DATA INHIBIT SW.....2-5-16,3-5-6
S1-3: BYPASS-1;SERIAL EE SW.....2-5-16,3-4
S1-4: BYPASS-2;PARALLEL EE SW.....2-5-16,3-4
S1-5: SWAP1 TEST SW(TBC IN).....2-5-16,3-5-5
S1-6: SWAP1 TEST DIRECTION SW.....2-5-16,3-5-5
S1-7: SWAP2 TEST SW(TBC OUT).....2-5-16,3-5-5
S1-8: SWAP2 TEST DIRECTION/ERROR ADD CH SELECT.....2-5-16,3-5-5,3-5-7
S2: ERROR ADD SIZE SW(LSB).....2-5-16,3-5-7
S3: ERROR ADD SIZE SW(MSB).....2-5-16,3-5-7
S4: ERROR ADD POSITION SW(LSB).....2-5-16,3-5-7
S5: ERROR ADD POSITION SW(MSB).....2-5-16,3-5-7
S6: ERROR ADD SIZE SW(SAMPLE).....2-5-16,3-5-7
S7: ERROR ADD TEST MODE SELECT SW...2-5-16,3-5-7

CN5: TBC MEMORY TEST1.....2-5-16,3-5-6
CN6: UPI TEST.....2-5-16
CN7: TBC MEMORY TEST2.....2-5-16,3-5-6
CN8: DE-SCRAMBLE INHIBIT.....2-5-16,3-5-4
CN9: ERROR ADD TEST.....2-5-16,3-5-7
CN10: SWAP TEST ENABLE.....2-5-16,3-5-5
CN11: JUMP TEST ENABLE.....2-5-16,3-5-6
CN12: TEST SIGNAL OUTPUT.....2-5-16,3-5-1

(2-5-1. Index of Switches and Jumpers)


TG-28 BOARD — Section

S1: ADVANCE AUDIO DELAY CONT (625/50) ..... 2-5-10
S2: ADVANCE AUDIO DELAY CONT (525/60) ..... 2-5-10
S3: SPOT ERASE FADE TIME CONT ..... 2-5-10
S4: CONFI AUDIO DELAY(625/50) ..... 2-5-10
S5: CONFI AUDIO DELAY(525/60) ..... 2-5-10
S6-1: TEST SW ..... 2-5-10
S6-2: TEST SW ..... 2-5-10
S6-3: TEST SW ..... 2-5-10
S6-4: TEST SW ..... 2-5-10
S6-5: TEST SW ..... 2-5-10
S6-6: TEST SW ..... 2-5-10
S6-7: TEST SW ..... 2-5-10
S6-8: TEST SW ..... 2-5-10,3-4
S7: REFERENCE INPUT SELECT DIG/ANA SW ..... 2-5-10
CN1: UPI TEST ..... 2-5-10

VA-45 BOARD — Section

S1-1: TEST SIGNAL SELECT SW ..... 2-5-3,3-5-1
S1-2: OFFSET ON/OFF SW ..... 2-5-3
S1-3: Not used.
S1-4: Not used.
S1-5: Not used.
S1-6: Not used.
S1-7: Not used.
S1-8: Not used.

S2-1: Not used.
S2-2: V BLANKING SELECT SW ..... 2-5-3
S2-3: V BLANKING SELECT SW ..... 2-5-3
S2-4: V BLANKING SELECT SW ..... 2-5-3
S2-5: V BLANKING SELECT SW ..... 2-5-3
S2-6: V BLANKING SELECT SW ..... 2-5-3
S2-7: V BLANKING SELECT SW ..... 2-5-3
S2-8: V BLANKING SELECT SW ..... 2-5-3

S3-1: V BLANKING SELECT SW ..... 2-5-3
S3-2: V BLANKING SELECT SW ..... 2-5-3
S3-3: V BLANKING SELECT SW ..... 2-5-3
S3-4: V BLANKING SELECT SW ..... 2-5-3
S3-5: V BLANKING SELECT SW ..... 2-5-3
S3-6: Not used.
S3-7: Not used.
S3-8: Not used.

S101: ANALOG VIDEO INPUT LEVEL PRE/VAR SW ..... 2-5-3
S701: ANALOG VIDEO OUTPUT LEVEL PRE/VAR SW ..... 2-5-3

CN5/6(JP5/6):
Y DIGITAL DELAY ..... 2-5-3
CN7/8(JP7/8):
R-Y DIGITAL DELAY ..... 2-5-3
CN9/10(JP9/10):
B-Y DIGITAL DELAY ..... 2-5-3
CN11/12(JP11/12):
Y DIGITAL DELAY ..... 2-5-3
CN13/14/15/16/17(JP13/4/15/16/17):
D/A C CLOCK ..... 2-5-3
CN18/19/20/21/22(JP18/19/20/21/22):
D/A Y CLOCK ..... 2-5-3
CN23/24(JP23/24):
D/A CLOCK ..... 2-5-3
CN25/26/27/28/29(JP25/26/27/28/29):
A/D Y CLOCK ..... 2-5-3
CN30/31(JP30/31):
A/D CLOCK ..... 2-5-3
CN32/33/34/35/36(JP32/33/34/35/36)
A/D C CLOCK ..... 2-5-3
CN37/38(JP37/38):
SETUP DELEDTE ON/OFF ..... 2-5-3
CN39/40(JP39/40):
INPUT BETACAM MASK ..... 2-5-3

VE-12 BOARD — Section

S1-1: MAPPING OFF SW ..... 2-5-8,3-5-2
S1-2: SHUFFLING OFF SW ..... 2-5-8,3-5-3
S1-3: BYPASS-3 SW ..... 2-5-8,3-4
S1-4: BYPASS-4 SW ..... 2-5-8,3-4
S1-5: BYPASS-5 SW ..... 2-5-8,3-4
S1-6: Not used.
S1-7: Not used.
S1-8: Not used.
S2: VIDEO INPUT SELECT DIG/ANA SW ..... 2-5-8

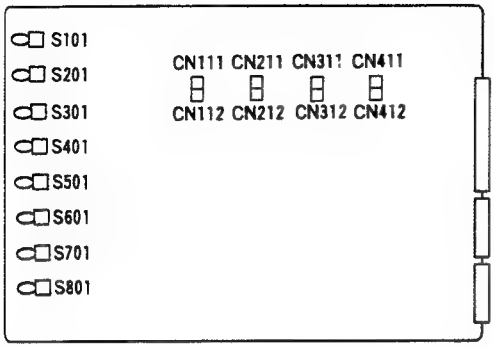
CN1: UPI TEST ..... 2-5-8

VN-01 BOARD — Section

S1-1: DE-MAPPING OFF SW ..... 2-5-13,3-5-2
S1-2: CONCEALMENT OFF SW ..... 2-5-13,3-5-13
S1-3: BYPASS-5 SW ..... 2-5-13,3-4
S1-4: Always set to off.
S1-5: Always set to off.
S1-6: PINK DISPLAY MODE STATIC/4SPL SW ..... 2-5-13,3-5-12
S1-7: PINK DISPLAY ON/OFF SW ..... 2-5-13,3-5-12
S1-8: Not used.
S2-1: ERROR ADD TEST SW ..... 2-5-13,3-5-13
S2-2: CONCEALMENT ALGORITHM CONTROL ..... 2-5-13,3-5-13
S2-3: CONCEALMENT ALGORITHM CONTROL ..... 2-5-13,3-5-13
S2-4: CONCEALMENT ALGORITHM CONTROL ..... 2-5-13,3-5-13
S2-5: CONCEALMENT ALGORITHM CONTROL ..... 2-5-13,3-5-13
S2-6: IDEAL DIR DISPLAY SW ..... 2-5-13,3-5-12
S2-7: DISPLAY CONT 1 ..... 2-5-13,3-5-12
S2-8: DISPLAY CONT 2 ..... 2-5-13,3-5-12
S3: Not used.
S4: DIGITAL DELAY SW(LSB) ..... 2-5-13
S5: DIGITAL DELAY SW(MSB) ..... 2-5-13

CN1: ERROR PATTERN SELECT (ERV) ..... 2-5-13,3-5-13
CN2: ERROR PATTERN SELECT (ERV) ..... 2-5-13,3-5-13
CN3: ERROR PATTERN SELECT (ERV) ..... 2-5-13,3-5-13
CN4: ERROR PATTERN SELECT (ERH) ..... 2-5-13,3-5-13
CN5: ERROR PATTERN SELECT (ERH) ..... 2-5-13,3-5-13
CN6: ERROR PATTERN SELECT (ERH) ..... 2-5-13,3-5-13
CN7: ERROR PATTERN MODE SELECT ..... 2-5-13,3-5-13
CN8: ERROR PATTERN MODE SELECT ..... 2-5-13,3-5-13
CN9: CONCEALMENT RATE DISPLAY MODE ..... 2-5-13
CN10: CONCEALMENT RATE DISPLAY MODE ..... 2-5-13
CN11: CONCEALMENT RATE DISPLAY MODE ..... 2-5-13
CN12: CONCEALMENT RATE DISPLAY MODE ..... 2-5-13
CN14: UPI TEST ..... 2-5-13

## 2-5-2. AA-29 Board



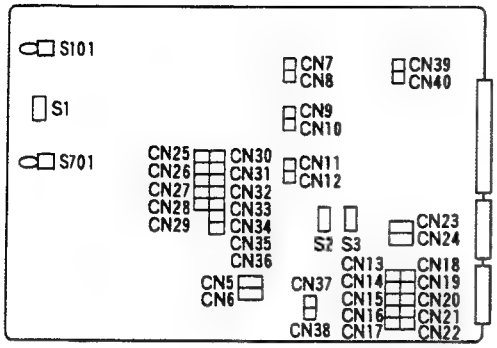

**S101: CH-1 analog audio input level PRE/VAR switch**
**S201: CH-2 analog audio input level PRE/VAR switch**
**S301: CH-3 analog audio input level PRE/VAR switch**
**S401: CH-4 analog audio input level PRE/VAR switch**
These are the PRESET/VARIABLE selector switches for the analog audio input levels.
**PRE:** The input level is set to the reference level.
**VAR:** The input level can be varied across a range from - ∞ to +12dB with respect to the reference level. The levels are adjusted using variable resistors RV101(CH-1), RV201(CH-2), RV301(CH-3) and RV401(CH-4), which are positioned underneath the switches.
The input signal levels can be checked on the input level meters of the control panel. The signal levels after A/D conversion are indicated.

**S501: CH-1 analog audio output level PRE/VAR switch**
**S601: CH-2 analog audio output level PRE/VAR switch**
**S701: CH-3 analog audio output level PRE/VAR switch**
**S801: CH-4 analog audio output level PRE/VAR switch**
These are the PRESET/VARIABLE selector switches for the analog audio output levels.
**PRE:** The output level is set to the reference level.
**VAR:** The output level can be varied across a range from - ∞ to +12dB with respect to the reference level. The levels are adjusted using variable resistors RV501(CH-1), RV601(CH-2), RV701(CH-3) and RV801(CH-4), which are positioned underneath the switches.
The analog output signal levels after D/A conversion are adjusted here. The digital signal levels before D/A conversion are indicated on the input level meters of the control panel, and so the meter displays will not change even when the variable resistors are adjusted.

**CN111/112 (JP101/102): CH-1 feedback ON/OFF jumpers**
**CN211/212 (JP201/202): CH-2 feedback ON/OFF jumpers**
**CN311/312 (JP301/302): CH-3 feedback ON/OFF jumpers**
**CN411/412 (JP401/402): CH-4 feedback ON/OFF jumpers**
CN112, 212, 312 and CN412 are shorted when the DC offset of the A/D converter is adjusted.
Normally, CN111, 211, 311 and CN411 are shorted.

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

### 2-5-3. VA-45 Board




*: These switches function only when the TEST switch S3 on the IF-139 board is ON. The standard setting position for these switches is OFF.

*** S1-1: TEST SIGNAL SELECT switch**

This switch selects the output of the video test signal generator on the VA-45 board. For details, refer to the description of TEST6 switch S3-2/PG-13.

*** S1-2: OFFSET ON/OFF switch**

When S1-2 is set to ON with Y/R-Y/B-Y output for the video analog ouptut 1 connector, a 50% offset is applied to R-Y, B-Y color difference signals output. This is used when viewing the Y/R-Y/B-Y output on the RGB monitor.

**S1-3 to 8:** Not used.

**S2, S3: V BLANKING SELECT switches**

These switches select the blanking lines. When the unit is shipped, all the switches are set to OFF. When they are set to ON, the corresponding video lines are blanked. The table below shows the relationship between the blanking lines and the switches.

| S2 | BLANKING LINE | |
|---|---|---|
| | 525/60 | 625/50 |
| S2-1 | ——— | ——— |
| S2-2 | 14 (276) | 11,324 |
| S2-3 | 15 (277) | 12,325 |
| S2-4 | 16 (278) | 13,326 |
| S2-5 | 17 (279) | 14,327 |
| S2-6 | 18 (280) | 15,328 |
| S2-7 | 19 (281) | 16,329 |
| S2-8 | 20 (282) | 17,330 |

| S3 | BLANKING LINE | |
|---|---|---|
| | 525/60 | 625/50 |
| S3-1 | ——— | 18,331 |
| S3-2 | ——— | 19,332 |
| S3-3 | ——— | 20,333 |
| S3-4 | ——— | 21,334 |
| S3-5 | ——— | 22,335 |
| S3-6 | ——— | ——— |
| S3-7 | ——— | ——— |
| S3-8 | ——— | ——— |

**S101: Analog video input level PRE/VAR switch**

This is the PRESET/VARIABLE selector switch for the analog video input level. It simultaneously controls the input levels of the three R,G,B or Y,R-Y,B-Y channels.

**PRE:** The input level is set at the reference level (0.7Vp-p).

**VAR:** The input level can be varied across a +/-20% range with respect to the reference level. The level is adjusted by RV310 on the front of the board.

**S701: Analog video output level PRE/VAR switch**

This is the PRESET/VARIABLE selector switch for the analog video output level. It simultaneously controls the output levels of the R,G,B or Y,R-Y,B-Y channels.

**PRE:** The output level is set at the reference level (0.7Vp-p).

**VAR:** The output level can be varied across a +/-20% range with respect to the reference level. The level is adjusted by RV701 on the front of the board.

**CN5-CN12 (JP5-JP12): Digital signal delay adjustment jumpers**

These jumpers adjust the delay of the digital video signals. Their settings should not be changed. The standard setting positions are as shown below.

| JUMPER PLUG | FUNCTION | SETTING |
|---|---|---|
| CN5/6 | Y DIGITAL DELAY | CN5; OPEN<br>CN6; SHORT |
| CN7/8 | R-Y DIGITAL DELEY | CN7; OPEN<br>CN8; SHORT |
| CN9/10 | B-Y DIGITAL DELAY | CN9; OPEN<br>CN10; SHORT |
| CN11/12 | Y DIGITAL DELAY | CN12; OPEN<br>CN11; SHORT |

**CN13-17 (JP13-17): D/A C CLOCK adjustment jumper**
**CN18-22 (JP18-22): D/A Y CLOCK adjustment jumper**
**CN23/24 (JP23/24): D/A CLOCK adjustment jumper**
**CN25-29 (JP25-29): A/D Y CLOCK adjustment jumper**
**CN30/31 (JP30/31): A/D CLOCK adjustment jumper**
**CN32-36 (JP32-36): A/D C CLOCK adjustment jumper**

These jumpers adjust the A/D and D/A conversion clocks. Adjustments are made before the unit is shipped and so the settings of these jumper plugs should not be changed unless absolutely necessary.

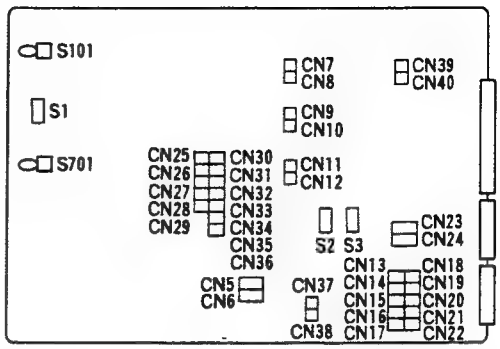
(2-5-3. VA-45 Board)

**CN37/38 (JP37/38): SETUP DELETE ON/OFF jumpers**
(Valid only with 525/60 system)
These jumpers select whether the Y signal setup is to be deleted or not when the Betacam output signal has been supplied to the video analog input 2 connector.
When CN38 is shorted, the setup of the Y input signal is deleted, and after the signal level has been adjusted, the signal is A/D converted. When CN37 is shorted, the Y input signal is A/D converted in its original form.
Normally, CN38 is shorted and CN37 is kept open.

**CN39/40 (JP39/40): INPUT BETACAM MASK jumpers**
(Valid only with 525/60 system)
Any fluctuations in the setup position of the video Y signal supplied to the video analog input 2 connector may cause the blanking level section to enter inside the digital active line and a signal with a lower level than the pedestal level to be A/D converted and recorded.
In cases like this, several samples at the head of the digital active line are forcibly replaced by the pedestal level when CN40 is shorted. When CN39 is shorted, the input signal is recorded in its original form.
Initialization entails shorting CN39 and keeping CN40 open.

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

**2-5-3. VA-45 Board**




*: These switches function only when the TEST switch S3 on the IF-139 board is ON. The standard setting position for these switches is OFF.

*** S1-1 to 4: TEST SIGNAL SELECT switch**
This switch selects the output of the video test signal generator on the VA-45 board. For details, refer to the description of TEST6 switch S3-2/PG-13.

*** CN2: OFFSET ON/OFF switch**
When CN2 is set to SHORT with Y/R-Y/B-Y output for the video analog ouptut 1 connector, a 50% offset is applied to R-Y, B-Y color difference signals output. This is used when viewing the Y/R-Y/B-Y output on the RGB monitor.

**S1-3 to 8:** Not used.

**S2, S3: V BLANKING SELECT switches**
These switches select the blanking lines. When the unit is shipped, all the switches are set to OFF. When they are set to ON, the corresponding video lines are blanked. The table below shows the relationship between the blanking lines and the switches.

| S2 | BLANKING LINE | |
|---|---|---|
| | 525/60 | 625/50 |
| S2-1 | ——— | ——— |
| S2-2 | 14 (276) | 11,324 |
| S2-3 | 15 (277) | 12,325 |
| S2-4 | 16 (278) | 13,326 |
| S2-5 | 17 (279) | 14,327 |
| S2-6 | 18 (280) | 15,328 |
| S2-7 | 19 (281) | 16,329 |
| S2-8 | 20 (282) | 17,330 |

| S3 | BLANKING LINE | |
|---|---|---|
| | 525/60 | 625/50 |
| S3-1 | ——— | 18,331 |
| S3-2 | ——— | 19,332 |
| S3-3 | ——— | 20,333 |
| S3-4 | ——— | 21,334 |
| S3-5 | ——— | 22,335 |
| S3-6 | ——— | ——— |
| S3-7 | ——— | ——— |
| S3-8 | ——— | ——— |

(2-5-3. VA-45 Board)

**S101: Analog video input level PRE/VAR switch**

This is the PRESET/VARIABLE selector switch for the analog video input level. It simultaneously controls the input levels of the three R,G,B or Y,R-Y,B-Y channels.

**PRE:** The input level is set at the reference level (0.7Vp-p).

**VAR:** The input level can be varied across a +/-20% range with respect to the reference level. The level is adjusted by RV310 on the front of the board.

**S701: Analog video output level PRE/VAR switch**

This is the PRESET/VARIABLE selector switch for the analog video output level. It simultaneously controls the output levels of the R,G,B or Y,R-Y,B-Y channels.

**PRE:** The output level is set at the reference level (0.7Vp-p).

**VAR:** The output level can be varied across a +/-20% range with respect to the reference level. The level is adjusted by RV701 on the front of the board.

**DL1, DL2, DL4, DL5; Digital signal delay adjustment**

These are used for delay adjustment of the digital video signal. Do not change the settings of these delay lines.

DL4; D/A R-Y CLOCK adjustment
DL5; D/A B-Y CLOCK adjustment
DL1; A/D R-Y CLOCK adjustment
DL2; A/D B-Y CLOCK adjustment

**A/D and D/A converter clock adjustment**

These are delay lines.

These delay lines are adjusted before shipping. Do not change their settings unless necessary.

**CN1; SETUP DELETE ON /OFF jumper**

(effective only when the 525/60 system is used)

This jumper is used to select whether or not to delete the setup of Y signal when a beta cam output signal is applied to the VIDEO ANALOG INPUT-2 connector.

When CN1 is shorted, the setup for input Y signal is deleted and the level is adjusted before converting from analog to digital. When CN1 is open, the input Y signal is converted from analog to digital as it is.

CN1 is shorted during normal operation.

**CN2; OFFSET ON/OFF jumper**

When CN2 is shorted with the selection of Y/R-Y/B-Y at the VIDEO ANALOG OUTPUT-1 output, a 50% offset is applied to the color-difference signal (R-Y, B-Y) output. Use this jumper when you want to observe the Y/R-Y/B-Y output on the RGB monitor.

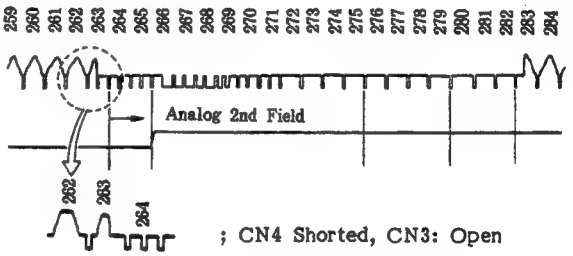
**CN3/4; SYNCHRONIZING SIGNAL DELETE ON/OFF jumper**

The analog video signal, the lines number 263 and 283 in the 525/60 system and the lines number 23 and 623 in the 625/50 system undergo half H blanking. But in the digital interface, full data are transmitted even to the above-mentioned lines and they are recorded.

The equalizing pulses of the line number 263 in the 525/60 system and of the line number 623 in the 625/50 system can be deleted by short circuiting CN3 and by opening CN4 so that the recorded signals are not affected by the equalizing pulses.

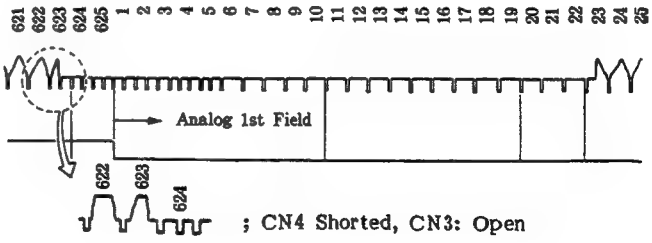
CN3 is shorted and CN4 is open during normal operation. At this time, the data is output in the analog format.

**525/60 System**




; CN4 Shorted, CN3: Open

**625/50 System**



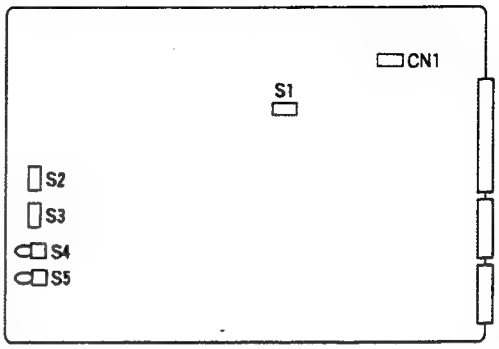

; CN4 Shorted, CN3: Open

(2-5-3. VA-45 Board)

**CN5; DIGITAL FORMAT OUTPUT ON/OFF jumper**

When CN5 is open, the lines number 263 and 283 in the 525/60 system and the lines number 23 and 623 in the 625/50 system undergo half H blanking.

## 2-5-4. PG-13 Board




*: These switches function only when TEST switch S3/IF-139 is ON. The standard setting position for these switches is OFF.

**: These switches function only when TEST switch S3/IF-139 is ON and the UPI TEST jumper JP1/PG-13 has been shorted. The standard setting position for these switches is OFF.

***: These switches function only when PR CONT (see Note) has been set to OFF on the SYSTEM SETUP sub menu.

**Note:** PR CONT= Processor control mode

*** S1: AUDIO TEST SIGNAL switch**

This switch selects the output of the audio test signal generator on the PG-13 board. For details, refer to the description of TEST7 switch S3-4/PG-13.

**** S2-1: AUDIO MONITOR SELECT 1 switch**

**** S2-2: AUDIO MONITOR SELECT 2 switch**

These switches are used to adjust and check the audio monitor signal system on the AA-29 and AT-45 boards. The signals indicated in the table below are output to the audio monitor output connector by setting these switches and PB BYPASS switch S3-6/PG-13.

| S3-6 | S2-1 | S2-2 | Audio monitor output (common to L/R CH) |
|---|---|---|---|
| ON | ON | ON | CH-1 analog audio input signal |
| | | OFF | CH-2 analog audio input signal |
| | OFF | ON | CH-3 analog audio input signal |
| | | OFF | CH-4 analog audio input signal |
| OFF | ON | ON | CH-1 analog audio output signal |
| | | OFF | CH-2 analog audio output signal |
| | OFF | ON | CH-3 analog audio output signal |
| | | OFF | CH-4 analog audio output signal |

(2-5-4. PG-13 Board)

**** S2-3: AUDIO EMPHASIS ON/OFF switch**

**** S2-4: AUDIO DE-EMPHASIS ON/OFF switch**

These switches are used to adjust and check the A/D and D/A converters. When the switches set to ON, the emphasis or de-emphasis circuits is activated.

Emphasis ON/OFF selection under normal operation is conducted on the DIGITAL AUDIO SETUP sub menu of the control panel. For details, refer to the DVR-1000 operation manual.

**** S2-5: AUDIO DIGITAL MIX CH-1 ON/OFF switch**

**** S2-6: AUDIO DIGITAL MIX CH-2 ON/OFF switch**

**** S2-7: AUDIO DIGITAL MIX CH-3 ON/OFF switch**

**** S2-8: AUDIO DIGITAL MIX CH-4 ON/OFF switch**

These switches select the digital audio channels for mixing and recording onto the cue channel.

When the switches are set to ON, the corresponding digital audio channels are mixed on a time-sharing basis and the signals are sent to the DVR-1000. Depending on the number of channels to be mixed, the signal level of the channels is set to 1/4 with 4-channel mixing, to 1/3 with 3-channel mixing and to 1/2 with 2-channel mixing.

Under normal operation, the digital mix channels are selected on the ANALOG CUE SETUP sub menu. For details, refer to the DVR-1000 operation manual.

*** S3-1: BYPASS-6 (video signal system) switch**

Bypass-6 is the mode for bypass inside the VA-45 board.

When S3-1 is ON, the bypass-6 mode is set.

For details on the bypass mode, refer to the section 3 "TEST MODE".

*** S3-2: TEST-6: VIDEO TEST SIGNAL OUTPUT switch**

This switch is used in combination with test signal select switch S1-1/VA-45, and it selects the output of the video test signal generator on the VA-45 board.

When S3-2 is ON, the signals below are output according to the S1-1/VA-45 setting.

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

| S3-2/PG-13 | S1-1/VA-45 | TEST SIGNAL |
|---|---|---|
| ON | OFF | COLOR BARS |
| | ON | MULTI BURST |

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

| S3-2/PG-13 | S1/VA-45 1 | 2 | 3 | 4 | TEST SIGNAL |
|---|---|---|---|---|---|
| ON | OFF | OFF | × | OFF | 100% COLOR BARS |
| | ON | OFF | × | OFF | 75% COLOR BARS |
| | × | ON | OFF | OFF | MULTI BURST |
| | × | ON | ON | OFF | RAMP |
| | × | × | × | ON | BLA |

*** S3-3: BYPASS-7 (audio signal system) switch**

Bypass 7 is the mode for bypass inside the PG-13 board.

When S3-3 is ON, the bypass 7 mode is set.

For details on the bypass mode, refer to the section 3 "TEST MODE".

*** S3-4: TEST-7: AUDIO TEST SIGNAL OUTPUT switch**

This switch is used in combination with audio test signal select switch S1/PG-13, and it selects the output of the audio test signal generator on the PG-13 board.

When S3-4 is ON, the test signals below are output according to the S1/PG-13 setting.

| S1 | TEST SIGNAL | APPLICATION |
|---|---|---|
| 0, 8 | 1 kHz, 0 VU | D/A converter frequency response check |
| 1, 9 | 200 Hz, 0 VU | |
| 2, A | 5 kHz, 0 VU | |
| 3, B | 10 kHz, 0 VU | |
| 4, C | 20 kHz, 0 VU | |
| 5, D | 1 kHz, +20 VU | |
| 6, E | Not used. | |
| 7, F | LINEARITY | D/A linearity check |

**S3-5: ANALOG VIDEO OUTPUT RGB/Y,R-Y,B-Y select switch**

This switch selects the output signal format of the analog video output 1 (BNC) connector.

When S3-5 is OFF, R/G/B/SYNC is used as the video output signal format; when it is ON, Y/R-Y/B-Y is used.

*** S3-6: PB BYPASS: INPUT CHECK switch**

This is the input check switch.

When S3-6 is ON, the analog video/audio input signals are output in their original form to the monitor output connector.

When Y/R-Y/B-Y is used as the format for the analog video input signal, the Y/R-Y/B-Y signals are output in their original form to the picture monitor output connector. Under normal operation, the input check can be conducted using the controls on the control panel.

(2-5-4. PG-13 Board)

**S3-7, 8:** Not used.

***** S4: INPUT VIDEO RGB/Y, R-Y, B-Y selector switch**

This switch selects the format of the analog video input signal. It is initialized to RGB.

This switch is valid only when PR CONT (processor control mode) is OFF. When PR CONT is ON, the signal format is selected on the VIDEO SETUP sub menu.

The setting of this switch is invalidated when video input select switch S2/VE-12 is set to DIG.

**RGB:** The RGB signal from analog input 1 connector is input.

**Y, R-Y, B-Y:** The Y/R-Y/B-Y signal from the analog input 1 or analog input 2 connector is input.
The input connector in question is designated by S5 which is described next.

***** S5: VIDEO INPUT CONNECTOR BNC/MULTI select switch**

This switch selects the input connector when Y/R-Y/B-Y has been specified as the input signal format by S4/PG-13.

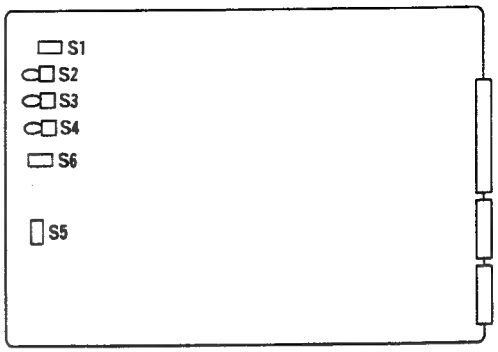
**BNC:** The analog input 1 connector (BNC) is specified as the input connector.

**MULTI:** The analog input 2 connector (12-pin multi) is specified as the input connector.

**CN1 (JP1): UPI TEST jumper**

This jumper is for the UPI test. Normally, it is kept open for use. When it is shorted, UPI suspends communication with the IF-139 board and it operates under the test program.

**2-5-5. IF-139 Board**




**S1: SYSTEM RESET switch**

When this switch is pressed, all the CPUs inside the DVPC-1000 are reset to the power-on status.

**S2: SYSTEM SELECT: 525/625 switch**

This switch selects the line standard for the input/output video signals. The switch setting appears on the front panel. Setting should be made as follows in accordance with the system in use.

**525:** When the 525/60 system is used

**625:** When the 625/50 system is used

**S3: TEST ON/OFF switch**

This switch selects the DVPC-1000 test mode. Normally, it is set to OFF for use.

**ON:** The DVPC-1000 is set to the test mode and the red lamp of the TEST MODE indicator on the front panel lights. The settings of the test DIP switches on the circuit boards are now made valid. A warning message appears on the control panel.

**OFF:** Normally, the switch is set to this position for use. The green lamp of the TEST MODE indicator on the front panel lights.
The settings of the test DIP switches on the circuit boards are now invalidated.

**S4: FREEZE switch**

This switch is for the freeze frame output signals. Freeze frame signals are output from the monitor output and video output connectors while S4 is set to its lower position.

This switch is valid only when the PR CONT (processor control mode) /SYSTEM SETUP sub menu is OFF. Freeze frame signals are also output when the F2 key is pressed on the HOME menu.

**S5:** Not used.

(2-5-5. IF-139 Board)

**S6: BOARD ID switch**

This switch selects the signals which are output to TP1 and TP2 (communication monitor) on the front of the IF-139 board.

The timing of the data writing from the IF-139 board to other boards can be monitored at TP1 (BDWR); the timing of the data reading from other boards can be monitored at TP2 (BDRD).

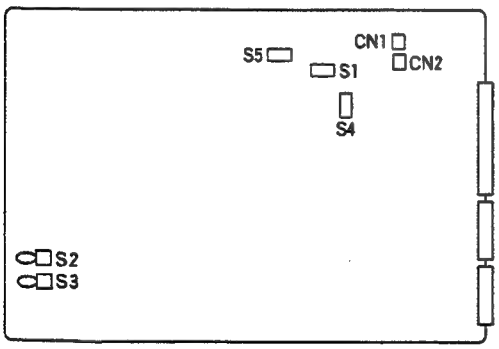
The S6 setting position determines the board whose communication is to be monitored.

| S6 | BOARD |
|---|---|
| 0 | SY-70B |
| 1 | SY-70A |
| 2 | CI-01 |
| 3 | FM-09B |
| 4 | FM-09A |
| 5 | VN-01 |
| 6 | AP-14 |
| 7 | AN-01 |

| S6 | BOARD |
|---|---|
| 8 | TG-28 |
| 9 | IE-17 *1 |
| A | VE-12 |
| B | AE-06 |
| C | AU-86 |
| D | PG-13 |
| E | Not used at present |
| F | |

*1: There is no communication at present between the IE-17 and IF-139 boards. This means that when S6 is set to "9", the level of the signals output to TP1 and TP2 will always be low.

**2-5-6. AU-86 Board**




*: These switches function only when TEST switch S3/IF-139 is ON. The standard setting position for these switches is OFF.

**: These switches function only when UPI test jumper CN1/AU-86 is shorted. The standard setting position for these switches is OFF.

***: These switches function only when PR CONT (see Note) has been set to OFF on the SYSTEM SETUP sub menu.

Note: PR CONT= Processor control mode

*** S1: AUDIO TEST SIGNAL switch**

This switch selects the output of the audio test signal generator on the AU-86 board. For details, refer to the description of TEST SIGNAL ENABLE switch S4-1/AU-86.

***** S2: AUDIO INPUT XLR/DSUB select switch**

This switch selects the digital audio input connector when DIG (digital) has been selected as the input signal format by AUDIO INPUT DIG/ANA select switch S3/AU-86.

This switch setting is valid only when PR CONT (processor control mode) is OFF. When PR CONT is ON, the input connector is selected on the DIGITAL AUDIO I/O SELECT sub menu.

This switch simultaneously sets the input connectors of all channels. It is not possible to set CH-1/2 and CH-3/4 separately.

XLR: The XLR connector is selected as the input connector.

DSUB: The DSUB connector is selected as the input connector.

***** S3: AUDIO INPUT DIG/ANA select switch**

This switch selects the format of the audio input signals. Its settings are valid only when PR CONT (processor control mode) is OFF. When PR CONT is ON, the signal format is selected on the DIGITAL AUDIO I/O SELECT sub menu.

ANA: The analog input signal from the audio analog input connector is selected.

DIG: The digital input signal from the audio digital input-1 (XLR) or audio digital input-2 (DSUB) connector is selected. The input connector at this time is selected by AUDIO INPUT XLR/DSUB select switch S2/AU-86.

(2-5-6. AU-86 Board)

*** S4-1: TEST SIGNAL ENABLE switch**

This switch is used in combination with AUDIO TEST SIGNAL select switch S1/AU-86 to select the output of the audio test signal generator on the AU-86 board. When S4-1 is ON, digital test data with the AES/EBU format are output from the test signal generator. The output signal at this time is selected by S1/AU-86.

| S1 | AUDIO TEST SIGNAL | CH | FREQ "Hz" | DETAILS OF CHANNEL STATUS DATA | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | PRO/ CONSUMER | AUDIO/ NON-AUDIO | PREF | CHAN | VALIDITY FLAG | CRCC |
| 0 | Sine wave 7FFF H 0000 H 8000 H | 1 | 250 | 1: PRO | 0: AUDIO | 0000 | 0000 | 0: VALID | NO ERROR |
| | | 2 | 500 | | | | | | |
| | | 3 | 1K | | | | | | |
| | | 4 | 2K | | | | | | |
| 1 | Triangular wave 7FFF H 0000 H 8000 H | 1 | 250 | 1: PRO | 1: NON-AUDIO | 1000 | 0001 | 0: VALID | NO ERROR |
| | | 2 | 500 | | | | | 1:IN-VALID | |
| | | 3 | 1K | 0: CONS. | 0: AUDIO | 1100 | 0100 | 0: VALID | ERROR |
| | | 4 | 2K | | | | | | |
| 2 | Ramp wave 5F80 H 0000 H | 1 | 250 | 1: PRO | 0: AUDIO | 1110 | 0010 | 0: VALID | ERROR |
| | | 2 | 500 | 0: CONS. | | 1100 | | | NO ERR |
| | | 3 | 1K | 1: PRO | | 1000 | 0011 | 1:IN-VALID | ERROR |
| | | 4 | 2K | 0: CONS. | | 0000 | | | NO ERR |
| 3 | Impulse (1T pulse) 7FFF H 0000 H | 1 | 250 | 0: CONS. | 0: AUDIO | 1110 | 0001 | 0: VALID | NO ERROR |
| | | 2 | 500 | | | 1110 | | | |
| | | 3 | 1K | 1: PRO | 1: NON-AUDIO | 1000 | 0010 | | |
| | | 4 | 2K | | | 1000 | | | |
| 4 | Sine wave (+20dB) 7FFF H 0000 H 8000 H | 1 | 1K | 1: PRO | 0: AUDIO | 0000 | 0000 | 0: VALID | NO ERROR |
| | | 2 | | | | | | | |
| | | 3 | | | | | | | |
| | | 4 | | | | | | | |
| 5 | Sine wave (+0 dB) 0CCD H 0000 H F333 H | 1 | 1K | 1: PRO | 0: AUDIO | 0000 | 0000 | 0: VALID | NO ERROR |
| | | 2 | | | | | | | |
| | | 3 | | | | | | | |
| | | 4 | | | | | | | |
| 6 | Sine wave (-20dB) 0188 H 0000 H FE78 H | 1 | 1K | 1: PRO | 0: AUDIO | 0000 | 0000 | 0: VALID | NO ERROR |
| | | 2 | | | | | | | |
| | | 3 | | | | | | | |
| | | 4 | | | | | | | |
| 7 | Random signal | 1 | — | 1: PRO | 0: AUDIO | 0000 | 0000 | 0: VALID | NO ERROR |
| | | 2 | | | | | | | |
| | | 3 | | | | | | | |
| | | 4 | | | | | | | |
| 8 to F | Not used. | | | | | | | | |

| PREF | |
|---|---|
| 0000 | DEFAULT |
| 1000 | OFF |
| 1100 | CD (50/15) |
| 1110 | CCITT |

| CHAN | |
|---|---|
| 0000 | DEFAULT |
| 0100 | STEREO |
| 0001 | 2CH MODE |
| 0010 | 1CH MODE |
| 0011 | PRE. /SEC. |

(2-5-6. AU-86 Board)

S4-2: Not used.

** S4-3: CH-4 RECORD DATA SELECT switch
** S4-4: CH-3 RECORD DATA SELECT switch
** S4-5: CH-2 RECORD DATA SELECT switch
** S4-6: CH-1 RECORD DATA SELECT switch
These switches select the audio recording data.
When the switches are OFF, the line input data are recorded; when they are ON, the advance return data from the AN-01 board are recorded.

** S4-7: CH-3/4 MODE MONO/STEREO select switch
** S4-8: CH-1/2 MODE MONO/STEREO select switch
These switches select the channel mode.
When the switches are ON, the corresponding channels are set to the 1-channel mode; when they are OFF, they are set to the 2-channel mode.
For normal operation, the channel mode is selected by the DIGITAL AUDIO I/O SELECT sub menu.

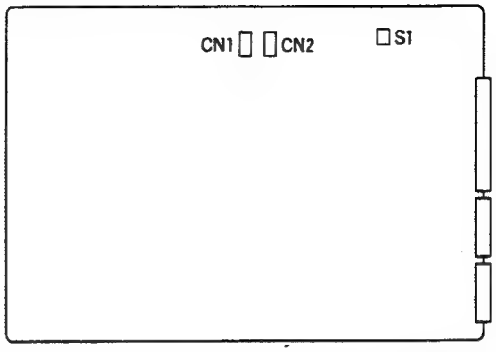
S5: DIGITAL AUDIO Delay Adjustment Switch
(only for the AU-86 board number that is 1-620-928-13 or after)
This is a delay adjustment switch for the digital audio input signal. When S5 is set to "0", the delay amount is 0 sample. When it is set to "F", the delay amount is 15 samples (15 x 20 sec). This switch is set to "5" at shipment.

CN1 (JP1): UPI TEST jumper
This is the UPI test jumper. Normally, it is kept open for use. When it is shorted, UPI suspends communication with the IF-139 board and it operates under the test program.

CN2; VERSION SELECT jumper
(AU-86 board number is 1-620-929-13 or later)
Perform setting according to the version of the software in the ROM (ICF4) on IF-139 board.
Open CN2 for IF1390127 or later, and short it for IF1390126 or earlier.

CN3: AUDIO LEVEL +6 dB/+12 dB SELECT jumper
This jumper selects a variable range of the audio digital output level. Refer to Section 2-5-11, "JP4: AUDIO LEVEL +6 dB/+12 dB select jumper" for the details.

2-5-7. AE-06 Board

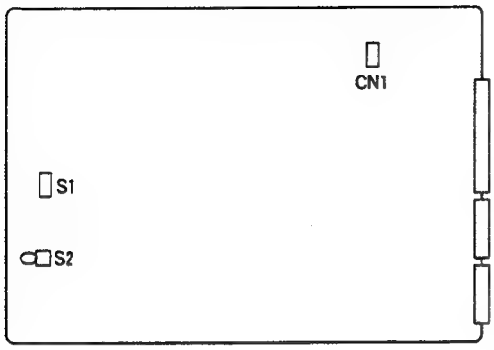



S1: AUDIO SEGMENT Signal Delay Adjustment Switch
(only for the AE-06 board number that is 1-620-929-12 or after)
This is a delay adjustment switch for the audio segment signal. When S1 is set to "0", the delay amount is 4 samples (4 x 20 sec). When it is set to "7", the delay amount is 11 samples (11 x 20 sec). This switch is set to "1" at shipment.

CN1 (JP1): UPI TEST jumper
This is the UPI test jumper. Normally, it is kept open for use. When it is shorted, UPI suspends communication with the IF-139 board and it operates under the test program.

CN2; VERSION SELECT jumper
(AE-06 board number is 1-620-929-12 or later)
Perform setting according to the version of the software in the ROM (ICF4) on IF-139 board.
Open CN2 for IF1390127 or later, and short it for IF1390126 or earlier.

## 2-5-8. VE-12 Board




*: These switches function only when TEST switch S3/IF-139 is ON. The standard setting position for these switches is OFF.

***: These switches function only when PR CONT (see Note) has been set to OFF on the SYSTEM SETUP sub menu.

**Note:** PR CONT= Processor control mode

*** S1-1: MAPPING OFF switch**

This switch is for checking the source mapping circuit. There is no source mapping of the video data when S1-1 is ON. When S1-1 is set to ON, DE-MAPPING OFF switch S1-1/VN-01 should also be set to ON.

*** S1-2: SHUFFLING OFF switch**

This switch is for checking the video shuffling circuit. There is no intraline shuffling of the video data when S1-2 is ON. When S1-2 is set to ON, DE-SHUFFLING OFF switch S1-1/FM-09A/B should also be set to ON.

*** S1-3: BYPASS-3 switch**

*** S1-4: BYPASS-4 switch**

*** S1-5: BYPASS-5 switch**

These switches select the bypass mode.

The table below shows the relationship between the switch settings and the selected modes. The switch settings in the table must be changed with each mode.

For details on the bypass mode, refer to the section 3 "TEST MODE".

| S1-3 | S1-4 | S1-5 | BYPASS MODE | OTHER SWITCH SETTINGS |
|---|---|---|---|---|
| OFF | OFF | OFF | BYPASS-2 (IE→SY) | S3/IF-139; ON<br>S1-4/SY-70A, B; ON |
| ON | OFF | OFF | BYPASS-3 (IE→CI) | S3/IF-139; ON<br>S101-3/CI-01; ON |
| X | ON | OFF | BYPASS-4 (VE→FM) | S3/IF-139; ON<br>S1-2/FM-09A, B; ON<br>S6-8/TG-28; ON |
| X | X | ON | BYPASS-5 (VE→VN) | S3/IF-139; ON<br>S1-3/VN-01; ON<br>S6-8/TG-28; ON |

X: This switch setting is not related.

**S1-6, 7, 8:** Not used.

***** S2: VIDEO INPUT DIG/ANA select switch**

This switch selects the video input signals.

Its settings are valid only when PR CONT (processor control mode) is OFF. When PR CONT is ON, the video input signal is selected on the VIDEO SETUP sub menu.

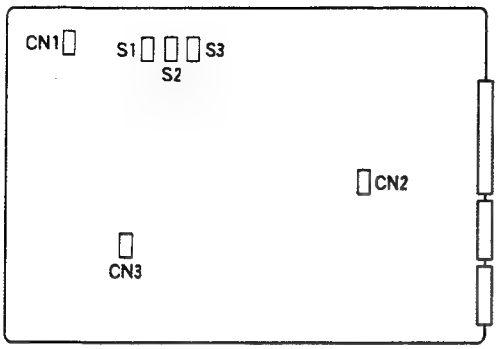
**DIG:** The digital video signal from the video digital input (DSUB) connector is selected as the input signal.

**ANA:** The analog video signal from the video analog input-1 (BNC) or input-2 (multi) connector is selected as the input signal. The signal format (R/G/B or Y/R-Y/B-Y) and input connector (BNC or multi) are selected by S4 and S5 on the IG-13 board.

**CN1: UPI TEST jumper**

This is the UPI test jumper. Normally, it is kept open for use. When it is shorted, UPI suspends communication with the IF-139 board and it operates under the test program.

## 2-5-9. IE-17 Board




**S1: B/D-CH DELAY switch**

This switch adjusts the delay in the B/D channel with respect to the A/C channel. Its settings should not be changed. The settings made when the unit was shipped are given below.

Board Parts No. Suffix-11 1; ON 0; OFF

| S1 | 8 (MSB) | 7 | 6 | 5 | 4 | 3 | 2 | 1 (LSB) |
|---|---|---|---|---|---|---|---|---|
| SETTING | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

Board Parts No. Suffix-12 1; ON 0; OFF

| S1 | 8 (MSB) | 7 | 6 | 5 | 4 | 3 | 2 | 1 (LSB) |
|---|---|---|---|---|---|---|---|---|
| SETTING | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

**S2: EE DELAY switch (for 525/60 system)**

**S3: EE DELAY switch (for 625/50 system)**

These switches adjust the EE and playback data phases. Their settings should not be changed. The settings made when the unit was shipped are given below.

Board Parts No. Suffix-11 1; ON 0; OFF

| | 8 (MSB) | 7 | 6 | 5 | 4 | 3 | 2 | 1 (LSB) |
|---|---|---|---|---|---|---|---|---|
| S2 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| S3 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

Board Parts No. Suffix-12 1; ON 0; OFF

| | 8 (MSB) | 7 | 6 | 5 | 4 | 3 | 2 | 1 (LSB) |
|---|---|---|---|---|---|---|---|---|
| S2 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| S3 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

**CN1: SCRAMBLE INHIBIT jumper**

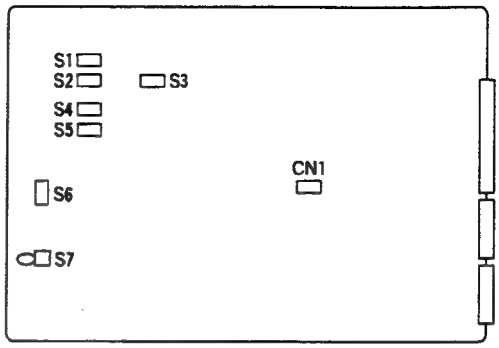
Normally, this is kept open. When CN1 is shorted, the recorded data are not scrambled. When it is shorted, DE-SCRAMBLE INHIBIT jumper CN8/SY-70A/B should also be shorted.

**CN2: Forcible REC jumper**

This is normally kept open. When CN2 has been shorted, data are also output to the edit gap section.

**CN3:** Always open.

## 2-5-10. TG-28 Board




**S1: ADVANCE AUDIO DELAY adjustment switch (625/50)**

**S2: ADVANCE AUDIO DELAY adjustment switch (525/60)**

These switches adjust the advance audio delay. Their settings should not be changed. The settings made when the unit was shipped are S1=4 and S2=6.

**S3: SPOT ERASE FADE TIME setting switch**

This switch sets the fade-out time during audio spot erasing. Its setting should not be changed. The setting made when the unit was shipped is S3=2.

**S4: CONFI AUDIO DELAY adjustment switch (625/50)**

**S5: CONFI AUDIO DELAY adjustment switch (525/60)**

These switches adjust the CONFI audio delay. Their settings should not be changed. The settings made when the unit was shipped are S4=3 and S5=E.

**S6-1 to 7: TEST switches**

These switches are for testing the TG-28 board as a discrete unit. Normally, all the switches are set to OFF.

**S6-8: TEST 8 switch**

This switch is valid when TEST switch S3/IF-139 is ON or when UPI TEST jumper CN1/TG-28 is shorted. Normally, S6-8 is set to OFF. It is set to ON in the bypass 4 or bypass 5 mode. At this time, the sync phase and system phase controls on the VIDEO SETUP sub menu are invalidated.

(2-5-10. TG-28 Board)

**S7: REFERENCE INPUT DIG/ANA select switch**

This switch selects the reference sync signal for servo lock. It is valid only when the PR CONT (processor control mode)/SYSTEM SETUP sub menu is OFF and when the EXT mode(*1) has been selected on the SERVO SETUP sub menu.

When PR CONT is ON, the servo reference signal is selected on the SERVO SETUP sub menu.

DIG: The digital reference video input is selected as the servo reference signal.

ANA: The analog reference video input is selected as the servo reference signal.

*1: Depending on the SERVO SETUP sub menu setting, the servo reference signal is as below.

INPUT: In this case, the S7 setting is invalid, and the video input signal selected by VIDEO INPUT DIG/ANA select switch S2/VE-12 board is selected as the reference signal.

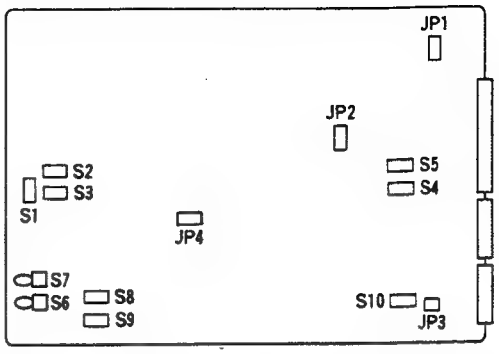
EXT: The S7 setting is valid.

AUTO: In this case, the INPUT mode is automatically selected when the REC/EDIT mode functions as the equipment mode; the EXT mode is automatically selected when it is any other mode.

**CN1: UPI TEST jumper**

This is the UPI test jumper. Normally, it is kept open for use. When it is shorted, UPI suspends communication with the IF-139 board and it operates under the test program.

## 2-5-11. AN-01 Board




*: These switches function only when TEST switch S3/IF-139 is ON. The standard setting position for these switches is OFF.

***: These switches function only when PR CONT (see Note) has been set to OFF on the SYSTEM SETUP sub menu.

Note: PR CONT: Processor control mode

*** S1-1: CONCEALMENT OFF switch**

This switch is for checking the audio error concealment circuit.

There is no error concealment of the audio data when S1-1 is ON.

*** S1-2: MUTE INHIBIT switch**

This switch forcibly releases the audio output muting.

The audio output will be muted when errors in the audio data which can be concealed during the concealment process are generated continuously. However, this muting is forcibly released when S1-2 is set ON. It will not be released when the PLL circuit on the TG-28 board is not locked and when the audio output is muted by the MUTE command sent from the IF-139 board.

*** S1-3: BYPASS: DIGITAL AUDIO BYPASS switch**

This switch selects the audio signal system bypass mode between the AU-86 and AN-01 boards.

Setting is made to the bypass mode when S1-3 is ON.

For details on the bypass mode, refer to the section 3 "TEST MODE".

**S1-4 to 8:** Always set to OFF

(2-5-11. AN-01 Board)

**S2: MUTING TIME switch**

This switch sets the minimum muting time for the audio output. Every time the S2 setting is changed by one step, the muting time changes by 4096 audio samples (85.3 msec). S2 is set to "7" (approximately equivalent to 683 msec) when the unit is shipped.

**S3: MUTING DELAY setting switch**

This switch sets the amount of audio data delay in the muting circuit. Its setting should not be changed.
S3 is set to "B" (192 audio samples) when the unit is shipped.

**S4 (LSB), S5 (MSB): DIGITAL AUDIO OUTPUT DELAY setting switches**

These switches set the amount of delay in the delay circuit provided in the digital signal system in order to align the phases of the analog audio and digital audio outputs. S4 is set to "1" and S5 is set to "2" when the unit is shipped. The amount of delay applying at this time is 33 audio samples.

***** S6 (LSB), S7 (MSB): ADVANCE AUDIO DELAY adjustment switches**

These switches adjust the phase of the advance audio output. This phase can be advanced by a maximum of 50 audio samples with respect to the reference phase.
These switches are valid only when PR CONT (processor control mode) is OFF. When PR CONT is ON, adjustment is made on the DIGITAL AUDIO SETUP sub menu.
S6 is set to "7" and S7 is set to "C" when the unit is shipped. The amount of advance applying at this time is 0 audio samples.
Every time the switch setting is changed by one step, the amount of advance changes by 1 audio sample.

**S8 (LSB), S9 (MSB): ADVANCE RETURN DELAY setting switches**

These switches set the amount of delay in the advance return signal. Their setting should be not changed.
S8 is set to "F" and S9 is set to "F" when the unit is shipped.

**S10:** Not used.

**JP1: UPI TEST jumper**

This is the UPI test jumper. Normally, it is kept open for use. When it is shorted, UPI suspends communication with the IF-139 board and it operates under the test program.

**JP2: ADVANCE AUDIO MONITOR jumper**

Normally, the CONFI head playback signals are output to the analog audio and audio monitor output connectors. However, when JP2 is shorted, the ADVANCE head playback signals are output to these connectors. This jumper is normally kept open for use.

**JP3:** Always open.

**JP4: AUDIO LEVEL +6 dB/+12 dB selection jumper**

This jumper selects a variable range of the audio digital output level. This jumper is used in combinations with the CN3 shorted socket on the AU-86 board. The table below shows the relation between the jumper and the selectable range.

| Board (last two digits) | *1 VERSION I | *2 VERSION II | Variable Range |
|---|---|---|---|
| AN -01 (-12) | JP4 SHORT | | +6dB ~ -∞ |
| AN -86 (-13) | CN3 SHORT | | |
| AN -01 (-12) | | JP4 OPEN | +12dB ~ -∞ |
| AN -86 (-13) | | CN3 OPEN | |
| AN -01 (-11) | | | +6dB ~ -∞ |
| AN -86 (-13) | | CN3 OPEN | |
| AN -01 (-12) | | JP4 OPEN | +6dB ~ -∞ |
| AN -86 (-11,12) | | | |

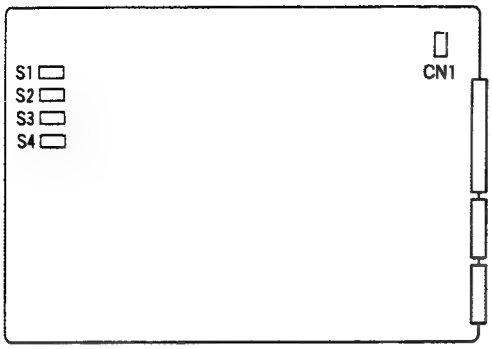
*1: Software version of ROM (ICF4) on the IF-139 board is earlier than IF1390134.

*2: Software version of ROM (ICF4) on the IF-139 board is IF1390135 or later.

**Note 1:** If JP4 on the AN-01 board with numbers ending with 12 and CN3 on the AU-86 board with numbers ending with 13 are shorted in version II, the audio level control does not operate properly. Be sure to open JP4/AN-01 and CN3/AU-86.

**Note 2:** JP4 and CN3 are omitted on the AN-01 boards with numbers ending with 11 or lower and the AU-86 boards with numbers ending with 12 or lower respectively.

## 2-5-12. AP-14 Board



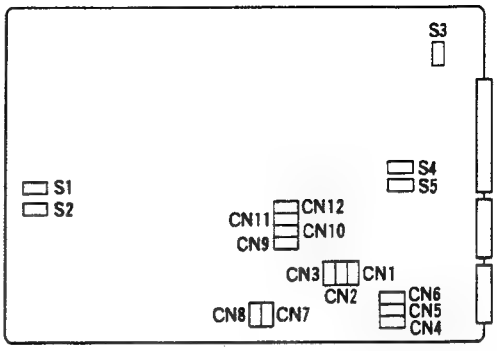

**: These switches function only when UPI test jumper CN1 or JP1/AP-14 is shorted. The standard setting position for these switches is OFF.

**** S1: ADVANCE RETURN DELAY adjustment switch (MSB)**
**** S2: ADVANCE RETURN DELAY adjustment switch (LSB)**
These switches adjust the amount of delay in the advance return signals. For normal use, the delay information is supplied from UPI. S1 is set to "2" and S2 is set to "0" when the unit is shipped.

**** S3: PB AUDIO DELAY adjustment switch (MSB)**
**** S4: PB AUDIO DELAY adjustment switch (LSB)**
These switches adjust the amount of delay in the audio playback signals. They are valid when the UPI TEST jumper CN1/AP-14 has been shorted and also when the DVPC-1000 is operating as a discrete unit.
For normal use, the delay is adjusted on the DIGITAL AUDIO OUTPUT SETUP sub menu.
With the 525/60 system, S3 is set to "7" and S4 to "5" and with the 625/50 system, S3 is set to "6" and S4 to "6" when the unit is shipped.

**CN1 (JP1): UPI TEST jumper**
This is the UPI test jumper. Normally, it is kept open for use. When it is shorted, UPI suspends communication with the IF-139 board and it operates under the test program.

## 2-5-13. VN-01 Board




*: These switches function only when TEST switch S3/IF-139 is ON. The standard setting position for these switches is OFF.

*** S1-1: DE-MAPPING OFF switch**
This switch is for checking the video source mapping circuit. There is no source mapping of the video data when S1-1 is ON. When S1-1 is set to ON, MAPPING OFF switch S1-1/VE-12 should also be set to ON.

*** S1-2: CONCEALMENT OFF switch**
This switch is for checking the error concealment circuit. When S1-2 is ON, the outer error flag which is output from the FM-09 board is forcibly set low (no error). Consequently, there is no error concealment even when outer residual errors are present in the video data and the error data are output in their original form.

*** S1-3: BYPASS-5 switch**
Bypass 5 is the bypass mode between the VE-12 and VN-01 boards. Setting is made to this mode when switches S3/IF-139, S1-3/VN-01, S1-5/VE-12 and S6-8/TG-28 are ON.
For details on the bypass mode, refer to the section 3 "TEST MODE".

**S1-4, 5:** Always set to OFF.

*** S1-6: PINK DISPLAY MODE STATUS/4SPL select switch**
*** S1-7: PINK DISPLAY ON/OFF switch**
Refer to the description of IDEAL DIR DISPLAY switch S2-6/VN-01.

**S1-8:** Not used.

(2-5-13. VN-01 Board)

*** S2-1: ERROR ADD TEST switch**

When S2-1 is ON, the errors corresponding to the CN1 through CN8 settings are added to the video data. These data are provided by inverting the Y data MSB. Consequently, the C data section cannot be checked by this switch. The error flag is also inverted at the same time as the errors are added and so ERROR CONCEALMENT OFF switch S1-2/VN-01 must be set to ON in order to generate the error flag that corresponds with the error pattern.

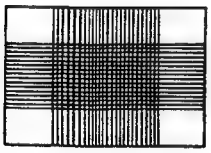
These switches, jumpers and CONCEALMENT ALGORITHM CONT. switches S2-2, 3, 4, 5/VN-01 can be used in combination to check the concealment circuit.

The errors below are added by the CN1 through CN8 settings.

| CN7 | CN8 | MODE |
|---|---|---|
| OPEN | OPEN | No error added |
| OPEN | SHORT | ERROR H (ERH) |
| SHORT | OPEN | ERROR V (ERV) |
| SHORT | SHORT | ERROR H+V (ERH+ERV) |

**ERH + ERV MODE: (CN7: shorted, CN8: shorted)**

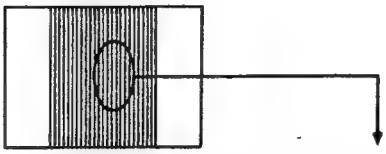
This mode combines the above-mentioned ERH and ERV modes. The errors appear at the position on the picture monitor which is shown in the figure below. The error pattern in this mode is selected by CN1, 2 and 3 in the horizontal direction and by CN4, 5 and 6 in the vertical direction.



**ERH MODE: (CN7: open, CN8: shorted)**

In this mode, the errors appear at the position on the picture monitor which is shown in the figure below. The error pattern is selected by CN1, CN2 and CN3.

<PICTURE MONITOR>



| CN1 | CN2 | CN3 | ERROR PATTERN |
|---|---|---|---|
| S | O | O | PATTERN 1 ○●○●○●○●○<br>○●○●○●○●○<br>○●○●○●○●○ |
| O | S | O | PATTERN 2 ○●●○●●○●●<br>○●●○●●○●●<br>○●●○●●○●● |
| O | O | S | PATTERN 3 ○●●●○●●●○<br>○●●●○●●●○<br>○●●●○●●●○ |

O; OPEN ○; No error

S; SHORT ●; Error data

**Pattern 1:** The error is added at every other sample. This errors concealed by 2-point interpolation.

**Pattern 2:** The error is added for two samples in succession. This error cannot be concealed by 2-point interpolation but is concealed completely by simple replacement.

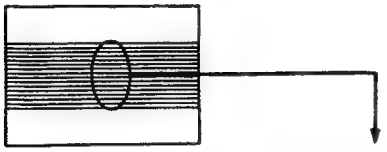
**Pattern 3:** The error is added for three samples in succession. When simple replacement is used to conceal this error, the error data in the center sample will remain unconcealed but it can be concealed completely by recursive replacement.

(2-5-13. VN-01 Board)

**ERV MODE: (CN7: shorted, CN8: open)**

In this mode, the errors appear at the position on the picture monitor which is shown in the figure below. The error pattern is selected by CN4, CN5 and CN6.

<PICTURE MONITOR>



| CN4 | CN5 | CN6 | ERROR PATTERN |
|---|---|---|---|
| S | O | O | PATTERN 1 ○○○○○○○○○ ●●●●●●●●● ○○○○○○○○○ ●●●●●●●●● ○○○○○○○○○ |
| O | S | O | PATTERN 2 ○○○○○○○○○ ●●●●●●●●● ●●●●●●●●● ○○○○○○○○○ ●●●●●●●●● ●●●●●●●●● ○○○○○○○○○ |
| O | O | S | PATTERN 3 ○○○○○○○○○ ●●●●●●●●● ●●●●●●●●● ●●●●●●●●● ○○○○○○○○○ ●●●●●●●●● ●●●●●●●●● ●●●●●●●●● ○○○○○○○○○ |

O; OPEN
S; SHORT

○; No error
●; Error data

**Pattern 1:** The error is added every other line. This error is concealed by 2-point interpolation.

**Pattern 2:** The error is added on two lines in succession. This error cannot be concealed by 2-point interpolation but is concealed completely by simple replacement.

**Pattern 3:** The error is added on three lines in succession. When simple replacement is used to conceal this error, the error data on the center line will remain unconcealed but it can be concealed completely by recursive replacement.

*** S2-2, 3, 4, 5: CONCEALMENT ALGORITHM CONTROL switches**

These switches are used in combination with ERROR ADD TEST switch S2-1/VN-01 to check the error concealment circuit. Errors are concealed using the methods below.

**1. 2-point interpolation**

The error data are replaced by the average value of two sample data in the direction (H, V, D+ or D-) with the strongest correlation (ideal direction).

**2. Simple replacement**

When errors cannot be concealed by 2-point interpolation, the error data are replaced by 8-proximity data.

**3. Recursive replacement**

When errors cannot be concealed by 2-point interpolation or by simple replacement, the data are replaced by data other than 8-proximity data. In principle, replacement using the same data may be performed for a maximum of 6 times.

**4. Data through**

When errors cannot be concealed by methods 1 to 3, the error data are not written into the frame memory and the data of 1 frame before are output in their original form.

Errors can be concealed using the S2-2 to S2-5 settings only by the methods below.

| S2-2 | S2-3 | S2-4 | S2-5 | CONCEALMENT MODE |
|---|---|---|---|---|
| ON | X | X | X | No concealment. *1, *2 |
| OFF | ON | X | X | Concealment by 2-point interpolation only. *2 |
| OFF | OFF | ON | X | Concealment by 2-point interpolation or simple replacement only. |
| OFF | OFF | OFF | ON | Concealment by 2-point interpolation, simple replacement or recursive replacement. |

X: This switch setting is not related.

*1: The same operation is performed as when CONCEALMENT OFF switch S1-2/VN-01 is set to ON. However, whereas the error flag sent from the FM-09 board is forcibly set low (no error) when S1-2 is set ON, the error flag remains unchanged in this case and the concealment circuit stops operating.

*2: The VID ERROR CCEAL indicator D1 (red) at the front of the VN-01 board lights.

(2-5-13. VN-01 Board)

*** S2-6: IDEAL DIR DISPLAY switch**

This switch is used together with S1-6/7 and S2-7/8 for conducting a visual check of the ideal direction decision. When S1-7 and S2-6 are ON, the pixels appear on the picture monitor in pink in the ideal direction which is based on the direction specified by S2-7 and S2-8.

| S1-6 | S1-7 | S2-6 | S2-7 | S2-8 | DISPLAY DIRECTION |
|---|---|---|---|---|---|
| *1 | ON | ON | OFF | OFF | H (→) |
| | | | OFF | ON | V (↓) |
| | | | ON | OFF | D− (↘) |
| | | | OFF | OFF | D+ (↗) |

*1: When S1-6 is ON, all the samples appear in pink in the ideal direction which is based on the direction specified by S2-7 and S2-8. When it is OFF, every fourth sample appears in pink.

**S2-7: DISPLAY CONT1 switch**
**S2-8: DISPLAY CONT2 switch**

Refer to the description of IDEAL DIR DISPLAY switch S2-6/VN-01.

**S3:** Not used.

**S4: DIGITAL DELAY adjustment switch (LSB)**
**S5: DIGITAL DELAY adjustment switch (MSB)**

These switches set the digital delay for adjusting the phases of the analog video and digital video outputs. Their settings should be not changed. S4 is set to "6" (or "7") and S5 is set to "1" when the unit is shipped.

**CN1, 2, 3: ERROR PATTERN (ERH) selector jumpers**
**CN4, 5, 6: ERROR PATTERN (ERV) selector jumpers**
**CN7, 8: ERROR PATTERN MODE selector jumpers**

Refer to the description of ERROR ADD TEST switch S2-1/VN-01.

**CN9, 10, 11, 12: CONCEALMENT RATE DISPLAY MODE select jumpers**

These jumpers set the lighting conditions for the VIDEO ERROR CONCEALMENT indicator (D1) on the front of the VN-01 board.

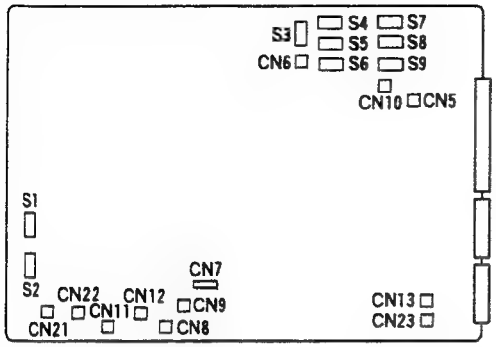
D1 lights when there are more data in 1 frame than the set number of data which cannot be concealed (give-up data). These conditions are shown below when the jumpers are shorted. CN12 is shorted when the unit is shipped.

| JUMPER PLUG CN9/10/11/12 | D1 lighting condition (give-up rate) |
|---|---|
| CN9; SHORT | ≧32 SAMPLE/FRAME |
| CN10; SHORT | ≧64 SAMPLE/FRAME |
| CN11; SHORT | ≧128 SAMPLE/FRAME |
| CN12; SHORT | ≧256 SAMPLE/FRAME |

**CN14: UPI TEST jumper**

This is the UPI test jumper. Normally, it is kept open for use. When it is shorted, UPI suspends communication with the IF-139 board and it operates under the test program.

## 2-5-14. FM-09A/B Boards




*: These switches function only when TEST switch S3/1F-139 is ON. The standard setting position for these switches is OFF.

**: These switches function only when test jumper CN6/FM-09A/B are shorted. The standard setting position for these switches is OFF.

*** S1-1: DE-SHUFFLING THROUGH switch**

This switch is for checking the video de-shuffling circuit. There is no video data intraline de-shuffling when S1-1 is ON. When S1-1 has been set ON, SHUFFLING OFF switch S1-2/VE-12 should also be set to ON.

*** S1-2: BYPASS-4 switch**

Bypass-4 is the bypass mode between the VE-12 and FM-09A/B boards. Setting is made to this mode when switches S3/1F-139, S1-2/FM-09A/B, S1-4/VE-12 and S6-8/TG-28 are ON and when switch S1-5/VE-12 is OFF. For details on the bypass mode, refer to the section 3 "TEST MODE".

*** S1-3: TEMPORARY CONCEALMENT OFF switch**

This switch sets the concealment in the time base direction to ON and OFF. Normally, the inner error data are not written into the 3-field memory and the data of 1 frame before are read out in their original form. However, when S1-3 is ON, the inner error data are written into the 3-field memory.

**S1-4:** Not used.

*** S1-5: VIDEO OUTER CORRECTION OFF switch**

This switch is for checking the video outer decoder. Errors are not corrected by the outer decoder when S1-5 is ON. At this time, all the inner error data are outer residual errors and they are sent to the error concealment circuit on the VN-01 board.

**S1-6, 7, 8:** Not used.

**S2-1 to 7:** Always set to OFF.

**S2-8: INHIBIT CHANNEL select switch**

Refer to OUTPUT DATA INHIBIT switch S3-7/FM-09A/B.

**S3-1:** Always set to OFF.

**** S3-2: FRAME MEMORY test switch**

This switch is for read/write testing of the frame memory on the FM-09A/B boards. If TP64/FM-09A/B (A/C-CH) or TP74/FM-09A/B (B/D-CH) is grounded momentarily when S3-2 is ON, the input data are written once only into all the addresses ($0000_H$ to $FFFF_H$) of the 3-field memory and then the read mode is established.

The S/P/S converter and DRAM can be checked by supplying the stair-step signal (see Note 1) from the test signal generator on the SY-70A/B boards to the FM-09A/B boards. For details, refer to the section 3 "TEST MODE".

**(Note 1):** When the CI-01 board with the board number suffix of -11 is used, the test signal output from the SY-70A/B board cannot be supplied to the FM-09A/B board.

**** S3-3:** Always set to OFF.

**** S3-4: 1H DE-SHUFFLE MEMORY test switch**

This switch is for read/write testing of the de-shuffle memory. When the stair-step signal from the test signal generator on the SY-70A/B boards is input to the 1H de-shuffle memory with S3-4 at ON, these waves will be output to the output side in their original form and this will enable the de-shuffle memory to be tested. For details, refer to the section 3 "TEST MODE".

(2-5-14. FM-09A/B Boards)

** S3-5, 6: Always set to OFF.

** S3-7: OUTPUT DATA INHIBIT switch
This switch limits the data output from the FM-09A/B boards to a specific channel. It is used to verify in which channel the error has arisen.
When S3-7 is ON, the data from the FM-09A/B boards are output as follows, depending on the setting of TEST MODE select switch S2-8/FM-09A/B.
**When S2-8 is ON:** Only A (C) channel data are output.
**When S2-8 is OFF:** Only B (D) channel data are output.

The images on one specific channel only can be viewed by removing either the FM-09A or FM-09B board and proceeding to operate with only one board. However, when the board is removed with the DVR-1000 connected, the "BOARD DISCONNECT ERROR OPERATION STOP" error message will appear. But functions can be operated.

** S3-8: Always set to OFF.

** S4 to 9: Not used.

CN5: UPI TEST jumper
This is the UPI test jumper. Normally, it is kept open for use. When it is shorted, UPI suspends communication with the IF-139 board and it operates under the test program.

CN6: TEST jumper
This is the jumper for testing the FM-09A/B boards. Normally, it is kept open for use. When it is shorted, the setting of the DIP switch S3 for testing is made valid.

CN7, 8, 9: Always open.

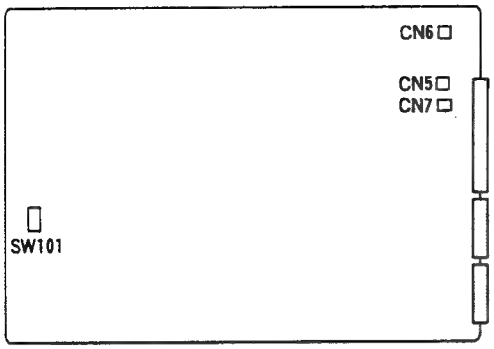
CN10: HEAD DE-INTERLEAVE FLAG TEST jumper
This jumper is for head de-interleave flag memory testing.
Normally, it is kept open for use. When it is shorted, the MSB of the various channel data are input to the flag memory. The operation of the flag memory can be checked by comparing the flag memory output data and video data MSB. In actual fact, these data are supplied to CH-1 and CH-2 of the oscilloscope, the data of one channel are inverted and observed in the ADD mode. The flag memory is operating properly if the trace on the oscilloscope screen appears as a straight line (some fuzz may be visible).
Observation points:
Y; Pins 19 of ICA31 and 15 of ICC31 (FLAG)
C; Pins 19 of ICB31 and 12 of ICC31 (FLAG)

CN11, 21: Always open.

CN12: A/C-CH FRAME MEMORY READ INHIBIT jumper
CN22: B/D-CH FRAME MEMORY READ INHIBIT jumper
These jumpers are normally kept open for use. When they are shorted, the corresponding channel data are not read from the frame memory and all the input data of the 1H de-shuffle memory are set high.

CN13: BYPASS-4 A/C-CH INPUT DATA INHIBIT jumper
CN23: BYPASS-4 B/D-CH INPUT DATA INHIBIT jumper
These jumpers are normally kept open for use. When they are shorted in the bypass 4 mode, the corresponding channel data are not input into the de-shuffle memory and the data of all-high signals are input instead.

## 2-5-15. CI-01 Board




*: These switches function only when TEST switch S3/IF-139 is ON. The standard setting position for these switches is OFF.

*** SW101-1: INNER CORRECTION OFF switch**

This switch is for checking the inner decoder.
When SW101-1 is ON, errors cannot be corrected by the inner decoder.

*** SW101-2: AUDIO OUTER CORRECTION OFF switch**

This switch is for checking the audio outer decoder.
When SW101-2 is ON, errors cannot be corrected by the audio outer decoder.

*** SW101-3: BYPASS-3 switch**

Bypass-3 is the bypass mode between the IE-17 and CI-01 boards. Setting is made to this mode when switches S1-4/VE-12 and S1-5/VE-12 are OFF and when switches S3/IF-139, S1-3/VE-12 and SW101-3 are ON.
For details on the bypass mode, refer to the section 3 "TEST MODE".

*** SW101-4: INTER CHANGE ON switch**

When SI01-4 is ON, the channel exchanger is activated even in the normal playback mode.
Normally, this switch is used at OFF. The channel exchanger will now be activated only during stunt playback.

*** SW101-5: INNER DECODER BYPASS TEST switch**

This switch is valid when the CI-01 board has a board number suffix of -12 and higher.
Set this switch to ON when supplying the stair-step signal, which has been output from the test signal generator on the SY-70A/B boards, to the FM-09A/B boards.
The CI-01 board input data bypass the inner decoder and are output in their original form to the FM-09A/B boards.

**SW101-6: Swap test direction switch**

See the description for swap test jumper CN7/CI-01.

**SW101-7 and 8: Not used.**

**CN5: BOARD DIRECTION selection jumper**

Set it as follows according to the board number of the CI-01.

| Last digit of board number | CN5 |
|---|---|
| -11 | OPEN |
| -12 or higher | SHORT |

**CN6: UPI TEST**

This is the UPI test jumper. Normally, it is kept open for use. When it is shorted, UPI suspends communication with the IF-139 board and it operates under the test program.

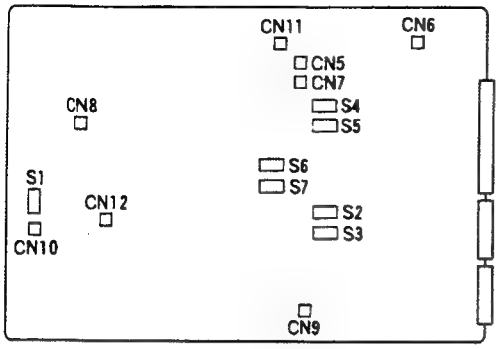
***CN7: SWAP TEST jumper**

(only for CI-01 boards having a board number with -12 or higher for its last digits)
It is a jumper for the swap test in the CI-01 board, and is used in combination with SW101-6. Usually, it is used in its open state. However, when CN7 is shorted, same data are outputted to A and B channels (or C and D channels) of the video according to the setting of SW101-6. Use of this function enables the 3-field memory and 1H deshuffle memory to be debugged.
See "3-5-5 Swap Test Function" for the testing method.
The test function is contained in the channel exchanger on the CI-01 board, and also performs the changing-over of SYNC data as well as video data.

| CN7 | SW101-6 | MODE |
|---|---|---|
| OPEN | * | TEST OFF |
| SHORT | OFF | A→A, B→B ・ C→C, D→D |
| SHORT | ON | A→B, B→A ・ C→D, D→C |

*; Don't Care

## 2-5-16. SY-70A/B Boards




*: These switches function only when TEST switch S3/IF-139 is ON. The standard setting position for these switches is OFF.

*** S1-1: A/C-CH DATA INHIBIT switch**
*** S1-2: B/D-CH DATA INHIBIT switch**
When these switches have been set to ON, all the TBC output data in the SY-70 board are set high.

*** S1-3: BYPASS-1: SERIAL EE switch**
The serial EE mode is established when S1-3 is ON.
In this mode, the serial recording data, which have been delayed by an amount equivalent to the difference between the phases of the REC and CONFI heads, are supplied to the SY-70A/B boards. When two SY-70 boards are being used, the SY-70B board (slot #17) switch takes precedence.

*** S1-4: BYPASS-2: PARALLEL EE switch**
Bypass-2 is the parallel data bypass mode between the IE-17 and SY-70A/B boards.
The bypass-2 mode is established when S1-4 is ON and S2-3, 2-4 and S2-5 on the VE-12 are OFF. For details on the bypass mode, refer to the section 3 "TEST MODE".

**S1-5: SWAP1 test switch**
**S1-6: SWAP1 TEST DIRECTION switch**
**S1-7: SWAP2 test switch**
Refer to the description of swap test jumper JP10/ SY-70A/B.

**S1-8: SWAP2 TEST DIRECTION/ERROR ADD CH selector switch**
This switch designates the direction of the data in the swap 2 test mode and the channel to which the error is to be added in the error add test. For details, refer to the description of CN9 and CN10.

**S2: ERROR ADD SIZE (INNER) switch (LSB)**
**S3: ERROR ADD SIZE (INNER) switch (MSB)**
**S4: ERROR ADD POSITION (SYNC) switch (LSB)**
**S5: ERROR ADD POSITION (SYNC) switch (MSB)**
**S6: ERROR ADD SIZE (SAMPLE) switch**
**S7: ERROR ADD TEST MODE selector switch**
Refer to the description of ERROR ADD TEST jumper CN9/SY-70A/B.

**CN5: TBC MEMORY TEST1 jumper**
This jumper is for checking the TBC read address.
Normally, it is kept open for use. When it is shorted, data are not written into the TBC.
At this time, the read addresses are input at all times into the ICC15-C20 and ICH15-H20 address input pins of the TBC memory.

**CN6: UPI TEST jumper**
This is the UPI test jumper. Normally, it is kept open for use. When it is shorted, UPI suspends communication with the IF-139 board and it operates under the test program.

**CN7: TBC MEMORY TEST2 jumper**
This switch is for checking the TBC write address.
Normally, it is kept open for use. When it is shorted, data are not read from the TBC.
At this time, the write addresses are input at all times into the ICC15-C20 and ICH15-H20 address input pins of the TBC memory.

**CN8: DE-SCRAMBLE INHIBIT jumper**
This is normally kept open for use. De-scrambling is not performed when it is shorted. Scramble inhibit jumper CN1/IE-17 should also be shorted when CN8 is shorted.
These jumper plugs should also be shorted when the FM-09 A/B boards are checked at the test signal output of the SY-70 A/B boards.

(2-5-16. SY-70A/B Boards)

**CN9: ERROR ADD TEST jumper**

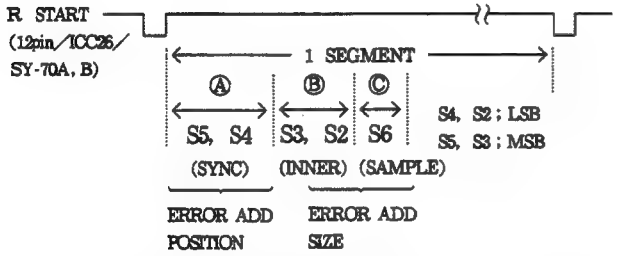
This is used in combination with switches S2 through S7 and S1-8 to check the error correction capacity of the inner and outer decoders. Normally it is kept open for use. When it is shorted, the error is added to the desired position within the segment.

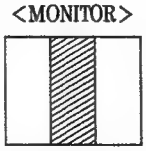
The channel in which the error is to be added is designated by S1-8, and the position and size are designated by S2 through S7.

When S1-8 is OFF, the error is added to channel A (C); when it is ON, it is added to channel B (D).

S4 (LSB) and S5 (MSB) designate the position where the error is to be added in units of 1 sync or 2 sync blocks (See Note). S2 (LSB) and S3 (MSB) designated the size of the error in inner block units whereas S6 designates it in sample units.

The figure below shows the relationship between the switch settings and the positions and sizes of the error which is to be added.



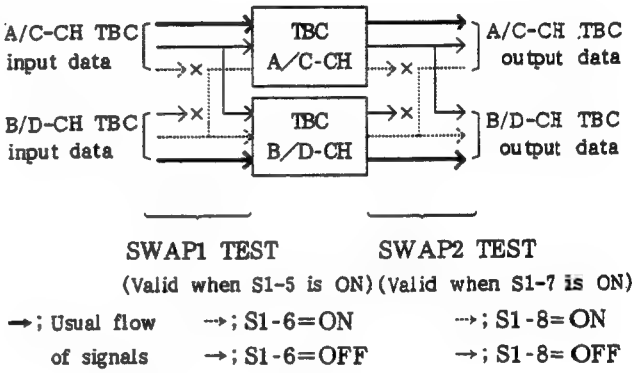

| MODE | S7 (Note) | AREA WHERE ERROR IS TO BE ADDED | |
|---|---|---|---|
| 0 | 0, 8 | Ⓑ and Ⓒ in above figure | No error in sync, ID area |
| 1 | 1, 9 | Ⓑ only in above figure | |
| 2 | 2, A | Ⓒ only in above figure | |
| 3 | 3, B | Ⓑ and Ⓒ in above figure | Error added to sync, ID area |
| 4 | 4, C | Ⓑ only in above figure | |
| 5 | 5, D | Ⓒ only in above figure | |
| 6 | 6, 7, E, F | 1 sample/inner error is added to all the inner blocks regardless of the S2-S6 settings (except when S4, S5 = $00_H$). The error appears on the picture monitor in the shaded area shown in the figure on the right (when video shuffling is ON). <MONITOR>  | |

(Note): When S7 is 0-7, the error position based on S4 and S5 is designated in 1 sync block units; when S7 is 8-F, it is designated in 2 sync block units.

*** CN10: SWAP TEST ENABLE jumper**

This jumper is for data swap testing in the TBC circuit. Swap test circuits are provided on the SY-70A/B boards in both the TBC input area (SWAP1) and output area (SWAP2). When CN10 is shorted, the settings of SWAP1 TEST switch S1-5/SY-70A/B and SWAP2 TEST switch S1-7/SY-70A/B are made valid. The input/output signals at this time are selected by S1-6 and S1-8. The swap 1 and swap 2 tests can be specified simultaneously.

The figure below shows the flow of the signals in the swap test mode.




**CN11: JUMP TEST ENABLE jumper**

This is the TBC bypass test jumper. Normally it is kept open for use.

When it is shorted, the video data are output in their original form without being written into the TBC. When signals containing jitter such as playback pictures are input, the processor may not function properly.

Therefore, during a jump test, input signals which do not contain jitter such as EE pictures should be supplied.

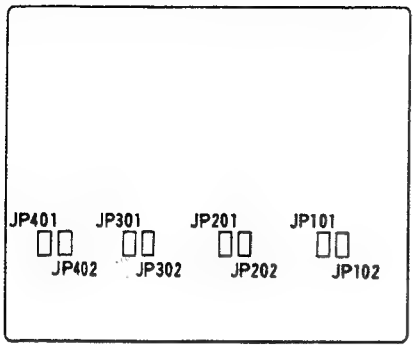
**CN12: TEST SIGNAL OUTPUT jumper**

Normally it is kept open for use. When it is shorted, the stair-step signal from the test signal generator is input to A (C)-CH TBC. The TBC memory can be tested using this test signal. The test signal can also be input to the B (D)-CH TBC by setting SWAP1 TEST switch S1-5/SY-70A/B.

By using this test signal, the 3-field memory and 1H de-shuffle memory on the FM-09 A/B boards can also be checked. But when the CI-01 board with a board number suffix of -11 is used, this function cannot be used. For details, see Section 3 "Test Mode".

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

## 2-5-17. AT-45 Board



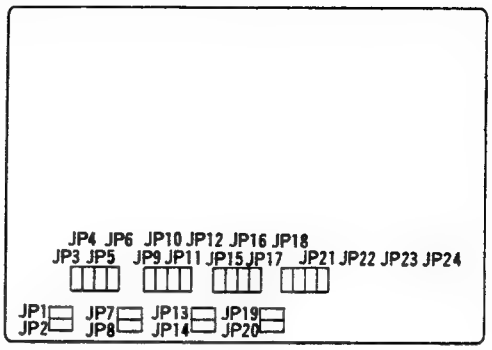

**A, B, C, D, E, F, G, H, I (soldered jumpers):**
**Analog audio output impedances**

These jumpers select the analog audio output impedances.
For details, refer to the section 1-9-4.

**JP101/102: Analog audio output level CH-1**
**JP201/202: Analog audio output level CH-2**
**JP301/302: Analog audio output level CH-3**
**JP401/402: Analog audio output level CH-4**

These jumpers select the analog audio output levels.
For details, refer to the section 1-9-6.

## 2-5-18. IV-14 Board




**JP1/2: Analog audio input impedance CH-4**
**JP7/8: Analog audio input impedance CH-3**
**JP13/14: Analog audio input impedance CH-2**
**JP19/20: Analog audio input impedance CH-1**

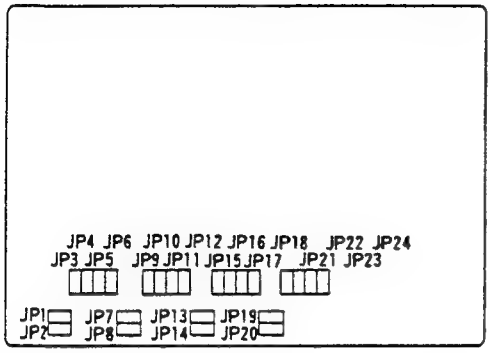
These jumpers select the analog audio input impedances.
For details, refer to the section 1-9-3.

**JP3/4/5/6: Analog audio input level CH-4**
**JP9/10/11/12: Analog audio input level CH-3**
**JP15/16/17/18: Analog audio input level CH-2**
**JP21/22/23/24: Analog audio input level CH-1**

These jumpers select the analog audio input levels.
For detils, refer to the section 1-9-5.

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

**2-5-18. IV-21 Board**

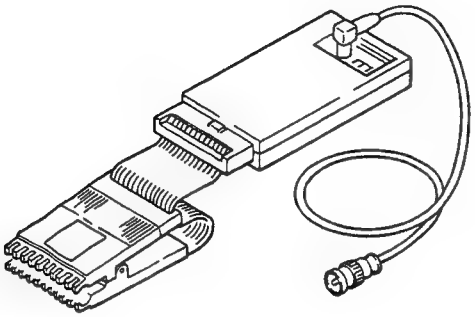



**CN801/802: Analog audio input impedance CH-1**
**CN821/822: Analog audio input impedance CH-2**
**CN841/842: Analog audio input impedance CH-3**
**CN861/862: Analog audio input impedance CH-4**
These jumpers select the analog audio input impedances.
For details, refer to the section 1-9-3.

**CN803/804/805/806: Analog audio input level CH-1**
**CN823/824/825/826: Analog audio input level CH-2**
**CN843/844/845/846: Analog audio input level CH-3**
**CN863/864/865/866: Analog audio input level CH-4**
These jumpers select the analog audio input levels.
For detils, refer to the section 1-9-5.

## 2-6. ROVING DAC

ROVING DAC SONY Parts Number; J-6263-470-A



**Note:** A conversion cable (BNC-UM cable; J-6264-360-A, 1 m) with a mini-RF plug on one end and a BNC plug on the other end is included.

It is used to check and diagnose the digital signal processing circuit. The ROVING DAC is connected with the 8-bit D-type flip flop IC such as LS273/573type (20 pins). It takes out 8-bit parallel data from the digital circuit, converts those data from digital signals to analog signals, and outputs them. The operation of the digital circuit is easily checked and diagnosed by observing those output signals with an oscilloscope.

### 2-6-1. Precautions on Handling

Please pay careful attention to the following points when using the ROVING DAC.

- Make sure to turn off the power of the measured equipment before installing or removing.
- Even though a protection circuit against the inverted insertion is provided, check that pin mark No.1 of the IC before turning the power on. When they are connected properly, the green LED is lit when the power is on.
- Set the mode selector switch S1 located in the ROVING DAC according to the pin assignment and the LSB and MSB assignment of the IC to be observed.
- Avoid using ICs other than those specified. It might cause trouble.
- Do not pull or exert a strong force on the cable between the main body and the IC clip, or the connection cable between the main body and the oscilloscope.

### 2-6-2. Mode Selector Switch S1

Set the mode selector switch S1 located in the ROVING DAC according to the pin assignment and the LSB and MSB assignment of the IC to be observed, as shown below.

| S1−1 | S1−2 | S1−3 | S1−4 | PIN ASSIGNMENT (PIN NO.) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| ON | ON | ON | ON | 16 | 19 | 2 | 5 | 12 | 15 | 6 | 9 |
| OFF | ON | ON | ON | 19 | 16 | 15 | 12 | 9 | 6 | 5 | 2 |
| ON | OFF | ON | ON | 2 | 5 | 6 | 9 | 12 | 15 | 16 | 19 |
| OFF | OFF | ON | ON | 19 | 2 | 16 | 5 | 15 | 6 | 12 | 9 |
| ON | ON | OFF | ON | 12 | 9 | 15 | 6 | 16 | 5 | 19 | 2 |
| OFF | ON | OFF | ON | 2 | 19 | 5 | 16 | 6 | 15 | 9 | 12 |
| ON | ON | ON | OFF | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 |
| OFF | ON | ON | OFF | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |

### 2-6-3. Photo of Waveforms in the Circuit Diagram

The photos of waveforms in the circuit diagram of the DVPC-1000 MAINTENANCE MANUAL VOL-2 are taken by using a ROVING DAC. The photos are taken under the following conditions unless otherwise specified.

Oscilloscope settings

0.2V/div
10μsec/div

Switch and jumper settings (DVPC-1000)

| | | | |
|---|---|---|---|
| IF-139 Board | S3; | TEST ..... | ON |
| CI-01 Board | SW101-1; | INNER CORRECTION OFF ..... | ON |
| FM-09A,B Board | S1-1; | DE-SHUFFLING THROUGH ..... | ON |
| | S1-3; | OUTER CORRECTION OFF ..... | ON |
| | S3-4; | 1H DE-SHUFFLE MEMORY TEST ..... | ON |
| | CN6; | TEST ENABLE ..... | SHORT |
| IE-17 Board | CN1; | SCRAMBLE INHIBIT ... | SHORT |
| PG-13 Board | S3-2; | VIDEO TEST SIGNAL OUTPUT ..... | ON |
| SY-70A,B Board | S1-3; | BYPASS-1 ..... | ON |
| | CN8; | DE-SCRAMBLE INHIBIT ..... | ON |
| VA-45 Board | S1-1; | TEST SIGNAL SELECT . | OFF |
| VE-12 Board | S1-1; | MAPPING OFF ..... | ON |
| | S1-2; | SHUFFLING OFF ..... | ON |
| VN-01 Board | S1-1; | DE-MAPPING OFF ..... | ON |
| | S1-2; | CONCEALMENT OFF .... | ON |

Other switch and jumper settings are the same as in Section 5-5. Settings which require changing are described on each photo.

Replacement of ROM for the testing signal generation-circuit

Replace the IC-B9/C9/D9 on the VA-45 board with the following linearity signal generation ROM. Make sure to turn the power off before replacing. Keep the removed ROM for later use as it is used for the video signal adjustment.

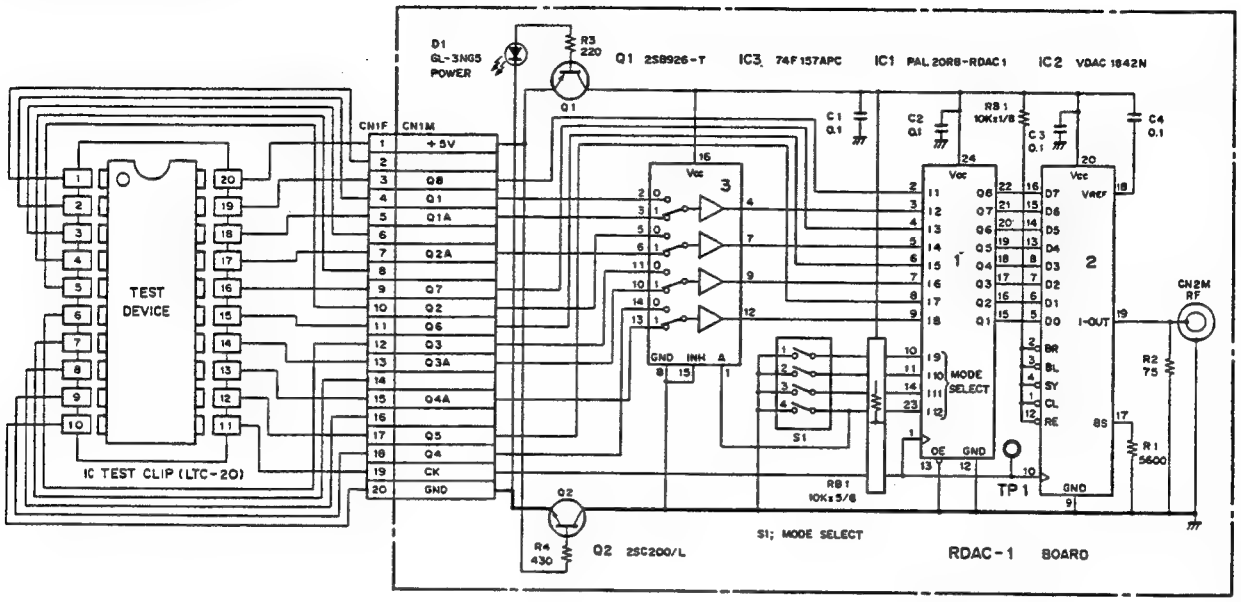
IC-B9 MB7138HSK-VA45011 → MB7138HSK-VA45911 PENDING

IC-C9 MB7138HSK-VA45021 → MB7138HSK-VA45921 PENDING

IC-D9 MB7138HSK-VA45031 → MB7138HSK-VA45931 PENDING

## 2-6-4. Circuit Diagram and Components

The circuit diagram of the ROVING DAC and the table of components are shown below.




| Ref.No. or Qty | Part No. | SP | Description |
|---|---|---|---|
| 1pc | J-6263-470-A | s | ROVING DAC |
| 1pc | ---------- | - | IC TEST CLIP, LTC-20<br>Manufacturer; AP PRODUCTS INCORPORATED |
| 1pc | J-6264-360-A | s | COAXIAL CABLE ASSY, BNC-UM 1m |
| C1,2,3,4 | 1-161-485-00 | s | CAP, CERAMIC 0.1 50V |
| CN1M | 1-564-857-11 | o | RECEP, PS 20P, MALE |
| CN2M | 1-561-365-21 | o | RECEP, COAXIAL, MALE |
| D1 | 8-719-930-50 | s | DIODE, LED, GL-3NG5 GREEN |
| IC1 | J-6264-370-A | s | IC, PAL20R8-RDAC1 |
| IC2 | ---------- | - | IC, VDAC1842N; D/A CONVERTER<br>Manufacturer; INTECH |
| IC3 | 8-759-938-93 | s | IC, 74F157APC |
| Q1 | 8-729-808-18 | s | TRANSISTOR, 2SB926-T |
| Q2 | 8-729-100-12 | s | TRANSISTOR, 2SC2001L |
| R1 | 1-215-439-00 | s | RES, METAL, 5.6K 1% 1/6W |
| R2 | 1-215-394-00 | s | RES, METAL, 75 1% 1/6W |
| R3 | 1-215-405-00 | s | RES, METAL, 220 1% 1/6W |
| R4 | 1-215-412-00 | s | RES, METAL, 430 1% 1/6W |
| RB1 | 1-231-410-00 | s | RESISTOR BLOCK,10Kx8 |
| S1 | 1-570-598-11 | s | SWITCH, DIP, 4-CKT |

# SECTION 3
# TEST MODE

## 3-1. GENERAL

This section describes the diagnostic functions of the discrete DVPC-1000.

In this 4:2:2 digital VTR system, the system control block is housed in the DVR-1000, and the DVPC-1000, which constitutes the signal processing block, is controlled by the IF-139 board.

Control between the various DVPC-1000 boards and IF-139 board is executed through a single-chip microcomputer called the universal peripheral interface (UPI), and even in the test modes control is executed by the IF-139 board through this UPI.

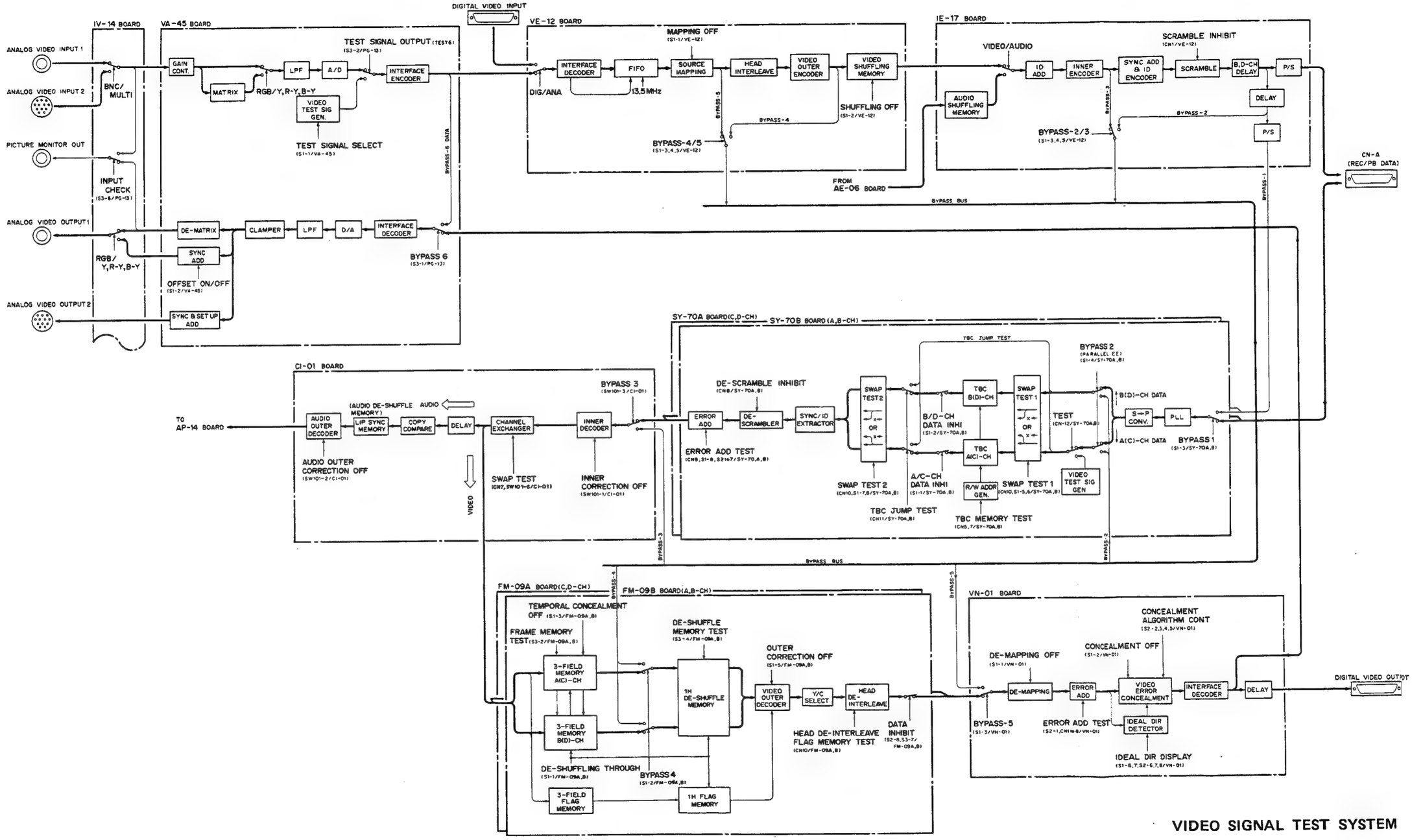
Given below is a list of test modes for the DVPC-1000 video and audio signal systems as well as a system diagram. The various test functions of the video/audio signal systems will now be described.

(Test modes of video signal system)

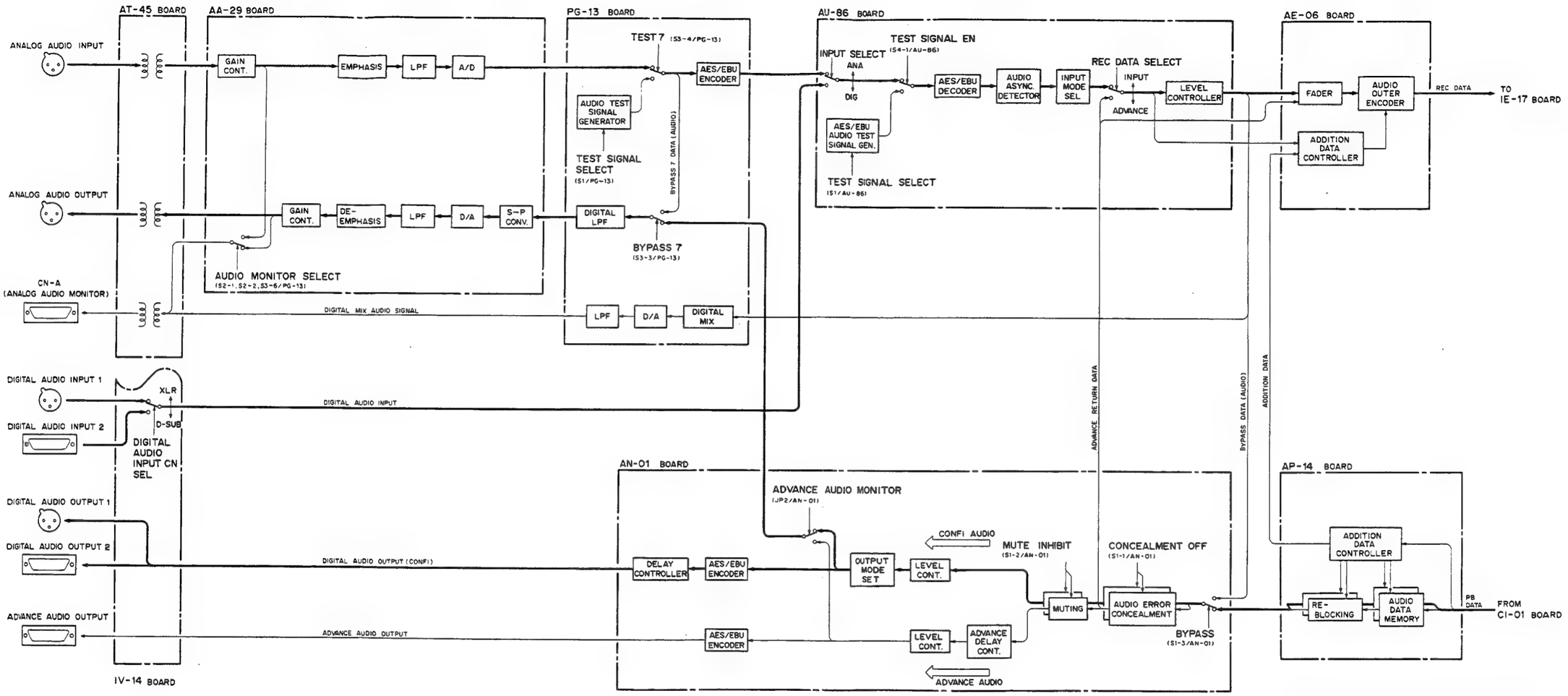
| Board | Test mode | Section |
|---|---|---|
| ..... | Bypass test | 3-4 |
| VA-45 | Video test signal generator | 3-5-1 |
| VE-12 | Source mapping circuit test | 3-5-2 |
| | Video shuffling memory test | 3-5-3 |
| IE-17 | Scramble circuit test | 3-5-5 |
| SY-70A,B | Video test signal generator | 3-5-1 |
| | Swap test | 3-5-5 |
| | TBC memory test | 3-5-6 |
| | TBC jump test | 3-5-6 |
| | De-scramble circuit test | 3-5-4 |
| CI-01 | Inner decoder correction capability test | 3-5-7 |
| | SWAP TEST | 3-5-5 |
| FM-09A,B | 3-field memory test | 3-5-8 |
| | De-shuffle memory test | 3-5-3 |
| | | 3-5-9 |
| | Outer decoder correction capability test | 3-5-8 |
| | Head de-interleave flag memory test | 3-5-10 |
| | FM-09 board output data test | 3-5-11 |
| VN-01 | De-mapping circuit test | 3-5-2 |
| | Ideal direction detector circuit test | 3-5-12 |
| | Error concealment circuit test | 3-5-13 |

(Test modes of audio signal system)

| Board | Test mode | Section |
|---|---|---|
| ..... | Bypass test | 3-4 |
| AA-29 | Audio monitor test (input check) | 3-5-2 |
| PG-13 | Audio test signal generator | 3-5-1 |
| AU-86 | AES/EBU test signal generator | 3-5-1 |
| CI-01 | Audio 2-time write processing circuit test | 3-5-6 |
| | Outer decoder circuit test | 3-5-4 |
| AN-01 | Audio error concealment circuit test | 3-5-5 |
| | Muting off test | 3-5-6 |
| | Advance audio monitor test | 3-5-7 |




**VIDEO SIGNAL TEST SYSTEM**




**AUDIO SIGNAL TEST SYSTEM**

## 3-2. BOARD SWITCH/JUMPER SETTINGS

Refer to the section 5-5 INITIAL SETTING OF THE SWITCHES/JUMPERS and set the switches and jumpers on the boards for the test modes.
The settings only for those switches and jumpers whose settings need to be changed are described below.
After the tests, return the switches and jumpers whose settings were changed to their original positions. If they are left as they are, the other test modes may be adversely affected and the processor may not function normally.

## 3-3. ERROR MESSAGES

If an error occurs after the power has been switched on or during normal operation, an error message will appear on the control panel of the DVR-1000. The operating status of the DVPC-1000 and the locations of problems can be checked by means of the alarm indicators on the front panel or on the front of the boards. Problems in the power supply are checked using the alarm lamp on the front panel of the power supply unit. For details on these error messages and alarm indicators reference should be made to the Operation Manuals of the DVR-1000 and DVPC-1000.

## 3-4. BYPASS MODES

The following bypass routes are provided in the DVPC-1000.
When there is a defect or malfunction inside the processor, the bypass tests are performed in order to isolate a particular circuit or circuits where it is assumed that a board is malfunctioning or the problem is actually lies.
Given below is a table listing the settings of the switches for the bypass tests, followed by flow charts of the bypass modes.

(Video signal system bypass test modes)

| Mode | Switch setting | |
|---|---|---|
| BYPASS 1 (Note)<br>(SERIAL EE)<br>(Between IE-17 → SY-70) | S3/IF-139:<br>S1-3/SY-70A,B: | TEST ..... ON<br>BYPASS 1 ... ON |
| BYPASS 2<br>(PARALLEL EE)<br>(Between IE-17 → SY-70) | S3/IF-139:<br>S1-4/SY-70A,B:<br>S1-3/VE-12:<br>S1-4/VE-12:<br>S1-5/VE-12: | TEST ..... ON<br>BYPASS 2 ... ON<br>BYPASS 3 ...OFF<br>BYPASS 4 ...OFF<br>BYPASS 5 ...OFF |
| BYPASS 3<br>(Between IE-17 → CI-01) | S3/IF-139:<br>SW101-3/CI-01:<br>S1-3/VE-12:<br>S1-4/VE-12:<br>S1-5/VE-12: | TEST ..... ON<br>BYPASS 3 ... ON<br>BYPASS 3 ... ON<br>BYPASS 4 .. OFF<br>BYPASS 5 .. OFF |
| BYPASS 4 (Note)<br>(Between VE-12→ FM-09) | S3/IF-139:<br>S1-2/FM-09A,B:<br>S1-4/VE-12:<br>S1-5/VE-12:<br>S6-8/TG-28: | TEST ..... ON<br>BYPASS 4 ... ON<br>BYPASS 4 ... ON<br>BYPASS 5 ... OF<br>TEST ..... ON |
| BYPASS 5 (Note)<br>(Between VE-12→ VN-01 | S3/IF-139:<br>S1-3/VN-01:<br>S1-5/VE-12:<br>S6-8/TG-28: | TEST ..... ON<br>BYPASS 5 ... ON<br>BYPASS 5 ... ON<br>TEST ..... ON |
| BYPASS 6<br>(On VA-45 board) | S3/IF-139:<br>S3-1/PG-13: | TEST ..... ON<br>BYPASS 6 ... ON |
| INPUT CHECK (Note) | S3/IF-139:<br>S3-6/PG-13: | TEST ..... ON<br>BYPASS 6 ... ON |

(Audio signal system bypass test modes)

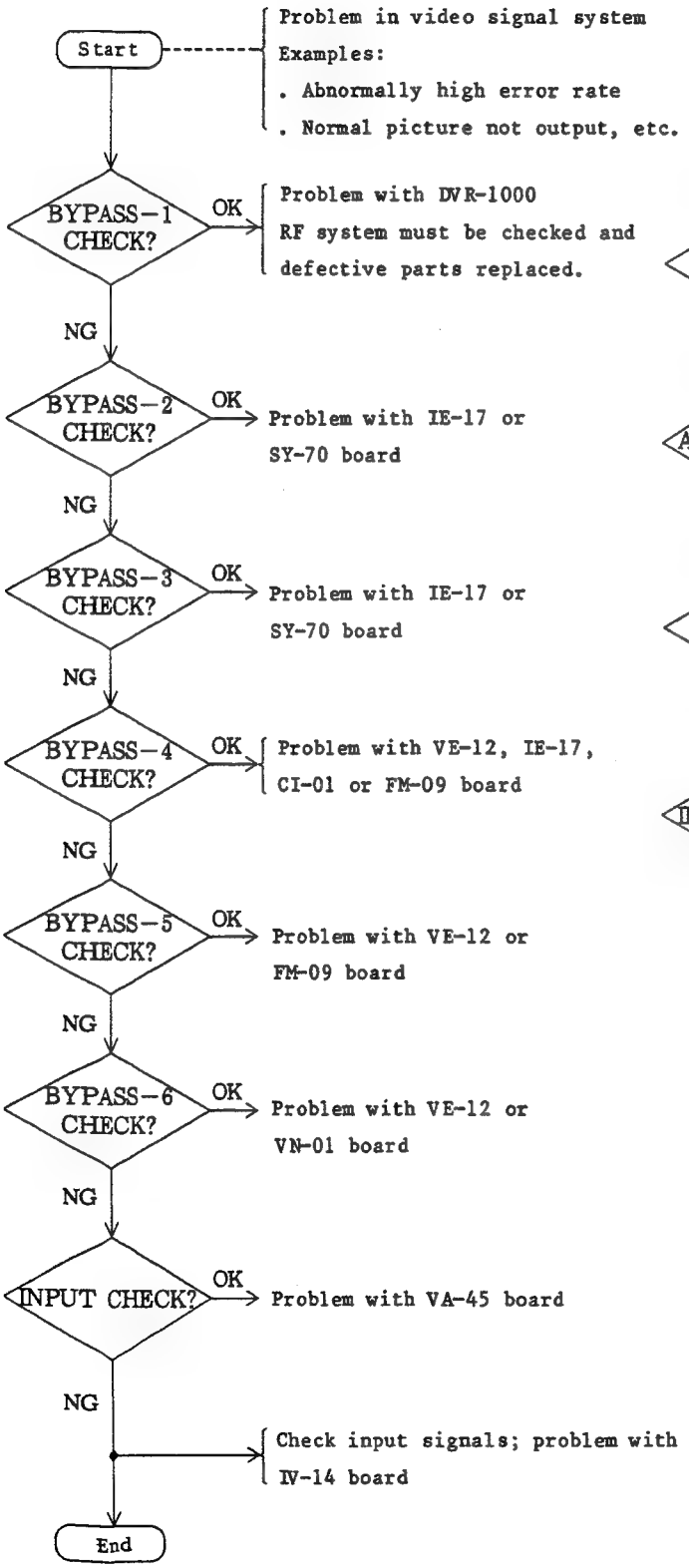
| Mode | Switch setting | |
|---|---|---|
| AUDIO BYPASS<br>(Between AU-86 → AN-01) | S3/IF-139:<br>S1-3/AN-01: | TEST ..... ON<br>BYPASS ..... ON |
| BYPASS 7<br>(Between AA-29 ↔ PG-13) | S3/IF-139:<br>S3-3/PG-13: | TEST ..... ON<br>BYPASS 7 ... ON |

**(Note)**

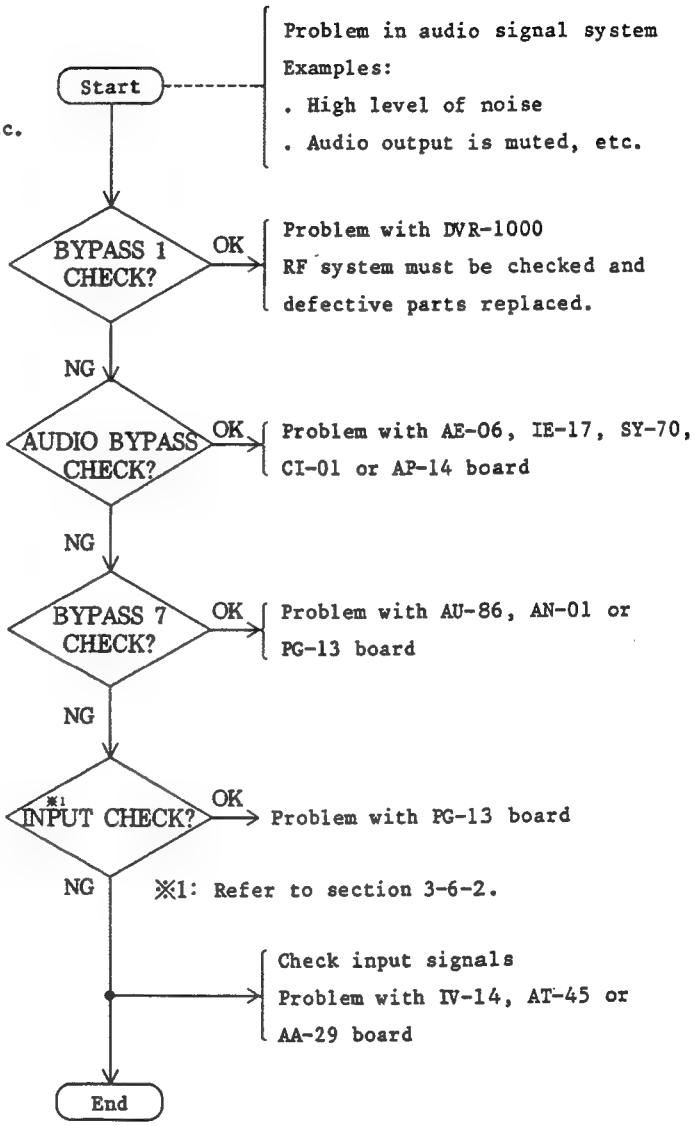
- In the BYPASS-4/5 modes, the brightness may change since the output pictures shift in the horizontal direction and the pedestal clamp position shifts.
- In the BYPASS-1 and INPUT CHECK modes among the bypass modes for the video signal system, the audio signals are also bypassed in the same way.
  Refer to section 3-6-2 for details on the input check function for the audio signal system.

(3-4. BYPASS MODES)

(Flow chart of video signal system bypass modes)




(Flow chart of audio signal system bypass modes)



## 3-5. VIDEO SIGNAL SYSTEM TEST FUNCTIONS

### 3-5-1. Video Test Signal Generator

The DVPC-1000 is provided with video test signal generators on both the VA-45 board and SY-70 boards. Circuitry can easily be checked and adjusted by using the test functions described below and the bypass function in combination with the outputs of these signal generators.

**Output signal of test signal generator on VA-45 board:**

Switch/jumper settings:

S3/IF-139: TEST ..... ON
S3-2/PG-13: TEST-6 ..... ON
Settings otherwise identical to those in section 5-5.

The COLOR BARS or MULTI BURST signal is output. The output signal is selected by switch S1-1/VA-45. When this switch is ON, the MULTI BURST signal is output; when it is OFF, the COLOR BARS signal is output.

This test signal is used to adjust the video signal system and check its circuitry.

**Output signal of test signal generator on SY-70A,B boards:**

Switch/jumper settings:

CN12/SY-70A,B: TEST SIGNAL OUTPUT ... SHORT
Settings otherwise identical to those in section 5-5.

A stair step (4-bit, 16-level) signal, that shown in the figure below, is input into channel A/C of the TBC on the SY-70A,B boards. This signal is used for checking the TBC memory circuit on the SY-70A,B boards.

When used in tandem with the swap test, this stair step signal can also be input into channels B and D. When the CI-01 board with the board number suffix of -12 or following is used, the 3-field memory and 1H de-shuffle memory on the FM-09A,B boards can also be checked using this test signal. In these cases, the switches and jumpers are set as below.

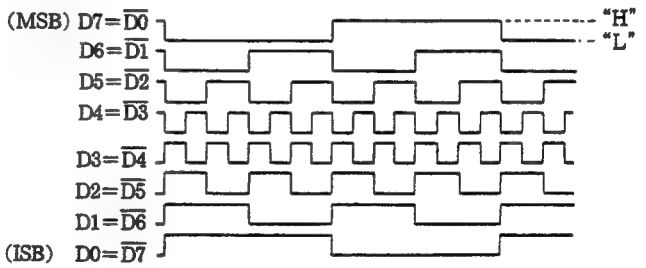
(1) When inputting the test signal into channels B and D

CN12/SY-70A,B: TEST SIGNAL OUTPUT ..... SHORT
S1-5/SY-70A,B: SWAP1 TEST ..... ON
S1-6/SY-70A,B: SWAP1 TEST DIR ..... ON
Settings otherwise identical to those in section 5-5.

(2) When checking the FM-09A,B boards using the test signal

CN12/SY-70A,B: TEST SIGNAL OUTPUT ..... SHORT
CN11/SY-70A,B: TBC BYPASS TEST ..... SHORT
CN8/SY-70A,B: DE-SCRAMBLE INHIBIT .. INHIBIT
SW101-5/CI-01: INNER DECODER BYPASS ..... ON
Settings otherwise identical to those in section 5-5.
Reference should be made to sections 3-5-3 and 3-5-9 for details on the FM-09A,B boards check methods.

**Output test signals**



### 3-5-2. Source Mapping/De-mapping Circuit Test Function

Switch/jumper settings:

S3/IF-139: TEST ..... ON
S1-1/VE-12: MAPPING OFF ..... See below
S1-5/VE-12: BYPASS 5 ..... ON
S1-1/VN-01: DE-MAPPING OFF ..... See below
S1-3/VN-01: BYPASS 5 ..... ON
S6-8/TG-28: TEST 8 ..... ON
Settings otherwise identical to those in section 5-5.

This is the check function for the mapping circuit on the VE-12 board and de-mapping circuit on the VN-01 board. There is no video data mapping when the S1-1 /VE-12 and S1-1/VN-01 switches are ON.
If one switch is ON and the other OFF, pictures with the hue changed will be output.
The circuits are functioning normally if a normal picture appears when both switches are set ON or OFF.

### 3-5-3. Line Shuffling/De-shuffling Memory Test Function

Switch/jumper settings:

S3/IF-139: TEST .....ON
S1-1/VE-12: SHUFFLING OFF ..... See below
SW101-3/CI-01: BYPASS 3 ..... ON
S1-3/VE-12: BYPASS 3 ..... ON
S1-4/VE-12: BYPASS 4 ..... OFF
S1-5/VE-12: BYPASS 5 ..... OFF
S1-1/FM-09A,B: DE-SHUFFLING THROUGH
..... See below
Settings otherwise identical to those in section 5-5.

This is the check function for the shuffling memory on the VE-12 board and de-shuffling memory on the FM-09A,B boards. There is no video data shuffling and de-shuffling when the S1-2/VE-12 and S1-1/FM-09A,B switches are ON.
If one switch is ON and the other OFF, pictures with the hue and contours distorted and with a high noise level will be output.
The circuits are functioning normally if a normal picture appears when both switches are set ON or OFF.

### 3-5-4. Scramble/De-scramble Circuit Test Function

Switch/jumper settings:

CN1/IE-17: SCRAMBLE INHIBIT..... SHORT
CN8/SY-70A,B: DE-SCRAMBLE INHIBIT..... SHORT
S1-3/SY-70A,B: BYPASS 1 ..... ON
Settings otherwise identical to those in section 5-5.

This is the check function for the scramble circuit on the IE-17 board and de-scramble circuit on the SY-70A,B boards. There is no video data scrambling and de-scrambling when the CN1/IE-17 and CN8/SY-70A,B jumpers are shorted. This function checks the changes in the pictures which are output when these jumper settings are changed.

### 3-5-5. Swap Test Function

Switch/jumper settings:

| | | |
|---|---|---|
| S3/IF-139: | TEST ..... | ON |
| CN10/SY-70A,B: | SWAP TEST EN ..... | SHORT |
| S1-5/SY-70A,B: | SWAP1 TEST ..... | See below |
| S1-6/SY-70A,B: | SWAP1 TEST DIR ..... | See below |
| S1-7/SY-70A,B: | SWAP2 TEST ..... | See below |
| S1-8/SY-70A,B: | SWAP2 TEST DIR ..... | See below |
| CN7/CI-01; | SWAP TEST ..... | SHORT |
| SW101-6/CI-01; | SWAP TEST DIR ..... | See below |

Settings otherwise identical to those in section 5-5.

The swap test function pinpoints the problem channel by supplying the data of either channel A or B (C or D) to the other channel and comparing the output data of both channels.
Swap test circuits are provided in both the input (SWAP1) and output (SWAP2) sections of the TBC circuit on the SY-70A,B boards. It is also possible to set the SWAP1 and SWAP2 tests simultaneously.
In addition, a similar swap test function is contained in the channel exchanger on the CI-01 board.

**SWAP1 test (SY-70 board)**

This is the swap test mode for the TBC input section on the SY-70A,B boards. It is entered when the S1-5/SY-70A,B switch is set ON.
The TBC input signal applying at this time is selected by the S1-6/SY-70A,B switch. When S1-6 is OFF, the channel A (C) data are input into the TBC channels A and B (C and D); when it is ON, the channel B (D) data are input.
The SWAP1 test is also used when supplying the output signals of the test signal generator on the SY-70A,B board to channel B (D). Refer to section 3-5-1 for more details on this function.

**SWAP2 test (SY-70 board)**

This is the swap test mode for the TBC output section on the SY-70A,B boards. It is entered when the S1-7/SY-70A,B switch is set ON.
The TBC input signal applying at this time is selected by the S1-8/SY-70A,B switch. When S1-8 is OFF, the channel A (C) data are output to the TBC channels A and B (C and D); when it is ON, the channel B (D) data are output.

**SWAP test (CI-01 board)**

The CI-01 board of which last digits of the board number is -12 or higher contains the swap test function in its channel exchanger. It is primarily a test function for checking the memory on the FM-07 board. The swap mode is specified when CN7/CI-0 is shorted.
The mode is selected by SW101-6/CI-01. Data on A and C channels, if SW101-6 is off, and on B and D channels, if it is on, are outputted to A and B channels, and C and D channels, respectively.

**Test method**

Although the description is made by referring to the SY70 board, the test is performed similarly for the CI-01.
The swap test is effective when one of the two channels (A, B or C, D) on the SY-70A,B boards is functioning properly. The channels are configured with virtually the same circuitry from the SY-70A,B board to the CI-01 board inner decoder output section, and so the circuitry will function normally in the swap test mode.
When, for instance, channel A is problem-free but there is an error in channel B, the SWAP2 mode is entered, the TBC output data of channel A are supplied to channel B, and the output of the CI-01 inner decoder (TP1, 2, 3, 4/CI-01) is observed. If the circuitry is functioning properly, the same data will be output at TP1 and TP2 on the CI-01 board. In this case, it can be assumed that the trouble lies before the TBC output section on the SY-70A,B board. If the data at TP1 and TP2 differ, the trouble lies between the TBC output section on the SY-70A,B board and the inner decoder on the CI-01 board. In this case, the trouble can be pinpointed by the method outlined below.
Since the SWAP2 test circuit is in the TBC output section, this means that the data will not contain any jitter after this block, the data in channels A and B (or C and D) will be completely identical and that a defective IC can be easily pinpointed.

In actual fact, the data of channel A in the same circuit is supplied to CH-1 of an oscilloscope and the data of channel B are supplied to CH-2 in the inverted mode. The oscilloscope is then set to the ADD mode and the data of the 2 channels are compared. The circuitry is functioning normally if the trace on the oscilloscope is a straight line. It sometimes happens that the trace will have a slight fringe but this is normal, provided that the pulse width is sufficiently shorter than the latch clock period.
The latch output of the LS374, for instance, should be observed when comparing the data. Avoid directly observing the ROM output.
This is how the sync detector circuit and ID detector circuit, which are difficult to debug, can be checked comparatively easily.

### 3-5-6. TBC Test Function

The TBC circuit on the SY-70A,B boards has the following test functions.
(1) Data output inhibit test
(2) Read/write address test
(3) TBC jump test

(1) Data output inhibit test
Switch/jumper settings:

S3/IF-139: TEST SW ..... ON
S1-1/SY-70A,B: A/C-CH DATA INHIBIT ..... See below
S1-2/SY-70A,B: B/D-CH DATA INHIBIT ..... See below
Settings otherwise identical to those in section 5-5.

This function serves to turn all the TBC output data of a specific channel into errors. When switch S1-1/SY-70A,B is ON, all the TBC output data of channel A (C) are set high; when it is OFF, the channel B (D) data are set high. This function is used when pinpointing the defective channel.

(2) Read/write address test
Switch/jumper settings:

CN5/SY-70A,B: TBC MEMORY TEST1 .... See below
CN7/SY-70A,B: TBC MEMORY TEST2 .... See below
Settings otherwise identical to those in section 5-5.

This function checks the TBC read/write addresses. When CN5/SY-70A,B is shorted, the output of the TBC WRITE address generator is suspended and no data are written into the TBC. The read address is input to the address input pins of the TBC memory (ICC15-C20, ICH15-H20/SY-70A,B).
When CN7/SY-70A,B is shorted, the data from the TBC are not read and the write address is input to the address input pins of the TBC memory.
CN5 and CN7 must not be shorted at the same time.

(3) TBC jump test
Switch/jumper settings:

CN11/SY-70A,B: JUMP TEST ENABLE ..... SHORT
Settings otherwise identical to those in section 5-5.

This is the bypass test function for the TBC circuit. When trouble occurs in the TBC section, it is extremely difficult to know exactly where the trouble lies. This function isolates the circuitry of the TBC and facilitates the circuit checking by comparing the waveforms in the SYNC/ID extraction and decision sections.
When CN11/SY-70A,B has been shorted, the video data are output without being written into the TBC.
Since the processor may not be functioning properly when signals including jitter as in the playback pictures are bypassed, signals without jitter as in parallel EE pictures (BYPASS-2 mode) should be supplied for the TBC jump test.

### 3-5-7. Error Correcting Capability Test (ERROR ADD test)

The error correcting capabilities of the inner and outer decoders are checked by adding errors at the desired positions in the video sync block. The positions where the errors are added and the size of the errors are determined by switches S2 through S7 on the SY-70A,B boards. The channels in which the errors are added are determined by the S1-8/SY-70A,B switch.
Refer to section 2-5 for details on the switch functions. The methods of checking the error correcting capabilities using these switches are outlined below.

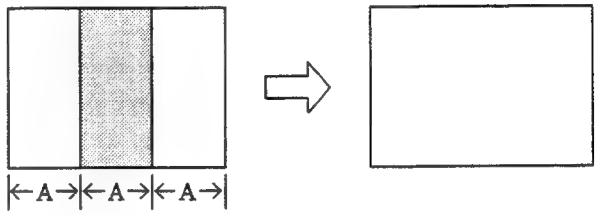
(1) Checking the inner decoder error correcting capability

Switch/jumper settings:

S3/IF-139: TEST SW ..... ON
CN9/SY-70A,B : ERROR ADD TEST ..... SHORT
S1-8/SY-70A,B: ERROR ADD CH SELECT
..... See below
S7/SY-70A,B: ERROR ADD TEST MODE
..... 6, 7, E or F
S1-3/FM-09A,B: TEMPORARY CONCEAL OFF ..... ON
S1-5/FM-09A,B: OUTER CORRECTION OFF ..... ON
S1-2/VN-01: CONCEALMENT OFF ..... ON
Settings otherwise identical to those in section 5-5.

Set the switches and jumpers on the boards as outlined above. Set the switches on the SY-70A or B board, whichever corresponds to the channel in which the errors are to be added, and set the switch on both the FM-09A and B boards.
Set the S1-8 switch on the SY-70A or B board, whichever corresponds to the channel in which the errors are to be added. When S1-8/SY-70A,B is OFF, the errors are added to channel A (C); when it is ON, they are added to channel B (D).

Set the INNER CORRECTION OFF switch S101-1/CI-01 to ON. The errors appear on the entire screen as indicated in the figure below. The LEDs on the front of the FM-09A,B light.
Check that all the errors are cleared (corrected) when the SW101-1/CI-01 switch is set OFF and that the LEDs on the front of the FM-09A,B boards go off. The inner decoder is functioning normally if all the errors are corrected. After having conducted the check, return the above switches and jumpers to their original positions.




SW101-1/CI-01; OFF
area: Error data
A=1/3 x H

SW101-1/CI-01; ON
Errors are cleared

(2) Checking the outer decoder error correcting capability

Switch/jumper settings:

S3/IF-139: TEST SW ..... ON
CN9/SY-70A,B : ERROR ADD TEST
..... SHORTED
S1-8/SY-70A,B: ERROR ADD CH SELECT
..... See below
S2/SY-70A,B: ERROR ADD SIZE (INNER/LSB) .. 4
S3/SY-70A,B: ERROR ADD SIZE (INNER/MS) ... 1
S4/SY-70A,B: ERROR ADD POSITION (LSB) .... 8
S5/SY-70A,B: ERROR ADD POSITION (MSB) .... 8
S6/SY-70A,B: ERROR ADD SIZE (SAMPLE) ..... 7
S7/SY-70A,B: ERROR ADD TEST MODE ..... 0
SW101-1/CI-01: INNER CORRECTION OFF ..... ON
S1-3/FM-09A,B: TEMPORARY CONCEAL OFF ..... ON
S1-2/VN-01: CONCEALMENT OFF ..... ON
Settings otherwise identical to those in section 5-5.

### (3-5-7. Error Correcting Capability Test (ERROR ADD test))

Set the switches and jumpers on the boards as outlined above. Set the switch on the SY-70A or B board, whichever corresponds to the channel in which the errors are to be added, and set the switch on both the FM-09A and B boards.

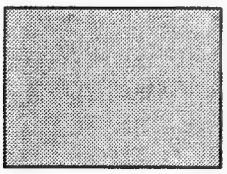
Set the S1-8 switch on the SY-70A or B board, whichever corresponds to the channel in which the errors are to be added. When S1-8/SY-70A,B is OFF, the errors are added to channel A (C); when it is ON, they are added to channel B (D).

Set the OUTER CORRECTION OFF switch S1-5/FM-09A,B to ON. The errors appear over the entire screen in the 525/60 mode and at the positions indicated in the figure below in the 625/50 mode.

Check that all the errors are cleared (corrected) when the S1-5/FM-09A,B switches are set OFF. The outer encoder is functioning normally if all the errors are corrected.

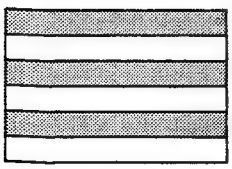
Next, set the S6/SY-70A,B switch to "8" and conduct a similar check. The errors now added will exceed the outer decoder's correcting capability and so residual errors will arise even when the S1-6/FM-09A,B switches are set ON. After having conducted the check, return the above switches and jumpers to their original positions.

525/60 mode

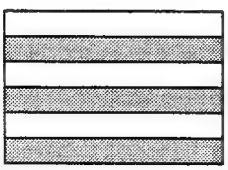


625/50 mode

Channels A, C



Channels B, D



### 3-5-8. 3-Field Memory Read/Write Test

Switch/jumper settings:

| | | |
|---|---|---|
| CN6/FM-09A,B: | TEST | SHORT |
| S3-2/FM-09A,B: | FRAME MEMORY TEST | ON |
| S1-1/FM-09A,B: | DE-SHUFFLING THROUGH | ON |
| CN8/SY-70A,B: | DE-SCRAMBLE INHIBIT | SHORT |
| CN11/SY-70A,B: | JUMP TEST ENABLE | SHORT |
| CN12/SY-70A,B: | TEST SIGNAL OUTPUT | SHORT |
| S1-5/SY-70A,B: | SWAP1 TEST | ON |
| S1-6/SY-70A,B: | SWAP1 TEST DIR | ON |
| SW101-5/CI-01: | INNER DECODER BYPASS | ON |

Settings otherwise identical to those in section 5-5.

Set the switches and jumpers on the boards as outlined above. The test signal (stair step wave; refer to section 3-5-1) is input from the SY-70A,B board into the 3-field memory on the FM-09A,B boards.

TP64 (channels A/C) or TP74 (channels B/D) on the FM-09A,B boards are clamped to ground only for an instant. This serves as a trigger, and the input data (test signal from SY-70 board) are written once only into all the addresses (0000-FFFF) of the 3-field memory and these data are subsequently repeatedly read out .

When the 3-field memory is functioning normally, the test signal from the SY-70A,B boards should be output in its original form to the final output IC-J12 (ch annels A/C) or IC-J6 (channels B/D) of the memory.

If the proper output is not obtained, the DRAM and SPS converter configuring the 3-field memory should be checked. To check, observe the memory output using the oscilloscope, and temporarily clamp to ground or +5V the data I/O pins of the DRAM and SPS converter (for instance, in the case of channels A/C, the D7 (MSB) data will be output from pins 22 through 27 of IC-J11/FM-09A,B).

It can then be checked on the oscilloscope whether the clamped data and error position overlap and the defective IC can be pinpointed.

### 3-5-9. 1H De-shuffling Memory Test Function

(Valid only when using the CI-01 board with board number suffix -12 or after)

Switch/jumper settings:

S3-4/FM-09A,B: 1H DE-SHUFFLE MEMORY TEST.. ON
CN6/FM-09A,B: TEST ..... SHORT
S3-2/FM-09A,B: FRAME MEMORY TEST..... ON
CN12/SY-70A,B: TEST SIGNAL OUTPUT ..... SHORT
CN11/SY-70A,B: JUMP TEST ENABLE ..... SHORT
CN8/SY-70A,B: DE-SCRAMBLE INHIBIT .... SHORT
SW101-5/CI-01: INNER DECODER BYPASS ..... ON
Settings otherwise identical to those in section 5-5.

This is the simple write/read test function for the 1H de-shuffle memory. The signal which is output from the test signal generator on the SY-70A,B board is input into the FM-09A,B board by means of the above switch settings.

When TP64 (channel A/C) or TP74 (channel B/D) on the FM-09A,B board is momentarily clamped to ground, the input test signal is written once only into all the addresses of the 3-field memory, the data are subsequently repeatedly read out and input into the 1H de-shuffle memory.

When the S3-4/FM-09A,B switch is ON, no de-shuffling in the lines in the 1H de-shuffle memory (ICH30, J30/SY-70A,B) is performed. This means that the circuit is functioning normally if stair step waveforms are output when the output pin of the de-shuffle memory is observed.

### 3-5-10. Head De-interleave Flag Memory Test

Switch/jumper setting:

CN10/FM-09A,B: HEAD DE INTERLEAVE FLAG MEMORY TEST ..... SHORT
Settings otherwise identical to those in section 5-5.

When CN10 is shorted, the same data as the video Y and C data MSB are respectively input into the flag memory. The flag memory is checked by comparing the flag memory output data with the video data MSB.

In actual fact, the video data MSB is input into channel A of the oscilloscope and the flag memory data into channel B, and either of these is inverted and observed in the ADD mode. The flag memory is functioning normally if the trace on the oscilloscope is a straight line. It sometimes happens that the trace will have a slight fringe but this can be ignored. Make the observations at the following points when comparing the signals.

**Observation points:** FM-09A,B

**Y signal:**

ICA31 pin 19 (VIDEO) and ICC31 pin 15 (FLAG)

**C signal:**

ICB31 pin 19 (VIDEO) and ICC31 pin 12 (FLAG)

### 3-5-11. FM-09A,B Board Output Data Check

Switch/jumper settings:

CN6/FM-09A,B: TEST ..... SHORT
S2-8/FM-09A,B: TEST MODE SELECT ... See below
S3-7/FM-09A,B: OUTPUT DATA INHIBIT ..... ON
Settings otherwise identical to those in section 5-5.

Although the data of 2 channels are processed and output for each of the FM-09A,B boards, the output data of one channel only are processed in this test. This enables the channel with the error to be pinpointed.

The procedure is facilitated by removing one of the two FM-09 boards and providing the output of 1 channel only. When the board is removed while the DVR-1000 is connected, the "BOARD DISCONNECT ERROR OPERATION STOP" error message appears on the control panel but this should be ignored.

The data which are output from the FM-09A,B board depend on the S2-8/FM-09A,B switch setting and are given below:

When S2-8 is ON: Data of channel A (C) only are output

When S2-8 is OFF: Data of channel B (D) only are output

### 3-5-12. Error Concealment Ideal Direction Detector Circuit Check

Switch/jumper settings:

S3/IF-139: TEST ..... ON
S1-2/VN-01: CONCEALMENT OFF ..... OFF
S1-6/VN-01: PINK DISPLAY MODE .. See below
S1-7/VN-01: PINK DISPLAY ON/OFF ..... ON
S2-6/VN-01: IDEAL DIR DISPLAY ..... ON
S2-7/VN-01: DISPLAY CONT1 ..... See below
S2-8/VN-01: DISPLAY CONT2 ..... See below
Settings otherwise identical to those in section 5-5.

Error are corrected by means of the data in the direction (ideal direaction from among H, V, D+ and D-) which has the closest correlation. This test function is for visually checking the ideal direction detector circuit.

When the switches have been set as listed above, pixels whose ideal direction has been specified by the S2-7/VN-01 and S2-8/VN-01 switches are displayed on the monitor in pink. When the S1-6/VN-01 switch is ON, all the pixels concerned will appear in pink; when it is OFF, every fourth pixel will appear in pink.

If there are directions with an identical correlation, they are determined in the sequence of H → V → D- → D+.

When checking, supply a signal whose ideal direction is already known.

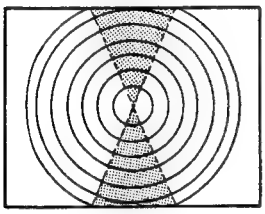
| S2-7/VN-01 | S2-8/VN-01 | Display direction |
|---|---|---|
| OFF | OFF | H(↔) |
| OFF | ON | V(↕) |
| ON | OFF | D-(↘) |
| ON | ON | D+(↗) |

### (3-5-12. Error Concealment Ideal Direction Detector Circuit Check)

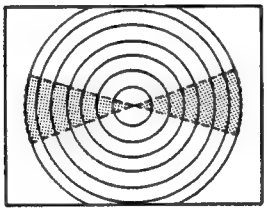
**For color bars:**

The ideal direction is vertical for areas on the boundary lines of the colors and horizontal for other areas.

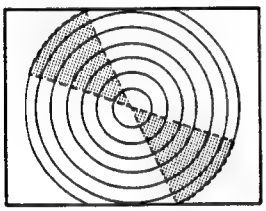
**For zone plates:**



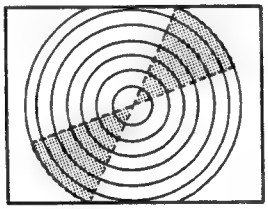
H (↔) direction



V (↕) direction



D+ (↗) direction



D- (↖↘) direction

### 3-5-13. Error Concealment Circuit Test

Switch/jumper settings:

S3/IF-139: TEST ..... ON
S1-2/VN-01: CONCEALMENT OFF ..... OFF
S2-1/VN-01: ERROR ADD TEST ..... ON
CN1-CN8/VN-01: ERROR PATTERN SELECT
..... See below
S2-2,3,4,5/VN-01: CONCEALMENT ALGORITHM CONTROL
..... See below
Settings otherwise identical to those in section 5-5.

The error concealment circuit is checked by adding errors in predetermined patterns to the video data. The errors are created by inverting the video Y data MSB and error flag. It is therefore not possible in this test mode to check the chroma signal system.

The error patterns are selected by jumper plugs CN1 through CN8 on the VN-01 board. Switches S2-2, 3, 4, 5/VN-01 are used for defining the concealment mode. The error patterns and concealment modes selected by these switches and jumpers are listed in the table below. All the errors in error patterns #1 through # 3 are corrected by 2-point interpolation. All the error patterns should therefore clear if the concealment mode is set to MODE 1.

Similarly, the errors in patterns #4 through #6 cannot be corrected by 2-point interpolation but by simple replacement (MODE 2). The errors in patterns #7 through #9 are corrected by recursive replacement (MODE 3) since if simple replacement is used to correct them, the error data in the center of the 3 lines (sample) will be left uncorrected. In this way, the concealment mode is selected in line with the error pattern which has been added, and whether or not an error pattern is present is checked.

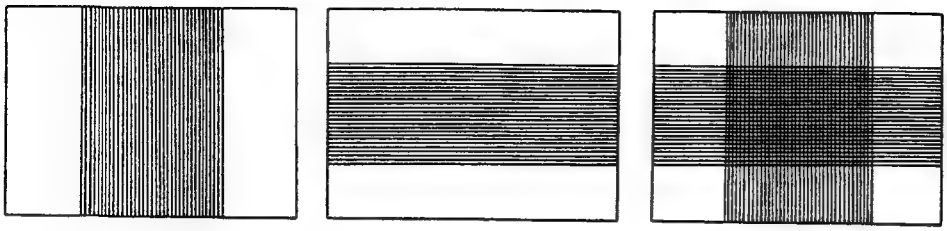
However, with error concealment, only the error data are corrected-the input data are not reproduced. This means that it will appear that the input pattern is reproduced for simple signals such as color bars, but the structure only for the low components of spatial frequencies will be reproduced with signals having a complex structure such as zone plates.

Since concealment cannot be applied to any data except video data, errors will appear on the screen when the monitor is set to the under scan mode.

| Jumper plug (CN1 through 8) | | | | | | | | Error pattern |
|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
| S | O | O | S | O | O | O | S | 2-point interpolation #1 |
| | | | | | | S | O | 2-point interpolation #2 |
| | | | | | | S | S | 2-point interpolation #3 |
| O | S | O | O | S | O | O | S | Simple replacement #4 |
| | | | | | | S | O | Simple replacement #5 |
| | | | | | | S | S | Simple replacement #6 |
| O | O | S | O | O | S | O | S | Recursive replacement #7 |
| | | | | | | S | O | Recursive replacement #8 |
| | | | | | | S | S | Recursive replacement #9 |

O:OPEN S:SHORT

(3-5-13. Error Concealment Circuit Test)



#1; OXOXOXOXOXOXO
OXOXOXOXOXOXO
OXOXOXOXOXOXO
OXOXOXOXOXOXO
OXOXOXOXOXOXO

#2; OOOOOOOOOOOOOO
XXXXXXXXXXXXXX
OOOOOOOOOOOOOO
XXXXXXXXXXXXXX
OOOOOOOOOOOOOO

#3; Pattern combining patterns #1 and #2.

#4; OXXOXXOXXOXXO
OXXOXXOXXOXXO
OXXOXXOXXOXXO
OXXOXXOXXOXXO
OXXOXXOXXOXXO
OXXOXXOXXOXXO
OXXOXXOXXOXXO

#5; OOOOOOOOOOOOOO
XXXXXXXXXXXXXX
XXXXXXXXXXXXXX
OOOOOOOOOOOOOO
XXXXXXXXXXXXXX
XXXXXXXXXXXXXX
OOOOOOOOOOOOOO

#6; Pattern combining patterns #4 and #5.

#7; OXXXOXXXOXXXO
OXXXOXXXOXXXO
OXXXOXXXOXXXO
OXXXOXXXOXXXO
OXXXOXXXOXXXO
OXXXOXXXOXXXO
OXXXOXXXOXXXO

#8; OOOOOOOOOOOOOO
XXXXXXXXXXXXXX
XXXXXXXXXXXXXX
XXXXXXXXXXXXXX
OOOOOOOOOOOOOO
XXXXXXXXXXXXXX
XXXXXXXXXXXXXX

#9; Pattern combining patterns #7 and #8.

X: Error data

| S2-2 | S2-3 | S2-4 | S2-5 | Concealment mode |
|---|---|---|---|---|
| ON | * | * | * | MODE 0: No error correction |
| OFF | ON | * | * | MODE 1: Correction with 2-point interpolation only |
| OFF | OFF | ON | * | MODE 2: Correction by 2-point interpolation and simple replacement |
| OFF | OFF | OFF | ON | MODE 3: Correction by 2-point interpolation, simple replacement, and recursive replacement |

*: Does not apply.

## 3-6. AUDIO SIGNAL SYSTEM TEST FUNCTIONS

### 3-6-1. Audio Test Signal Generators

The DVPC-1000 is provided with audio test signal generators both on the PG-13 board and AU-86 board. The audio signal system can be adjusted and its circuitry checked by using these test signals.

**Signal generator on PG-13 board**

Switch/jumper settings:

S3/IF-139: TEST ..... ON
S1/PG-13: AUDIO TEST SIGNAL SELECT
..... See below
S3-4/PG-13: TEST-7 ..... ON
Settings otherwise identical to those in section 5-5.

The signal from the test signal generator which corresponds with the S1/PG-13 setting is output to this line system. For further details, refer to section 2-5-4.

**Signal generator on AU-86 board**

Switch/jumper settings:

S3/IF-139: TEST ..... ON
S1/AU-86: AUDIO TEST SIGNAL SELECT
.....See below
S4-1/AU-86: TEST SIGNAL ENABLE ..... ON
Settings otherwise identical to those in section 5-5.

The AES/EBU format test signal is output to this line system. The output signal is selected by the S4-1 switch on the AU-86 board. For further details, refer to section 2-5-6.

### 3-6-2. Audio Monitor Test (Input Check)

Switch/jumper settings:

S3/IF-139: TEST ..... ON
JP1/PG-13: TEST ..... SHORT
S2-1/PG-13: AUDIO MONITOR SELECT 1
..... See below
S2-2/PG-13: AUDIO MONITOR SELECT 2
..... See below
S3-6/PG-13: PB BYPASS ..... See below
Settings otherwise identical to those in section 5-5.

This is the audio input check function which is used to adjust and check the audio monitoring system.

In accordance with the settings of the S2-1/2 and S3-6 switches on the PG-13 board, the following audio input signals are output to the audio monitor output connectors. The same signals are output to the left and right channels of the monitor output connectors.

| S3-6 | S2-1 | S2-2 | Audio monitor output (L/R-CH) |
|---|---|---|---|
| ON | ON | ON | CH 1 analog audio input signal |
| | | OFF | CH 2 analog audio input signal |
| | OFF | ON | CH 3 analog audio input signal |
| | | OFF | CH 4 analog audio input signal |
| OFF | ON | ON | CH 1 analog audio output signal |
| | | OFF | CH 2 analog audio output signal |
| | OFF | ON | CH 3 analog audio output signal |
| | | OFF | CH 4 analog audio output signal |

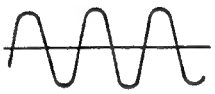
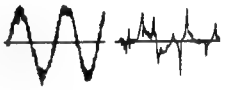
### 3-6-3. Audio 2-Time Writing Circuit Test Function

Switch/jumper settings:

S3/IF-139: TEST ..... ON
S1/AU-86: AUDIO TEST SIGNAL SELECT ... 0
S4-1/AU-86: TEST SIGNAL ENABLE ..... ON
S1-1/SY-70A,B: CH-A/C DATA INHIBIT ..... See below
S1-2/SY-70A,B: CH-B/D DATA INHIBIT ..... See below
S1-3/SY-70A,B: SERIAL EE (BYPASS-1) ..... ON
SW101-2/CI-01: AUDIO OUTER CORRECTION OFF ..... ON
S1-1/AN-01: AUDIO CONCEALMENT OFF ..... ON
S1-2/AN-01: MUTE INHIBIT ..... ON
Settings otherwise identical to those in section 5-5.

The same data are written twice onto different tracks on the tape. Provided that one set of data is error-free even when the other set is full of errors, errors will not appear in the output data even if the error concealment function is off.
These processing circuits are tested.
Check that the signals below are output at the test pins listed below in accordance with the settings of the S1-1 and S1-2 switches on the SY-70A,B boards.
Check that noise-free sinusoidal waves are also output when the AUDIO CONCEALMENT switch S1-1/AN-01 is set OFF during test modes 5 through 8. If there is noise in these waves or if random signals are output, a defect in the audio error concealment circuit may be to blame.
Observation points:

CH-1: TP501/AA-29 CH-2: TP601/AA-29
CH-3: TP701/AA-29 CH-4: TP801/AA-29

| Test mode | SY-70A board | | SY-70B board | | Output signal |
|---|---|---|---|---|---|
| | S1-1 | S1-2 | S1-1 | S1-2 | |
| 1 | OFF | OFF | ON | ON | Noise-free signal is output.  |
| 2 | OFF | ON | ON | OFF | |
| 3 | ON | OFF | OFF | ON | |
| 4 | ON | ON | OFF | OFF | |
| 5 | OFF | ON | ON | ON | Signal with noise or random signal is output.  |
| 6 | ON | OFF | ON | ON | |
| 7 | ON | ON | OFF | ON | |
| 8 | ON | ON | ON | OFF | |

### 3-6-4. Outer Decoder Circuit Test

Switch/jumper settings:

S3/IF-139: TEST ..... ON
SW101-2/CI-01: AUDIO OUTER CORRECTION OFF ..... ON
Settings otherwise identical to those in section 5-5.

Errors in the audio outer decoder are not corrected when the SW101-3/CI-01 switch is ON. Check the changes in the output signal when the switch is selected.

### 3-6-5. Audio Error Concealment Circuit Test

Switch/jumper settings:

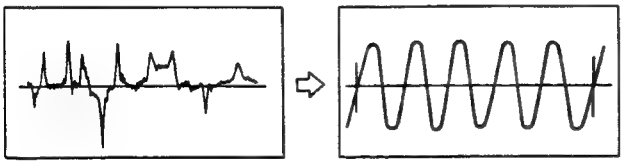
| | | |
|---|---|---|
| S3/IF-139: | TEST ..... | ON |
| S1/AU-86: | AUDIO TEST SIGNAL SELECT ... | 0 |
| S4-1/AU-86: | TEST SIGNAL ENABLE ..... | ON |
| S1-1/SY-70A,B: | A/C-CH DATA INHIBIT ..... | OFF |
| S1-2/SY-70A,B: | B/D-CH DATA INHIBIT ..... | ON |
| S1-3/SY-70A,B: | SERIAL EE ..... | ON |
| S1-1/AN-01: | CONCEALMENT OFF .... | See below |
| S1-2/AN-01: | MUTE INHIBIT ..... | ON |

Settings otherwise identical to those in section 5-5.

Observe the analog audio output signals when the S1-1/AN-01 switch is set to ON and OFF.
Check that a random signal resembling that below is output to the analog output connectors for channels 1, 2, 3 and 4 when S1-1 is ON, and that a sinusoidal wave is output when it is OFF.
The circuit is functioning normally if the following ratings are satisfied when the level and period of the sinusoidal waves are observed at this time. Also check, as shown in the figure below, that there is no noise apart from the noise generated periodically.

Level: 28.0±0.2dB(UC/EK)
24.0±0.2dB(J)
Period: CH-1=4.0±0.2msec
CH-2=2.0±0.1msec
CH-3=1.00±0.05msec
CH-4=0.50±0.03msec

ANALOG AUDIO OUTPUT



When S1-1/AN-01 is ON  When S1-1/AN-01 is OFF

### 3-6-6. Muting Circuit TestSwitch/jumper settings:3

Switch/jumper settings:

| | | |
|---|---|---|
| S3/IF-139: | TEST ..... | ON |
| S1/AU-86: | AUDIO TEST SIGNAL SELECT ... | 0 |
| S4-1/AU-86: | TEST SIGNAL ENABLE ..... | ON |
| S1-1/SY-70A,B: | A/C-CH DATA INHIBIT ..... | ON |
| S1-2/SY-70A,B: | B/D-CH DATA INHIBIT ..... | ON |
| S1-3/SY-70A,B: | SERIAL EE ..... | ON |
| S1-1/AN-01: | CONCEALMENT OFF ..... | ON |
| S1-2/AN-01: | MUTE INHIBIT ..... | See below |

Settings otherwise identical to those in section 5-5.

Check that the outputs of all channels are muted when the S1-2/AN-01 switch is set to OFF.
Set the switch to ON to check the playback data when errors which cannot be concealed arise in the audio data and the output is muted.

### 3-6-7. Advance Audio Monitor Test

Switch/jumper settings:

| | | |
|---|---|---|
| JP2/AN-01: | ADVANCE AUDIO MONITOR ..... | SHORT |

Settings otherwise identical to those in section 5-5.

When JP2/AN-01 is shorted, the advance head playback signal is output to the analog audio output connector. When this function is used together with the audio monitor test function (see section 3-6-2), the advance head playback signal can also be monitored.

# SECTION 4
# THEORY OF OPERATION

## OUTLINE

The 4:2:2 Component Digital VTR System by SONY is a digital VTR system based on the CCIR-657 standard which is unified worldwide. Since both video and audio signals are digitally recorded and played back, this system not only ensures high levels of both picture and sound quality but also makes it possible to conduct editing operations without any deterioration in this quality if the system is interconnected with equipment designed to handle digital signals only.

The system consists of the following 3 components:

**BKDV-1010 Control Panel;**
This enables almost all the system's operations to be controlled.

**DVR-1000 Digital Cassette VTR;**
This controls the recording, playback and other tape transport systems.

**DVPC-1000 Digital Signal Processor;**
This provides digital/analog processing for the video and audio signals.

By switching a selector on one of the circuit boards inside, the DVPC-1000 can accommodate either the 525/60 or 625/50 scanning line system.
Digital and analog signal input/output connectors are provded to enable hookup with existing equipment. The digital video I/O signals are based on the SMPTE RP-125/EBU TECH3246-E standard. The digital audio input/output signals are based on the AES/EBU format. Not only the Y, R-Y and B-Y signals but also the R, G and B signals can be used as the analog video input/output signals. Finally, the 12-pin multi-connector enables analog component signals from a Betacam unit to be directly input and output.
The system settings and the selection statuses of the input signals are displayed by the function indicators on the front panel of the equipment. Alarm lamps indicate whether the components are operating properly.

Even when errors occur in data readout due to dirt or marks on the tape, the powerful error correction capability (2-dimensional product code which uses the outer/inner error correction code) based on the D-1 format ensures high-quality playback. When errors cannot be corrected, the error concealment circuit compensates for the missing signals.

This section describes the D-1 format in Section 4-1 and then provides a detailed description of the circuit boards in the DVPC-1000 in Section 4-2 and following.

## 4-1. D-1 FORMAT

The description given in this section is based on the CCIR-657 (D-1 format). The SMPTE RP-125/EBU TECH3246-E standard applies to the video interfaces, and the AES/EBU format applies to the audio interfaces.

### 4-1-1. Interface Formats

This section describes the structure of the digital video and digital audio signals supplied to the DVPC-1000.

**1. Parallel video interface**

Under the parallel video interface format, the 8-bit data signals and clock signal are sent by means of 9 sets of balanced twisted pair lines.

The data signals which are sent are composed of the video data, timing reference signal, ancillary data and identification (ID) data. These signals are time-division- multiplexed and transmitted by the non-return to zero (NRZ) code.

**(A) Video data**

The video data is provided by quantizing the analog component signals, namely, the luminance signal (Y) and the two color difference signals ($C_R$, $C_B$). The luminance and color difference signals are expressed by the following formulas.

$Y = 0.299R + 0.587G + 0.114B$
$C_R = R\text{-}Y$
$C_B = B\text{-}Y$

The sampling frequency is 13.5 MHz for the luminance signal and 6.75 MHz for the color difference signals, and the sampling point positions on the TV screen appear in the form of a grid. The total number of samples per horizontal line is 1,716 (Y: 858; $C_R/C_B$: 429 each) for a 525/60 system and 1,728 (Y: 864; $C_R/C_B$: 432 each) for a 625/50 system. The total number of samples per digital active line is 1,440 (Y: 720, $C_R/C_B$: 360 each) for both the 525/60 and 625/50 systems.

The 8 bits of a data word are called DATA-0 through DATA-7, with DATA-7 serving as the most significant bit (MSB) and DATA-0 as the least significant bit (LSB). In the 8-bit code, $00_H$ and $FF_H$ are used as the identification code, and they cannot be used in the video data section.

Fig. 1-1-1 shows the relationship between the video signal level and quantizing level.

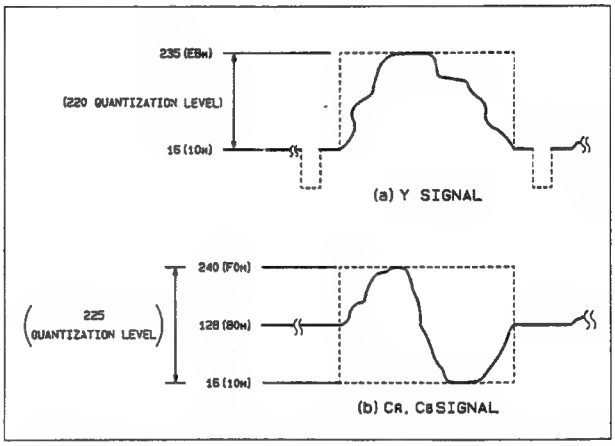



**Fig. 1-1-1. Relationship Between Video Signal Levels and Quantizing Levels**

The digital video data in words of 8 bits each is time-division-multiplexed and sent in the following sequence as 27 M word/sec parallel signal:

$C_B$, Y, $C_R$, Y, $C_B$, Y, $C_R$, Y, ...

The first "$C_B$, Y, $C_R$" are the luminance signal and color difference signal samples at the same position on the screen, and the following "Y" is the adjoining luminance signal sample.

The first video data word of each digital active line is the $C_B$ data.

Fig. 1-1-2 shows the relationship between the analog horizontal synchronization and digital signal, and Fig. 1-1-3 shows the relationship between the analog signal and digital field blanking.

Each digital active line contain the 1,440 time-division-multiplexed luminance and color difference samples. Four-word timing reference signals are added both before and after the digital active lines. This data contains the preamble, line and field reference information.

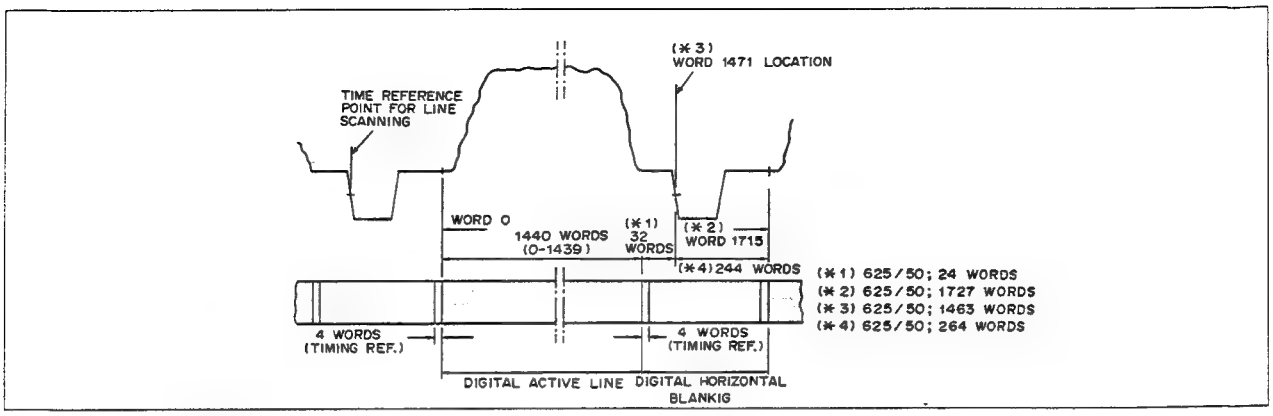



**Fig. 1-1-2. Relationship Between Analog Horizontal Synchronization and Digital Signal**

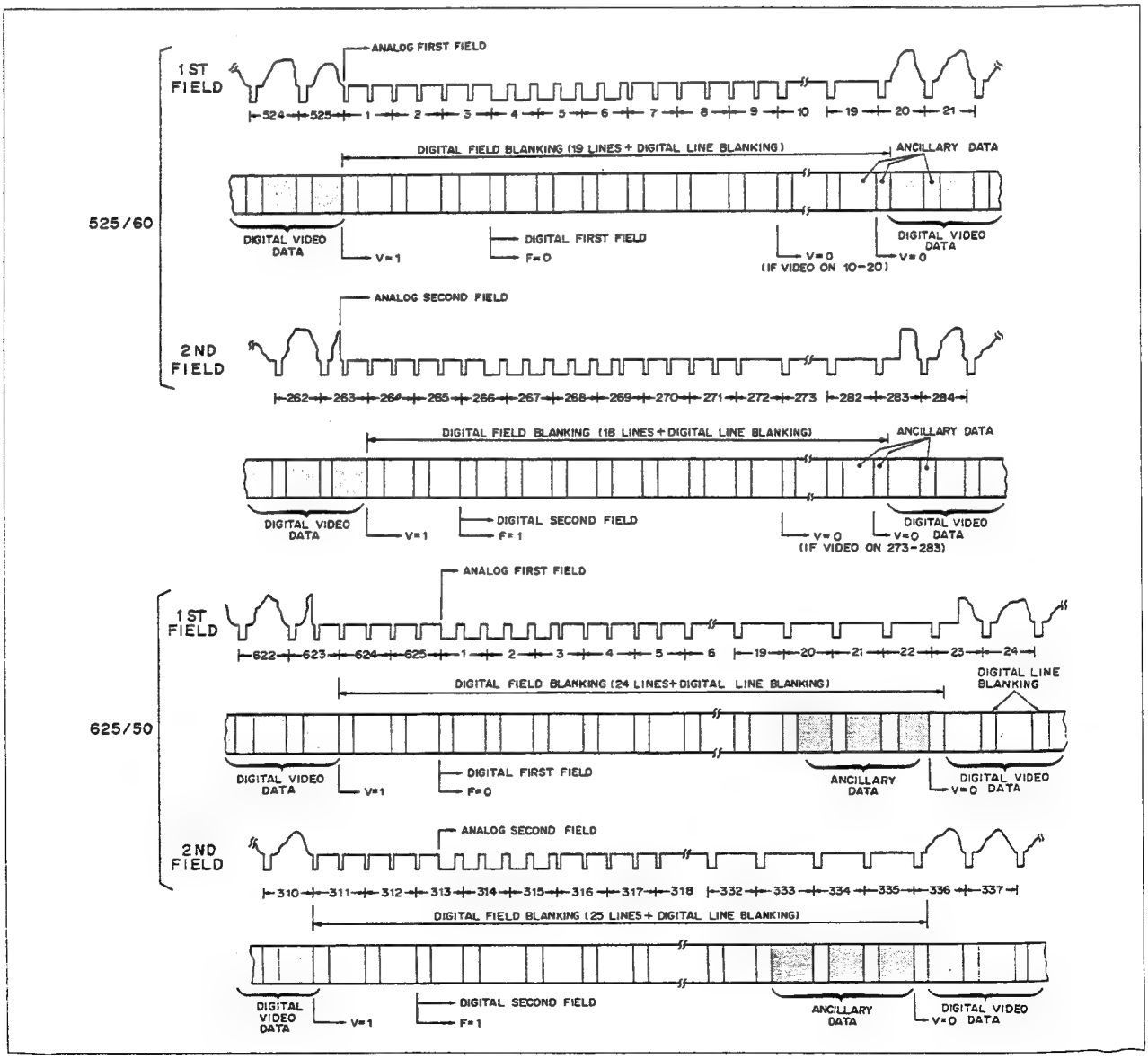



**Fig. 1-1-3. Relationship Between Analog Video Signal and Digital Field Blanking**

**(B) Timing reference signals**

As shown by Figs. 1-1-2 and 1-1-3, 4-word timing reference signals are added both before and after the digital active lines. These signals define the field status and timing of both the vertical and horizontal blanking.

The 4 words at the head of the digital active line define the start of the active line, and they are termed SAV (start of active video). Similarly, the 4 words at the end of the digital active line define the completion of the active line, and they are termed EAV (end of active video). The format for the timing reference is given below in hexadecimal notation:

Timing reference format: FF 00 00 (XY)

The first 3 words ($FF_H$, $00_H$, $00_H$) are a fixed preamble, and the fourth word "XY" defines the field status and indicates the timing of both the vertical and horizontal blanking.

The bits in the fourth word are defined as in Table 1-1-1.

F: This defines the field status: "0" for field 1 sections and "1" for field 2 sections.

V: This defines the vertical blanking timing: "1" for vertical blanking sections.

H: This defines the horizontal blanking timing: "1" for horizontal blanking sections.

P0/P1/P2/P3:

These are the redundant bits. When transmission errors occur in F, V and H, they are used to correct these errors.

| SIGNAL | BIT NUMBER 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | HEX VALUE |
|---|---|---|---|---|---|---|---|---|---|
| PREAMBLE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| TIMING REF. | 1 | F | V | H | P3 | P2 | P1 | P0 | (XY) |

**Table 1-1-1. Timing Reference Signal**

| F | V | H | P3 (V⊕E) | P2 (F⊕H) | P1 (F⊕V) | P0 (F⊕V⊕H) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

⊕=MODULO 2 ADDITION(X-OR)

**Table 1-1-2. P0/P1/P2/P3**

**(C) Ancillary data**

The ancillary data is inserted in the positions shown in Fig. 1-1-3 at a rate of 27 M word/sec. A description of the construction of this data is omitted here.

**(D) Clock signal**

Under the parallel video format, 27 MHz square wave clock signal is sent together with 8 pairs of data signals. In a 525/60 system, there are 1,716 clock intervals for each horizontal line period and in a 625/50 system, there are 1,728 intervals.

The timing relationship between the data and clock signals is regulated so that the clock signal rises in the exact middle of the data.

**(E) Connector**

The connector used with the parallel video interface is a 25-pin D-SUB connector. Table 1-1-3 shows its pin assignment.

| PIN NO. | SYMBOL | PIN NO. | SYMBOL |
|---|---|---|---|
| 1 | CLOCK | 14 | CLOCK (RET) |
| 2 | SYSTEM GND | 15 | SYSTEM GND |
| 3 | DATA-7 (MSB) | 16 | DATA-7 (RET) |
| 4 | DATA-6 | 17 | DATA-6 (RET) |
| 5 | DATA-5 | 18 | DATA-5 (RET) |
| 6 | DATA-4 | 19 | DATA-4 (RET) |
| 7 | DATA-3 | 20 | DATA-3 (RET) |
| 8 | DATA-2 | 21 | DATA-2 (RET) |
| 9 | DATA-1 | 22 | DATA-1 (RET) |
| 10 | DATA-0 (LSB) | 23 | DATA-0 (RET) |
| 11 | — | 24 | — |
| 12 | — | 25 | — |
| 13 | CHASSIS (GND) | — | — |

**Table 1-1-3. Pin Assignment**

**2. Audio interface**

The audio interface is common to both the 525/60 and 625/50 systems. Two-channel multiplex digital audio signals are sent from the transmitting side to a single or multiple number of receiving sides. The digital signals are sent in a single balanced twisted pair cable.

The send data is composed of the following data:

- Preamble data
- Audio data
- Channel status data
- User data
- Parity and validity data

These signals undergo time division multiplexing and bi-phase mark coding, and are transmitted.

**(A) Audio encoding parameters**

Sampling frequency: 48 kHz

Form of Coding:

Linear quantizing, 2's complement code, Max. 24 bits per sample

Data rate: 3.072 Mb/s

= 48 kHz x 2 (channel) x 32 (bits)

Status data: 48 kb/s, aligned in 192 bit blocks

User data: 48 kb/s

**(B) Frame and subframe format**

The subframes are composed of 32-bit data which consists of the one audio sample and other information from one of the two channels. They are designated as A and B. When operating in the stereo mode, subframe A includes the information of the left channel and subframe B includes the information of the right channel. Subframe A and subframe B together form one frame and, as shown in Fig. 1-1-4, this is sent during an audio sample period.

**(C) Preamble**

The subframes include the preamble which regulates the subframe and frame synchronization and identification. The digital audio data first undergoes biphase mark coding and is then sent, but the preamble waveforms do not conform to this rule in that the preamble section can be accurately detected at the receiving side. There are 3 types of preamble waveforms, as shown by Fig. 1-1-5.

Preamble 1:

This specifies the subframe A start, namely the frame start, and also the start of the channel status data block.

Preamble 2:

This specifies the subframe A start, namely the frame start.

Preamble 3:

This specifies the subframe B start.

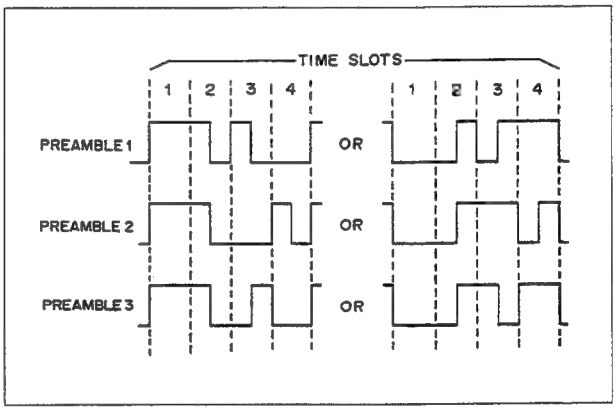



**Fig. 1-1-5. Preamble Waveforms**

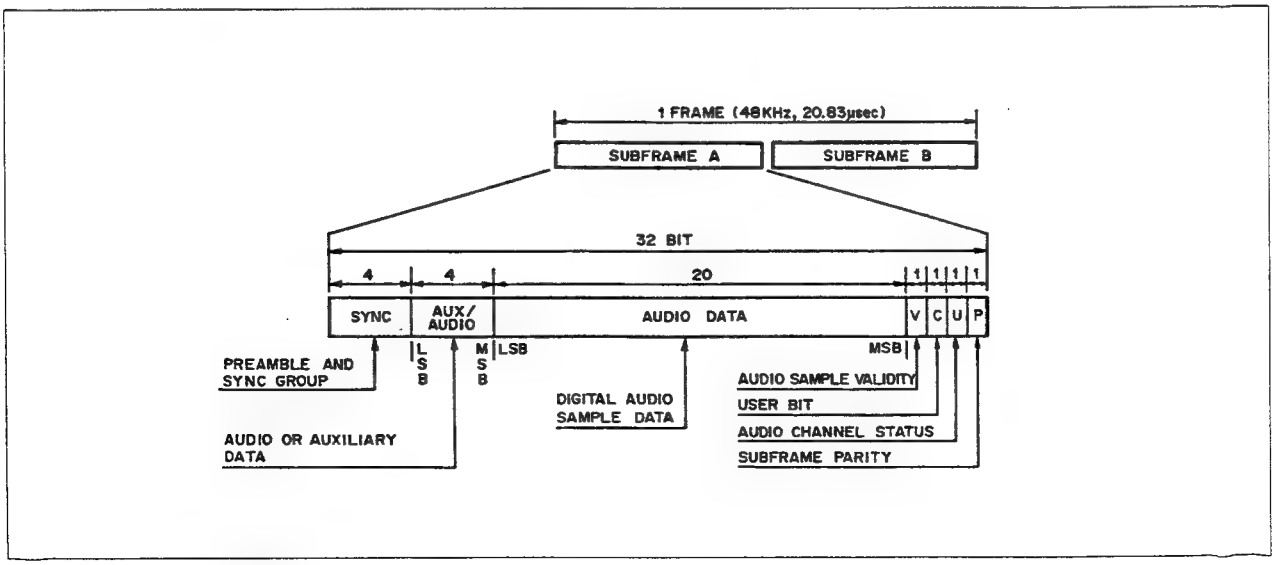



**Fig. 1-1-4. Frame and Subframe Formats**

**(D) Audio data**

Up to 24 bits can be used as the audio data. When 20 bits are used as the audio data, the ancillary data can be inserted into the first (least significant) 4 bits. When sending audio data of under 20 bits, the bits not used (least significant) bits are set to "0."

**(E) Audio sample validity bit**

This bit indicates the validity of the audio data. "0" is sent with valid data; "1" is sent with invalid data.

**(F) User bit**

This bit sends the data which has been defined by the user. As with the channel status data, it can also employ a block construction. For further details, refer to the section on the channel status block format.

**(G) Channel status bit**

The channel status bit configures the data block and sends the transmit information concerning the interface channel and the other system parameters.

For each channel, a single block is formed by the channel status bits included in 192 continuous frames. The start position of the block is designated by the above-mentioned preamble 1.

**(H) Parity bit**

The even parity for all data in the subframes except the preamble is inserted in this bit.

**(I) Channel status block format**

A data block is formed by the channel status bits (or user bits) in 192 continuous frames. This means that the block size is 192 bits (24 bytes). The blocks correspond to the names of the subframes and are called block A and block B. The block start is defined by the above-mentioned preamble 1.

Table 1-1-4 shows how the channel status data is configured.

| Byte | Bit | Definition |
|---|---|---|
| 0 | 0 | 0: Consumer use　1: Professional use |
| | 1 | 0: Normal audio mode　1: Non-audio mode |
| | 2, 3, 4 | 000: Manual emphasis　100: No emphasis　110: CD emphasis　111: CCITT emphasis |
| | 5 | 1: Source sampling frequency unlocked.　0: Source sampling frequency locked. |
| | 6, 7 | 00: Sampling frequency not indicated. Receiver default to 48KHz, manual override enabled.<br>01: 48kHz sampling frequency　10: 44.1kHz sampling frequency　11: 32kHz sampling frequency |
| 1 | 0 | 00: Default to two-channel mode. Manual override enabled.　01: Two-channel mode |
| | 1 | 00: Single channel (monophonic) mode　01: Primary/secondary mode (Channel 1 is primary)　10: Stereo phonic mode (Channel 1 is left channel) |
| | 2, 3, 4, 5, 6, 7 | Reserved but undefined. |
| 2 | 0, 1, 2 | 000: AUX sample bits use not defined. Audio sample data is 20 bits.　001: Audio sample data is 24 bits. |
| | 3, 4, 5, 6, 7 | Reserved but undefined. |
| 22 | 0, 1, 2, 3 | Reserved but undefined. Set to zero. |
| | 4 | 1: Bytes 0 - 5 are unreliable.　0: Reliable |
| | 5 | 1: Bytes 6 - 13 are unreliable.　0: Reliable |
| | 6 | 1: Bytes 14 - 17 are unreliable.　0: Reliable |
| | 7 | 1: Bytes 18 - 21 are unreliable.　0: Reliable |
| 23 | 0 to 7 | CRCC (cyclic redundancy check code)<br>Initial value of CRC generating register is all 1s.<br>Generating polynomial is : $G(x) = X^5+X^4+X^3+X^2+1$ |

**Table 1-1-4. Channel Status Data**

## 4-1-2. Program Track

Fig. 1-2-1 shows the tape format.
As shown by the figure, the tape format is composed of three longitudinal tracks (cue audio, CTL and time code tracks) and helical tracks called the "program tracks" which contain the digital video and digital audio data.

Under the D-1 format, a segmented format is adopted which records the fields onto a number of parallel and neighboring helical tracks. Each field is recorded onto 10 tracks with the 525/60 system and 12 tracks with the 625/50 system.
The following description divides the program tracks into video and audio tracks.

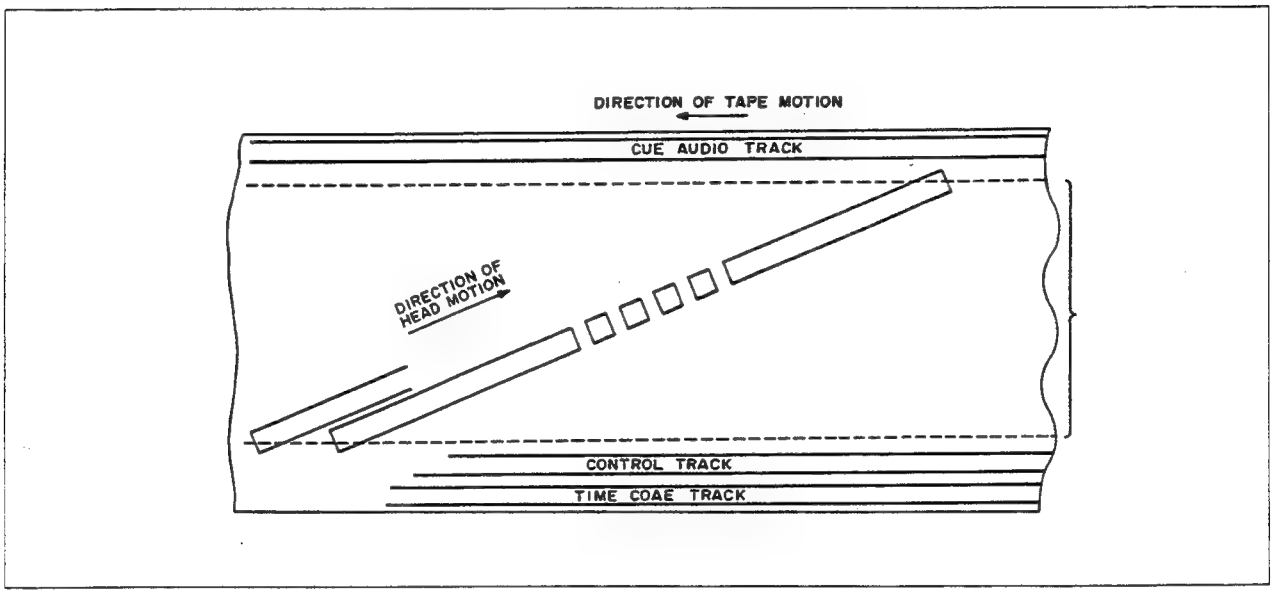



**Fig. 1-2-1. Tape Format**

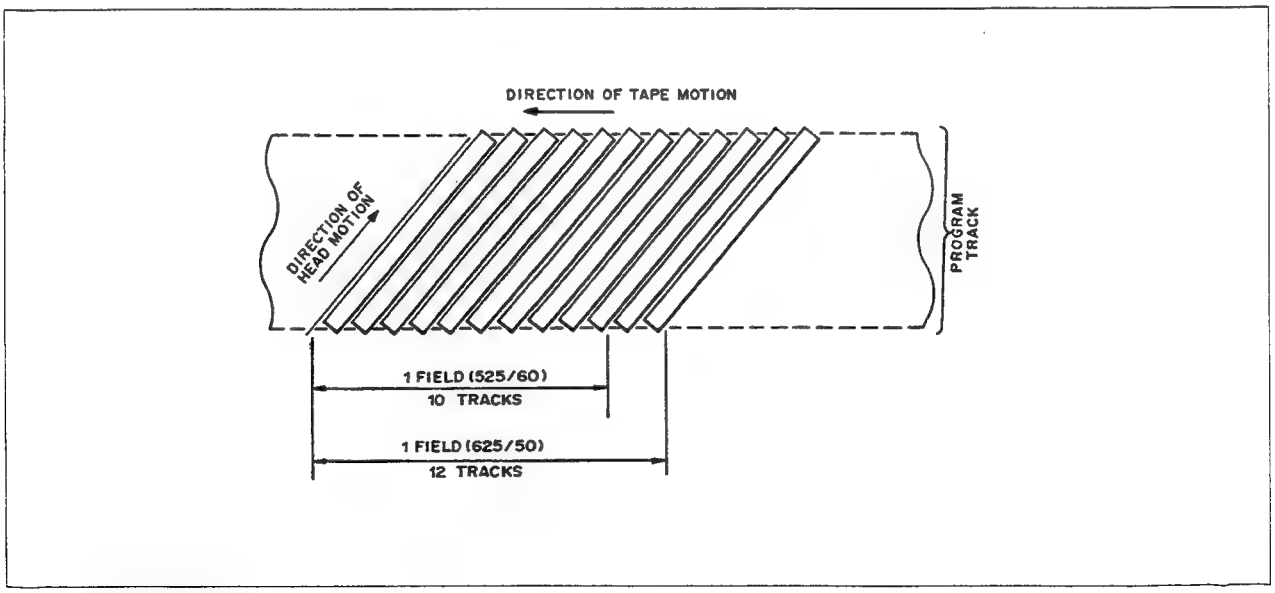



**Fig. 1-2-2. Basic Program Track Format**

**1. Video program tracks**

Under the D-1 format, the data of one video segment is distributed over 4 tracks for each sample and recorded. The number of tracks per field must be a multiple of 4 in order for recording and editing to be conducted field by field. Consequently, each program track is divided into two, and 20 half tracks per field are aligned for the 525/60 system and 24 half tracks are aligned for the 625/50 system.

Each half tracks is called a sector, and one video segment is composed of 4 sectors which have been recorded by separate heads. A video segment includes all the video information for 50 lines in the video signal.

**2. Audio program tracks**

The audio tracks are positioned in the center of the program tracks, as shown by Fig. 1-2-4. This not only protects the tape edge from damage but also safeguards againt tracking errors caused by skew errors.

The audio track sectors and segments are positioned in the same way as with the video tracks. One audio segment contains 6.66 milliseconds of digital audio data. This is equivalent to one-fifth of a video frame for the 525/60 system and one-sixth for the 625/50 system.

For each audio channel, one audio segment is composed of 4 audio sectors positioned between 4 neighboring program tracks. Each of the 4 sectors contains either odd- or even-numbered audio samples. This means that two sectors contain all the data required for 6.66 milliseconds. Duplicate data is recorded in the other two sectors in order to enhance the error correction capability.

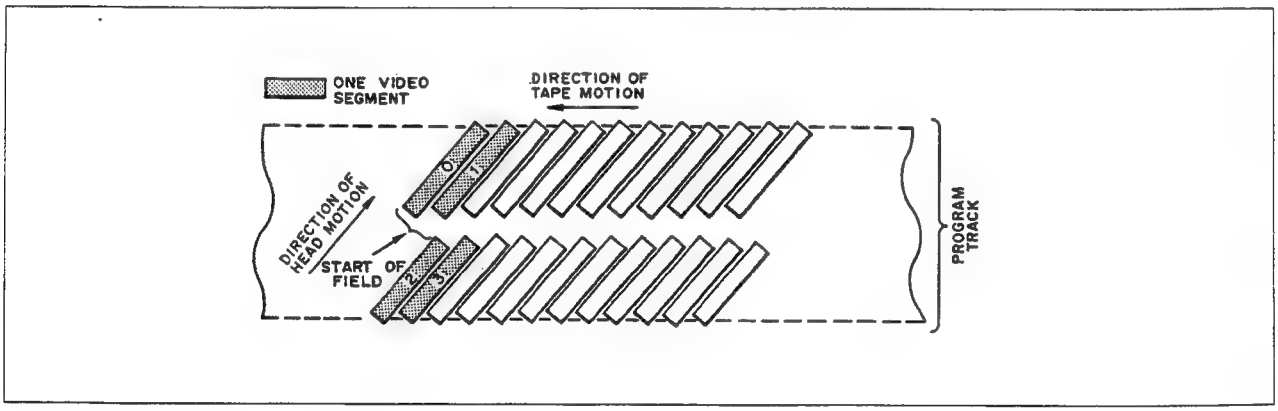



**Fig. 1-2-3. Video Sectors and Segments**

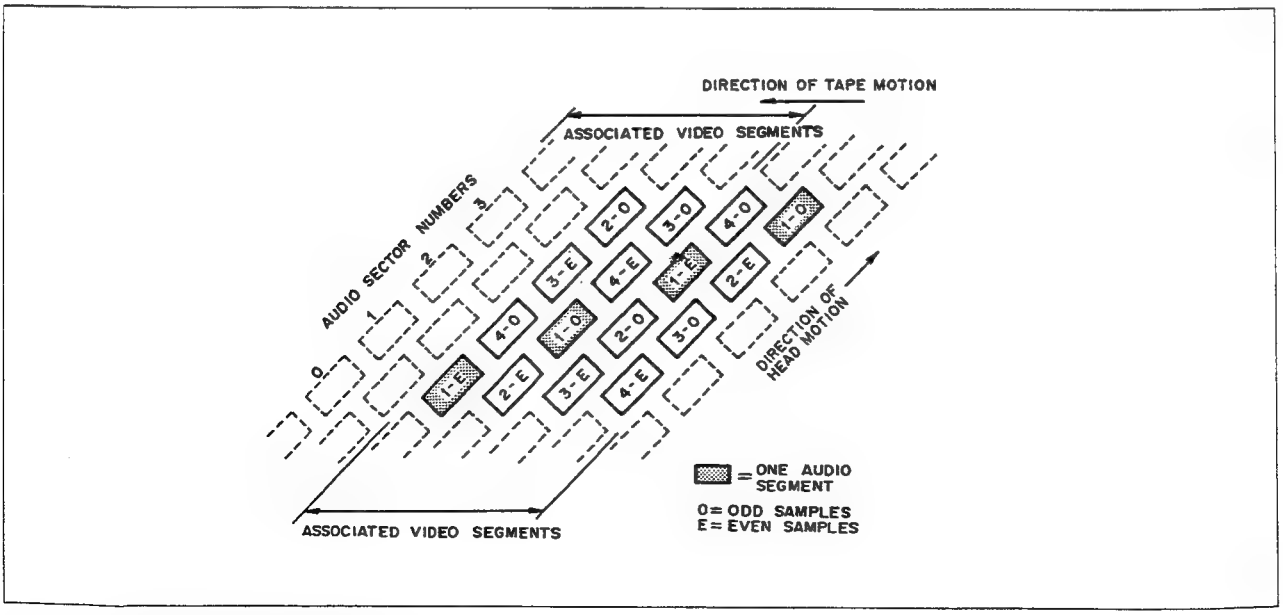



**Fig. 1-2-4. Audio Sectors and Segments**

### 3. Program track data contents

Fig. 1-2-5 show the contents of the program tracks. The data which configures the program tracks will now be described.

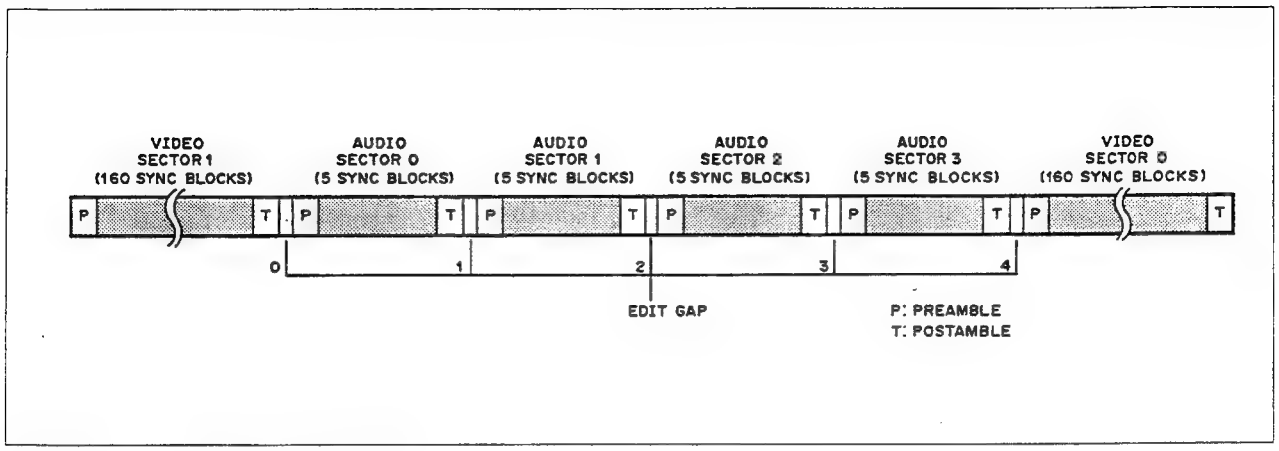



**Fig. 1-2-5. Contents of Program Tracks**

#### (A) Sync blocks

A sync block is the basic unit of a video and audio program track. The video and audio sectors are composed of 160 and 5 sync blocks, respectively.

Each sync block contains a sync pattern (2 bytes), block identifier (ID 4 bytes), and two inner code blocks consisting of 60 bytes of video or audio data together with related R-S correction codes (4 bytes).

#### (B) Sync pattern

The sync pattern defines the start of the sync blocks during playback. If this is expressed by the sequence in which they are recorded onto tape, the sync pattern will be "0CAF$_H$."

| | | | | |
|---|---|---|---|---|
| (Hexadecimal) | 0 | C | A | F |
| (Binary) | 0000 | 1100 | 1010 | 1111 |
| | –Byte 0– | | –Byte 1– | |

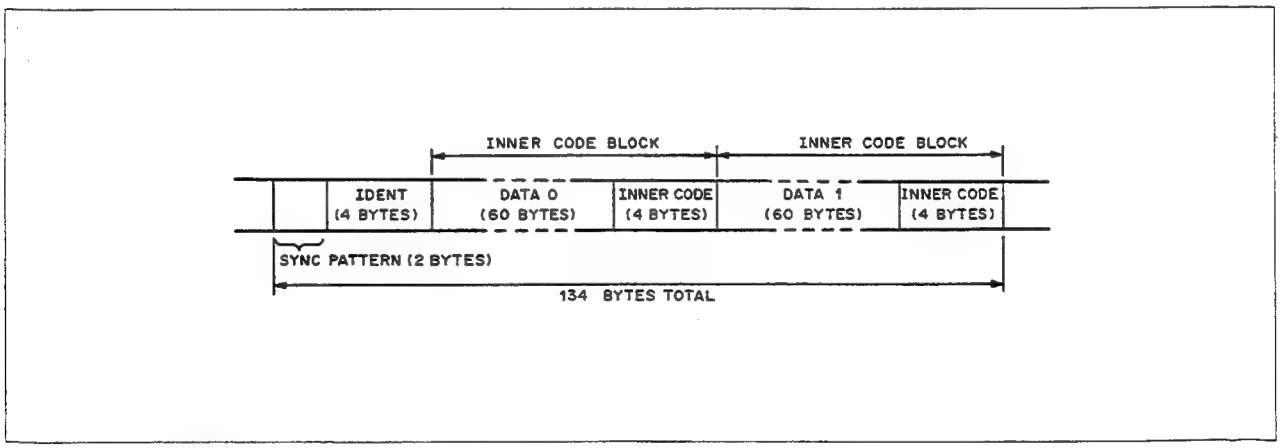



**Fig. 1-2-6. Sync Block**

**(C) Identification pattern (ID)**

The sync blocks in 4 fields are addressed by the 4-byte identification pattern (ID). This enables the data samples to be positioned properly on the monitor during operations in the shuttle and other modes.

The identification pattern is expressed by four 4-bit nibbles and these are mapped respectively into 8-bit data. Fig. 1-2-7 shows the identification pattern prior to mapping. Table 1-2-1 is the mapping table.

The sync block ID numbers the sync blocks along the program tracks. The sector ID, segment ID and field ID number the sync blocks in accordance with their respective positions.

| INPUT (ID NIBBLE) | OUTPUT (ID BYTE) | INPUT (ID NIBBLE) | OUTPUT (ID BYTE) |
|---|---|---|---|
| 0 | 1B | 8 | 96 |
| 1 | 2E | 9 | A3 |
| 2 | 35 | A | B8 |
| 3 | 47 | B | CA |
| 4 | 5C | C | D1 |
| 5 | 69 | D | E4 |
| 6 | 72 | — | — |
| 7 | 8D | — | — |

**Table 1-2-1. ID Word Mapping**

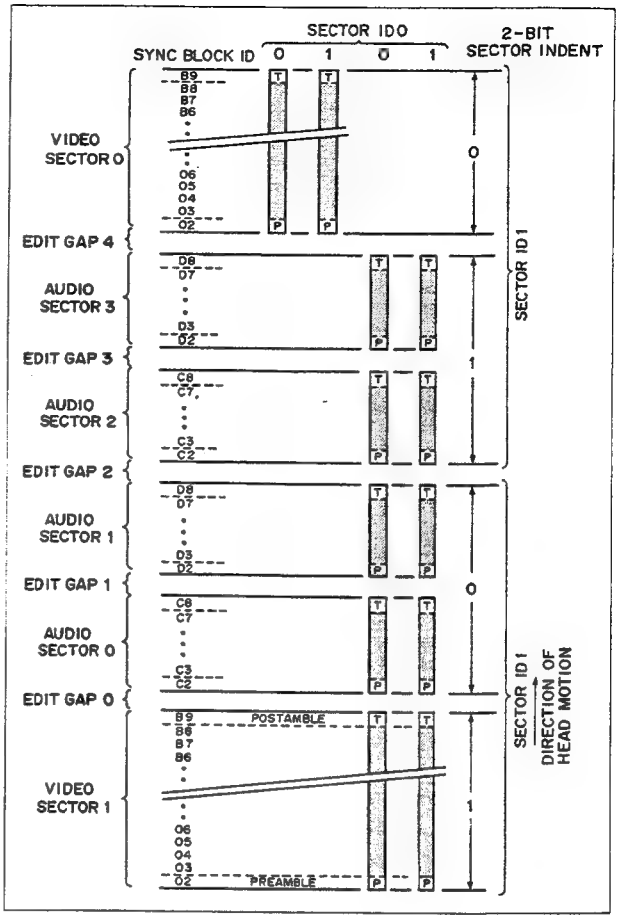



**Fig. 1-2-8. Sync Block ID and Sector ID**

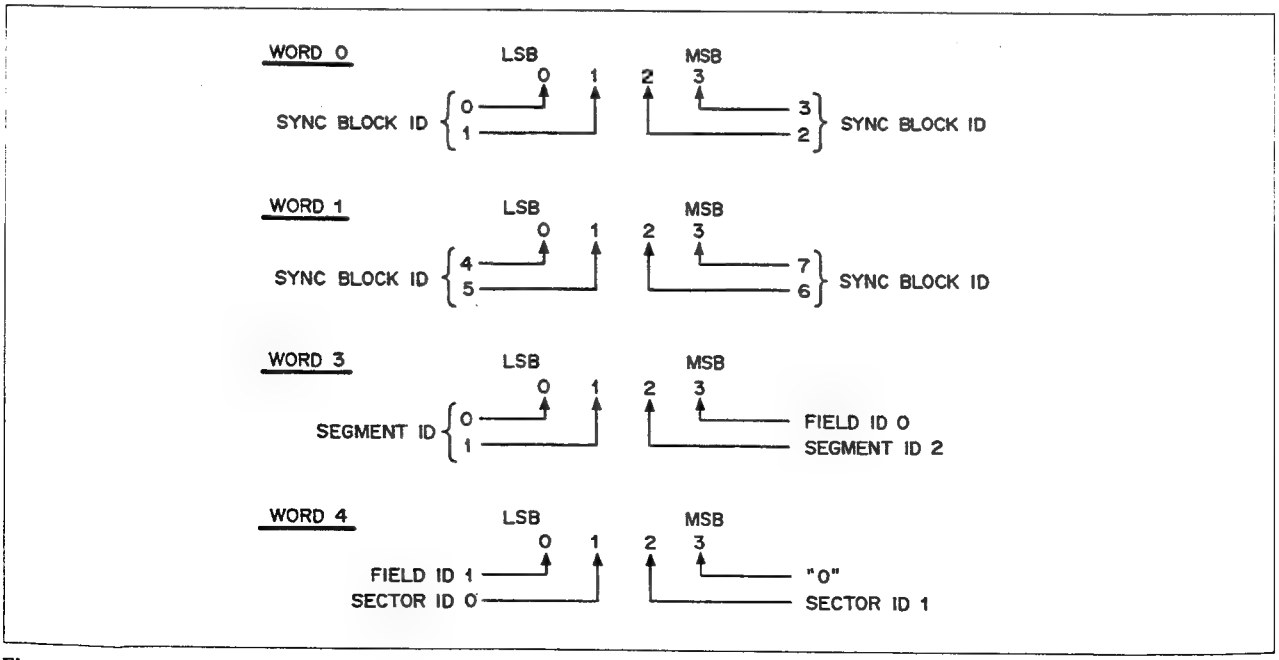



**Fig. 1-2-7. ID Pattern**

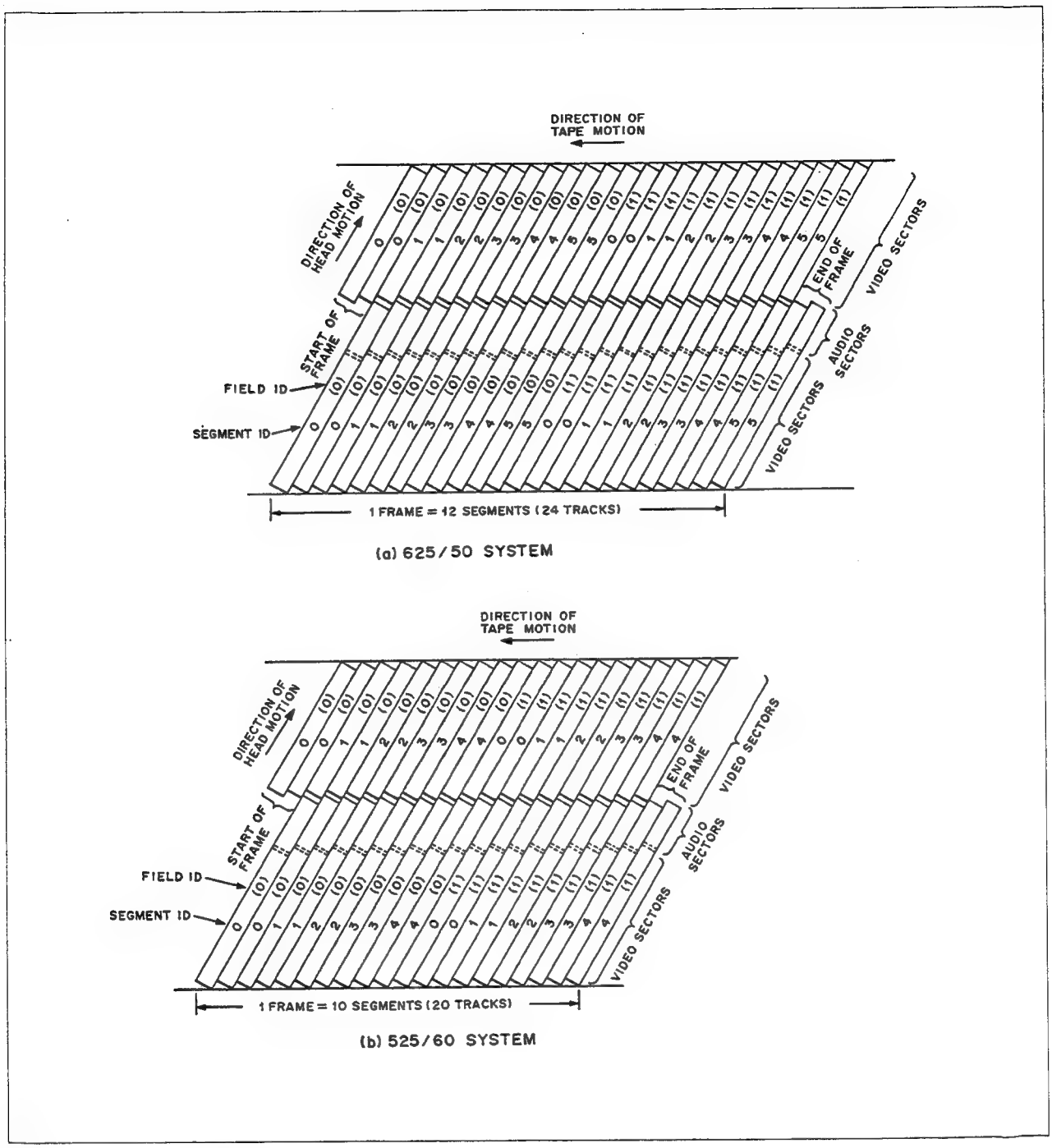



**Fig. 1-2-9. Field ID and Segment ID**

**(D) Preamble**

As shown by Fig. 1-2-5, all sectors start with the preamble sequence. Each preamble is composed of 30 bytes of data. The sync pattern and identification pattern (ID) are the same as what was described in sections (B) and (C).

"$CC_H$" equivalent to 20 bytes and 4 bytes is inserted respectively into the run-up section and fill data section.

**(E) Postamble**

As shown by Fig. 1-2-5, all sectors are completed with a postamble. The postamble is composed of 6 bytes of data, two bytes of which constitute the sync pattern and the remaining 4 bybtes of which constitute the identification pattern (ID). These are the same as what was described in sections (B) and (C).

**(F) Edit gaps**

Edit gaps are inserted between each sector of the program tracks. They are provided for timing errors during recording and are composed of fill data ($CC_H$) equivalent to 232 bytes.

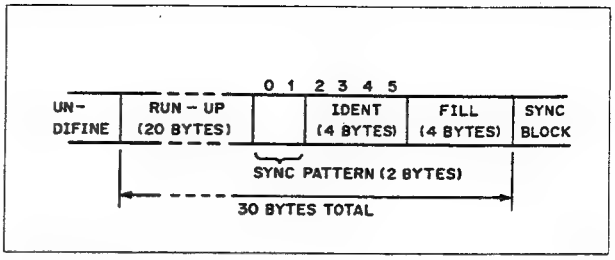



**Fig. 1-2-10. Preamble**

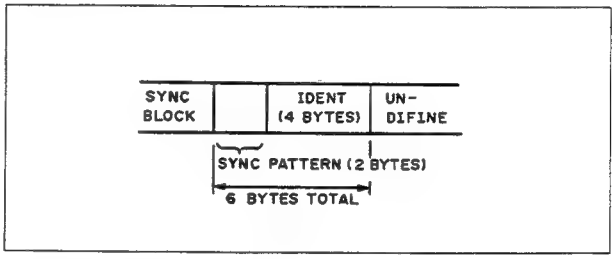



**Fig. 1-2-11. Postamble**

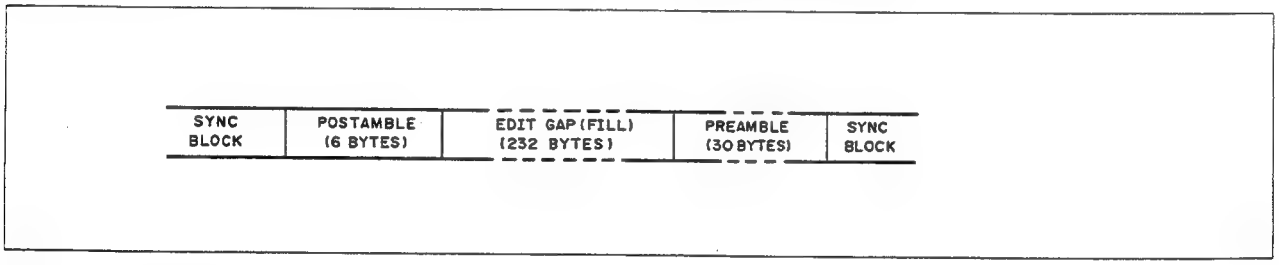



**Fig. 1-2-12. Edit Gap**

## 4-1-3. Video Signal Processing

This section gives an outline of the digital video signal processing based on the D-1 format.

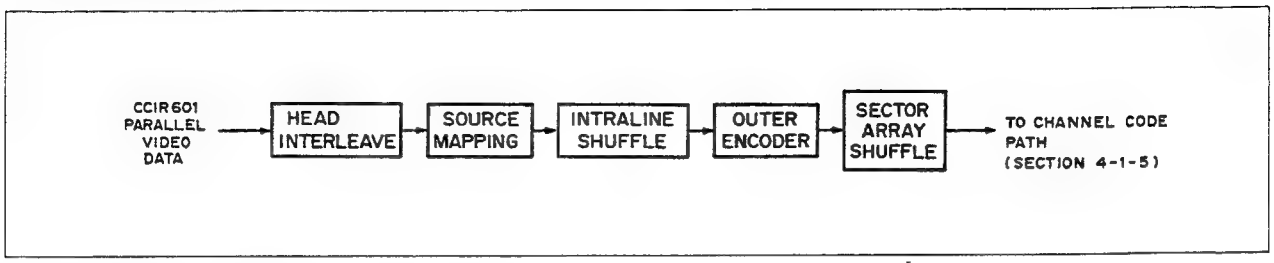



**Fig. 1-3-1. Outline of Video Signal System Processing**

**(A) Input data**

The video signals are supplied to the signal processor circuit under the parallel video interface format described in section 4-1-1.

With a 525/60 system, 250 lines are recorded for each field: lines 14 through 263 for field 1 and lines 276 through 525 for field 2. However, digital active video does not exist for all the lines and so only lines 21 through 263 in field 1 and lines 283 through 525 in field 2 are the subject of mapping and concealment.

With a 625/50 system, 300 lines are recorded for each field: lines 11 through 310 for field 1 and lines 324 through 623 for field 2. In this case, only lines 23 through 310 in field 1 and lines 336 through 623 in field 2 are the subject of mapping and concealment.

In each line, only 1, 440 bytes of data in the digital active video are recorded.

**(B) Head interleaving**

The input data is divided into 4 processing channels (heads). this brings the number of samples per line for each channel to 360 (1,440 divided by 4).

The video data is distributed evenly by this process to the 4 sectors which configure the video segment. This is why the process is called intersector shuffling. Even when a head is clogged, this process prevents all the data around the error data from being set to the error status when the samples are re-configured properly during playback. It enables the error concealment circuit to replace or interpolate the invalid (error) data with the surrounding valid data.

The way in which the data is distributed differs according to the segment numbers, field numbers and even/odd lines. For further details, refer to Section 4-2-5 on the VE-12 board.

| MS WORD (4 BITS) \ INPUT | LS WORD (4 BITS) 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 00 | 80 | 40 | 20 | 10 | 08 | 04 | 02 | 01 | C0 | A0 | 90 | 88 | 84 | 82 | 81 |
| 1 | 60 | 50 | 48 | 44 | 42 | 41 | 30 | 28 | 24 | 22 | 21 | 18 | 14 | 12 | 11 | 0C |
| 2 | 0A | 09 | 06 | 05 | 03 | E0 | D0 | C8 | C4 | C2 | C1 | B0 | A8 | A4 | A2 | A1 |
| 3 | 98 | 94 | 92 | 91 | 8C | 8A | 89 | 86 | 85 | B3 | 70 | 68 | 64 | 62 | 61 | 58 |
| 4 | 54 | 52 | 51 | 4C | 4A | 49 | 46 | 45 | 43 | 38 | 34 | 32 | 31 | 2C | 2A | 29 |
| 5 | 26 | 25 | 23 | 1C | 1A | 19 | 16 | 15 | 13 | 0E | 0D | 0B | 07 | F0 | E8 | E4 |
| 6 | E2 | E1 | D8 | D4 | D2 | D1 | CC | CA | C9 | C6 | C5 | C3 | B8 | B4 | B2 | B1 |
| 7 | AC | AA | A9 | A6 | A5 | A3 | 9C | 9A | 99 | 96 | 95 | 93 | 8E | 8D | 8B | 87 |
| 8 | 78 | 74 | 72 | 71 | 6C | 6A | 69 | 66 | 65 | 63 | 5C | 5A | 59 | 56 | 55 | 53 |
| 9 | 4E | 4D | 4B | 47 | 3C | 3A | 39 | 36 | 35 | 33 | 2E | 2D | 2B | 27 | 1E | 1D |
| A | 1B | 17 | 0F | F8 | F4 | F2 | F1 | EC | EA | E9 | E6 | E5 | E3 | DC | DA | D9 |
| B | D6 | D5 | D3 | CE | CD | CB | C7 | BC | BA | B9 | B6 | B5 | B3 | AE | AD | AB |
| C | A7 | 9E | 9D | 9B | 97 | 8F | 7C | 7A | 79 | 76 | 75 | 73 | 6E | 6D | 6B | 67 |
| D | 5E | 5D | 5B | 57 | 4F | 3E | 3D | 3B | 37 | 2F | 1F | FC | FA | F9 | F6 | F5 |
| E | F3 | EE | ED | EB | E7 | DE | DD | DB | D7 | CF | BE | BD | BB | B7 | AF | 9F |
| F | 7E | 7D | 7B | 77 | 6F | 5F | 3F | FE | FD | FB | F7 | EF | DF | BF | 7F | FF |

**Table 1-3-1. Source Mapping Table**

**(C) Source mapping (8-8 mapping)**

The input video data is mapped on a 1:1 basis in accordance with the mapping table shown by Table 1-3-1.

When a bit error has arisen in the two most significant bits of the video data, an error will result in the 128 or 64 quantizing level, respectively. This process is designed to reduce the peak errors which are caused by bit errors.

**(D) Intraline shuffling**

The above-mentioned head interleaving process brings the number of samples for one line of each channel to 360. This total breaks down into 90 samples each for the $C_B$, $C_R$, Y even samples and Y odd samples.

Intraline shuffling serves to re-arrange the 360 samples in a line into groups of 30 samples, namely into $30C_B$, $30C_R$, etc. This is because the 2-byte correction code generated by the outer encoder described next is related only to samples of the same type.

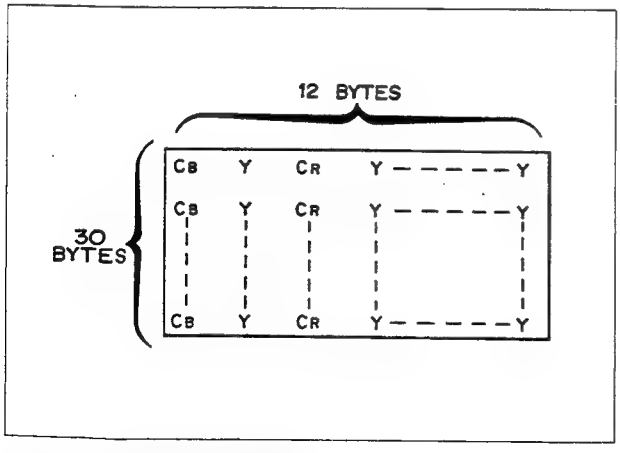



**Fig. 1-3-2. Intraline Shuffling**

**(E) Outer encoding**

The 2-byte Reed Solomon (R-S) correction code is added to each group of 30 bytes which have been re-arranged by Intraline shuffling, and 32-byte video outer code blocks are formed.

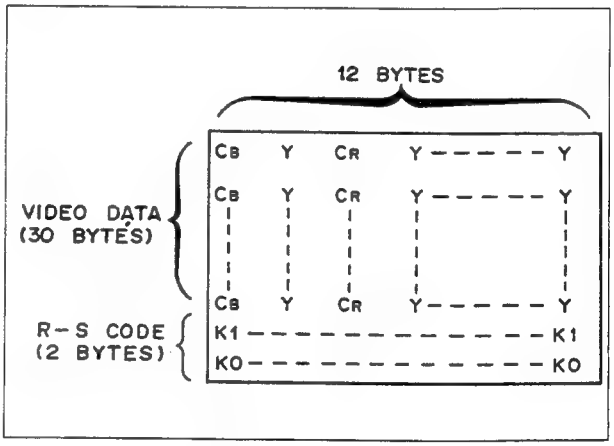



**Fig. 1-3-3. Outer Encoding**

**(F) Sector array shuffling**

The video data and outer correction code are re-arranged, and product blocks are generated to which the inner correction code is added.

Each video sector contains 18,000 bytes (50 x 1,440/4, see *1) of video data.

The outer correction code is then added to the sectors so that each sector has a total of 19,200 bytes of data, and the sector array is composed of 600 columns by 32 rows. This is divided down to create 10 product block arrays composed of 60 columns by 32 rows. Fig. 1-3-4 shows the configuration of a video product block.

As shown in the figure, the outer correction code is shuffled with the video data. In other words, all $C_B$, $C_R$ or Y samples and the outer correction code are re-positioned according to definite rules, and the samples in the same screen area are separated inside the product block array.

*1 50 = Number of lines per video segment
1440 = Number of samples in digital active line
4 = Number of data processing channels

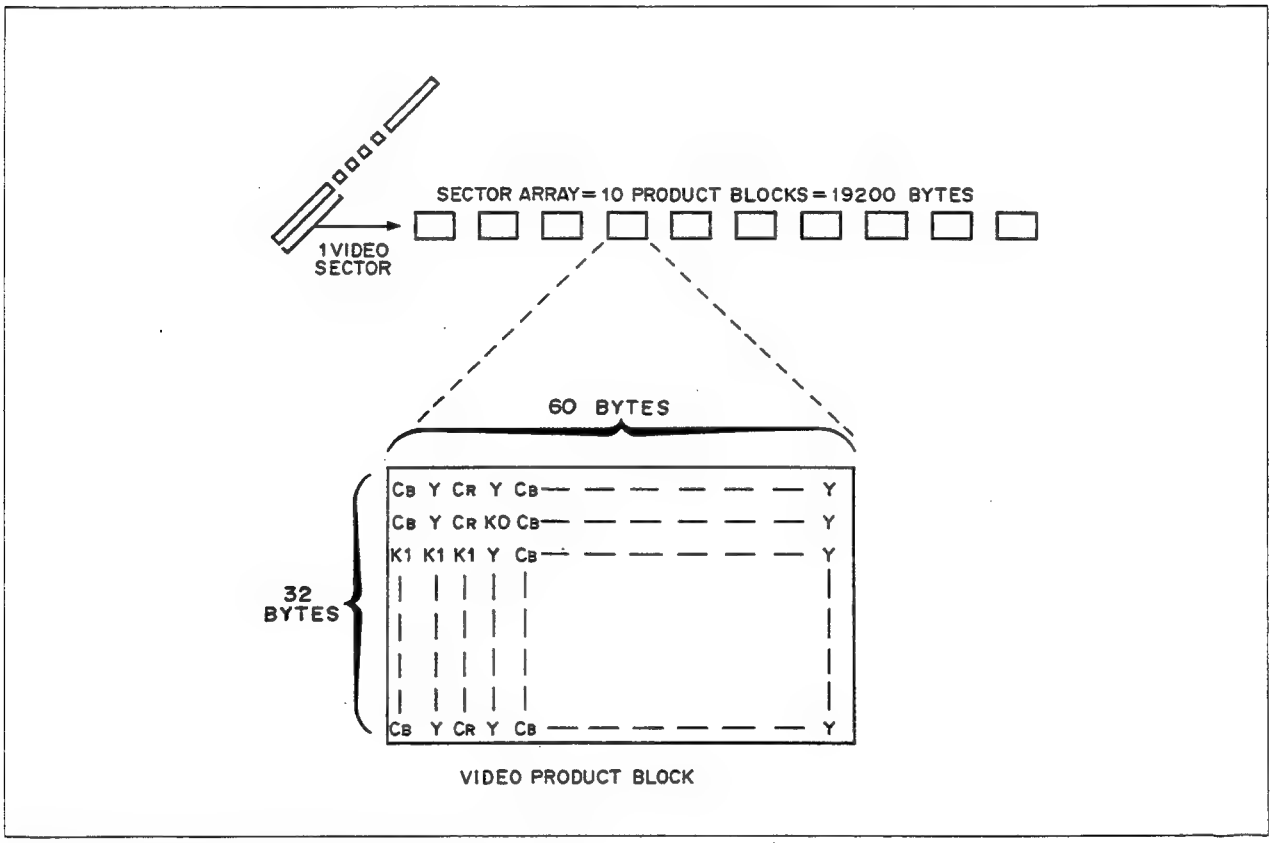



**Fig. 1-3-4. Product Block Array (Sector Array Shuffling)**

## 4-1-4. Audio Signal Processing

This section gives an outline of the digital audio signal processing based on the D-1 format.

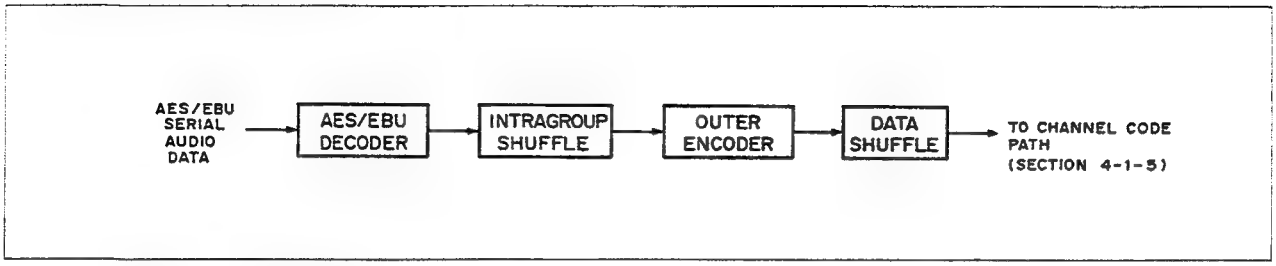



**Fig. 1-4-1. Outline of Audio Signal System Processing**

**(A) Input data**

The audio data is supplied in the AES/EBU format described earlier.

An audio data word is composed of 20 bits. Under the D-1 format, the configuration of a word (20 bits) can be set to any of 8 different modes, as shown by Table 1-4-1. The audio data length is set between 16 and 20 bits. The ancillary bits among the input data are inserted in the other bits.

The setting status of the audio word mode is written into the audio product block as audio word length data "LNGH."

| MODE | LNGH 3 | LNGH 2 | LNGH 1 | AUDIO LENGTH | ANCILLARY BITS C | U | V | R |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 16 BITS | X | X | X | X |
| 1 | 0 | 0 | 1 | 17 BITS | X | X | X | — |
| 2 | 0 | 1 | 0 | 18 BITS | X | — | X | — |
| 3 | 0 | 1 | 1 | 18 BITS | X | X | — | — |
| 4 | 1 | 0 | 0 | 19 BITS | X | — | — | — |
| 5 | 1 | 0 | 1 | 19 BITS | — | — | X | — |
| 6 | 1 | 1 | 0 | 19 BITS | — | X | — | — |
| 7 | 1 | 1 | 1 | 20 BITS | — | — | — | — |

CHANNEL STATUS
USER DATA
VALIDITY BIT
RESERVED

**Table 1-4-1. Audio Word Modes**

**(B) Intragroup shuffling**

The input data is divided into two blocks of odd and even samples which are respectively arranged as shown in Fig. 1-4-2.

The audio data (20 bits) is further divided into 4-bit nibbles and sent to the outer encoder.

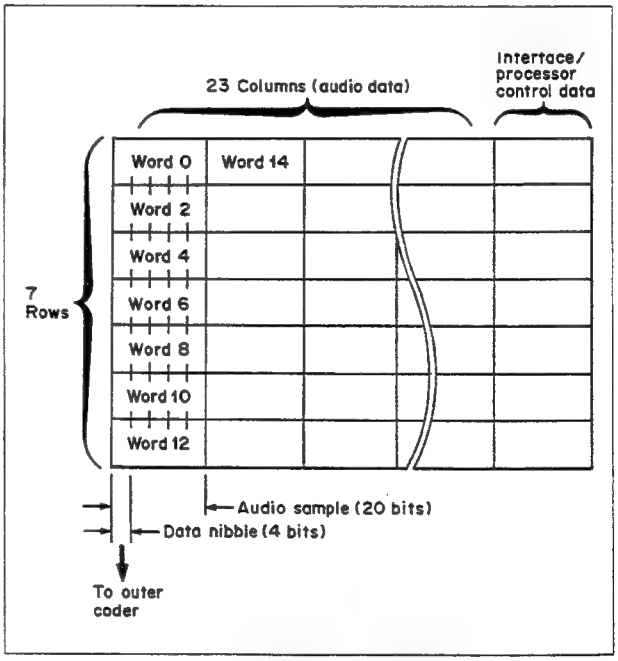



**Fig. 1-4-2. Intragroup Shuffling (Even Samples)**

**(C) Outer encoding**

The three 4-bit nibble R-S correction code is added to the columns composed of seven 4-bit nibbles in the outer encoder, making a total length of 10 columns.

During playback, the error position is provided by the inner code and so errors in a maximum of 3 nibbles in a column can be corrected by the outer code.

**(D) Data shuffling**

The audio data and R-S correction code are re-arranged for each audio sector, as shown in Fig. 1-4-4, to form the audio product block array.

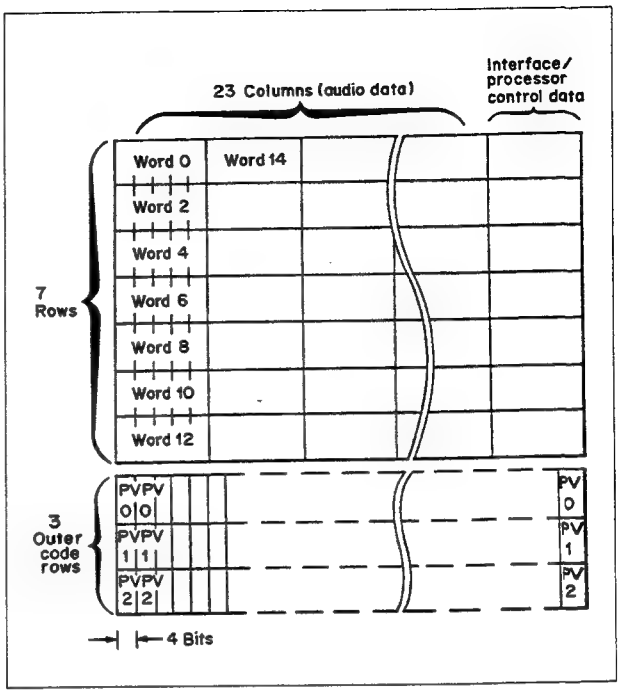



**Fig. 1-4-3. Addition of Outer Correction Code**

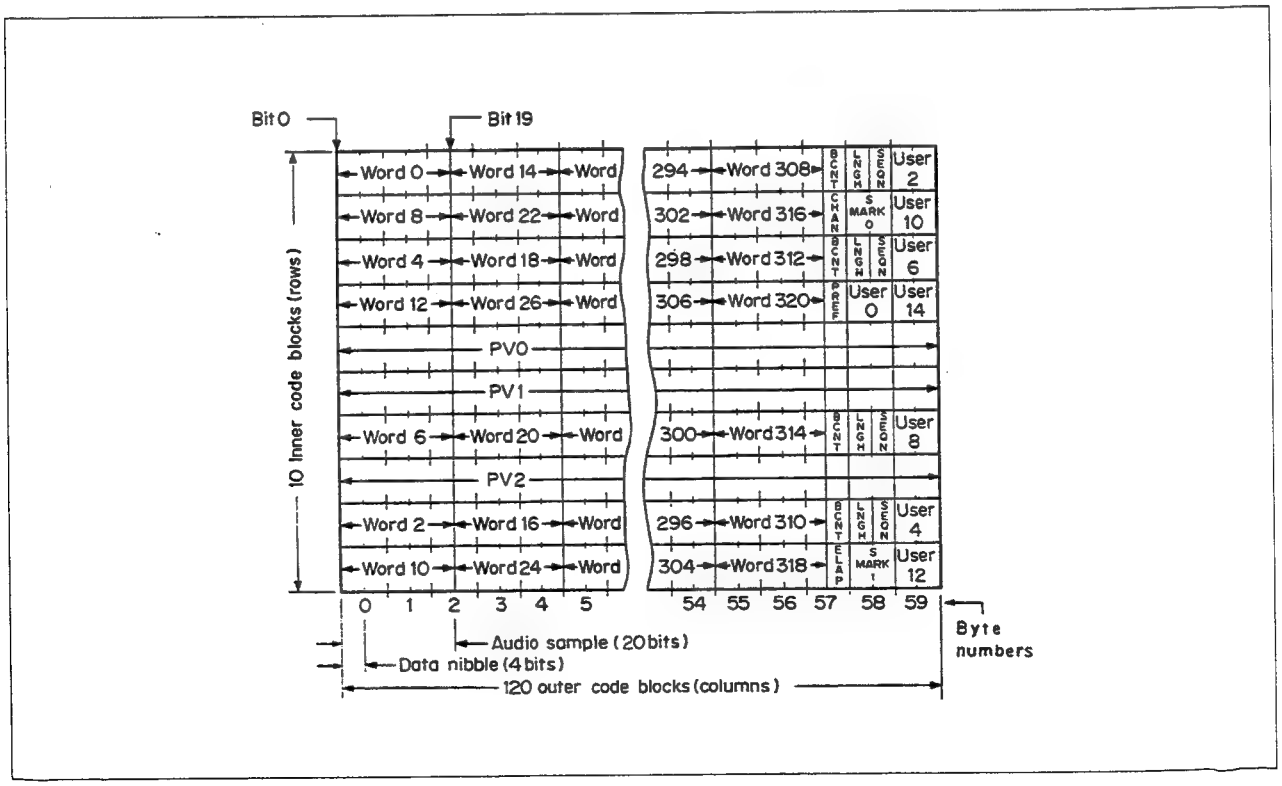



**Fig. 1-4-4. Audio Product Block Layout**

**(E) Control words**

The control words are inserted into the audio product block. This data is created either from the input data or by selection performed by the user. There are 3 types of control words: the interface control word (ICW), processing control word (PCW) and user control word (UCW).

**Interface control word**

- Channel use (CHAN)
  This designates the channel mode. Bits 0, 1, 2 and 3/byte 1 of the channel status data are inserted.
- Pre-emphasis (PREF)
  This instructs whether pre-emphasis is to be used or not. When it is used, it instructs the type of pre-emphasis. Bits 2, 3, and 4/byte 0 of the channel status data are inserted.
- Audio word length (LNGH)
  This specifies the audio word length and also the C, U, V and R allocation. This data is specified by the user. For further details, refer to (A) input data.
- Block sync position (S MARK 0, S MARK 1)
  S MARK 0 gives the word address of the head data in the AES/EBU block which has appeared first in the product block. S MARK 1 gives the word address of the head data in the AES/EBU block which has appeared last in the product block.
  AES/EBU block synchronization normally arises only in an odd or even product block. S MARK 0 and 1 are set to "$AA_H$" for sectors which do not include block synchronization.

**Processing control words**

- Word count (BCNT)
  The data related to the audio sample number in the audio product block is inserted.
  Bit-0, 1: Audio sample number in product block
  Bit-1...Bit-0... Sample number
  ... 0 ... 1 : 159
  ... 0 ... 0 : 160
  ... 1 ... 0 : 161
  ... 1 ... 1 : Illegal
  Bit-2: 0: Synchronous; 1: asynchronous
  Bit-3: Scanning line system 0: 525/60, 1: 625/50

| FRAME NO. | SEGMENT NO. | AUDIO SAMPLE COUNT | | |
|---|---|---|---|---|
| | | EVEN BLOCK | ODD BLOCK | FRAME |
| 0 | 00 | 160 | 160 | 1602 |
| | 01 | 161 | 160 | |
| | 02 | 160 | 160 | |
| | 03 | 161 | 160 | |
| | 04 | 160 | 160 | |
| 1 | 05 | 160 | 160 | 1601 |
| | 06 | 160 | 160 | |
| | 07 | 161 | 160 | |
| | 08 | 160 | 160 | |
| | 09 | 160 | 160 | |
| 2 | 0A | 160 | 160 | 1602 |
| | 0B | 161 | 160 | |
| | 0C | 160 | 160 | |
| | 0D | 161 | 160 | |
| | 0E | 160 | 160 | |
| 3 | 0F | 160 | 160 | 1601 |
| | 10 | 160 | 160 | |
| | 11 | 161 | 160 | |
| | 12 | 160 | 160 | |
| | 13 | 160 | 160 | |
| 4 | 14 | 160 | 160 | 1602 |
| | 15 | 161 | 160 | |
| | 16 | 160 | 160 | |
| | 17 | 161 | 160 | |
| | 18 | 160 | 160 | |

**Fig. 1-4-5. Audio Frame Block Sequence for 525/60 System**

- Overlap edit (E LAP)
  "$F_H$" is inserted for overlap segments; "$0_H$" is inserted for all other.
- Sequence (SEQN)
  This provides each product block with a 0-14 count sequence. It is used when restoring audio data in the shuttle mode.

**User control words**

Eight-byte user control words can be used with each audio product block in order to convey information from the recording system to the playback system. These words are composed of 8-bit data.

## 4-1-5. Channel Coding

The video data and audio data multiplexing and subsequent processing are now described.

**1. Video/audio data multiplexing**

As shown in fig 1-2-5, the program tracks are composed of the 4 audio sectors, the two video sectors which are each positioned on either side of the respective audio sectors, the edit gaps, preambles and postambles. After the video data and audio data have passed through the respective processing system, they are multiplexed at this stage at the timing shown in Fig. 1-2-5.

**2. Inner encoding**

After 60 bytes of data have been read out in sequence from the rows of the video and audio product blocks, they pass on to the inner encoding process. Each row of the audio product blocks contains 480 bits (24 columns x 20 bits) of data. The 480 bits are divided into 1-byte (8-bits) units and each row is read out as 60 bytes of data.

In the inner encoder, the 4-byte R-S correction code is added to each row of the product block and 64-byte inner code blocks are formed.

The inner code is designed to correct one byte in a row containing an error, detect all the other error positions and correct the errors using the outer code.

**3. Scrambling**

The inner encoded data is serialized for recording onto tape but there may be occasions when "0" or "1" long strings arise in the data. The recording data and dummy random data are exclusive OR-ed and randomized.

However, the sync and identification patterns in the sync blocks originally have a construction with no DC components and so these are not randomized.

**4. Fill data and SYNC/ID data adding**

The video, audio and inner correction code data as well as the fill, sync and identification data are multiplexed to produce the data stream which is used to create the program track format on the tape.

**5. Serializing**

The parallel processed recording data is converted into serial data for recording onto tape. The data is sent by the non-return to zero (NRZ) mode.

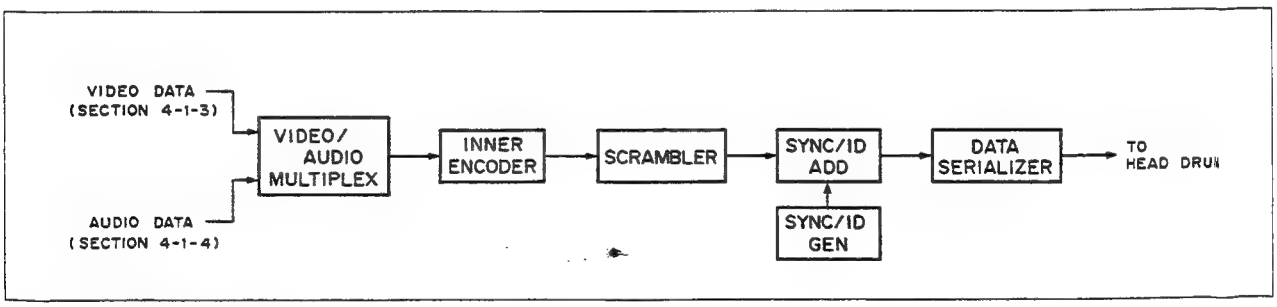



**Fig. 1-5-1. Channel Coding**

## 4-2. VIDEO SIGNAL SYSTEM

### 4-2-1. Outline of Video Signal System

The video signal system is composed of the following circuit boards. The functions of each board are as below.

IV-14 board/IV-20 Board:
- Analog video input/output circuit

VA-45 board:
- Video A/D, D/A conversion

VE-12 board:
- Digital video input circuit
- Source mapping
- Head interleave
- Video outer encode
- Video shuffling memory

FM-09 Board:
- Field memory
- De-shuffling memory
- Video outer decode
- Head de-interleave

VN-01 Board:
- Video concealment
- Source de-mapping

The video data and audio data undergo multiplexing and further processing on the following circuit boards.

IE-17 board:
- Inner encode
- ID/SYNC add
- Scramble
- Serialize

SY-70 board:
- PLL, SYNC/ID extract

CI-01 board:
- Inner decode

After the analog video signals have been supplied to the DVPC-1000, their level and offset are adjusted on the IV-14 board (or IV-20 board), and they are supplied to the VA-45 board. On the VA-45 board, the signals are A/D converted, further converted into the parallel interface format based on SMPTE RP-125/EBU TECH 3246-E and then sent to the VE-12 board.

In addition to the above data, the digital video data which has been supplied to the DIGITAL VIDEO INPUT connector is supplied to the VE-12 board, and the data corresponding to the control panel setting is selected.

The selected data undergoes source mapping and is distributed to 4 channels (heads) (head interleaving). The data further undergoes outer encoding and shuffling for each channel, and is then sent to the IE-17 board.

On the IE-17 board, the video data supplied from the VE-12 board and the audio data supplied from the AE-06 board are multiplexed, and the SYNC/ID and inner correction code are then added to them to form the program tracks. Finally, the data is sent to the DVR-1000 through the scrambler and serializer.

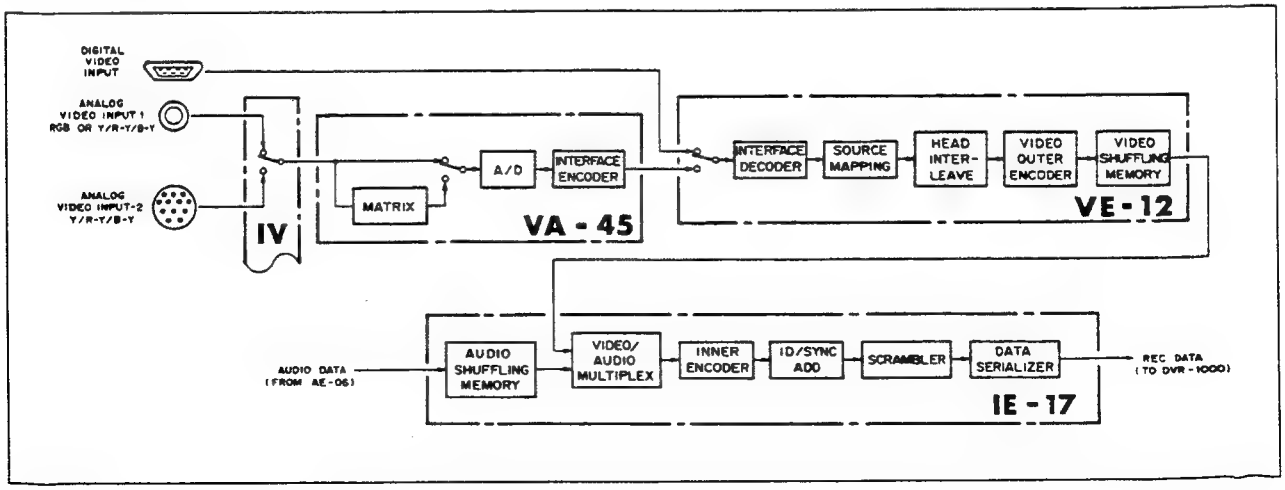



**Fig. 2-1. Video Signal Recording System**

The playback serial data from the DVR-1000 is supplied to the SY-70 board. On the SY-70 board, the clock signals are extracted from the playback data whose data rate changes in accordance with the VTR mode, and bit synchronization is provided. Also, the SYNC/ID data among the data is extracted and the playback data is converted into 8-bit parallel data based on this phase information. The parallel converted playback data is now de-scrambled and sent to the CI-01 board along with the extracted SYNC/ID data.

Errors are corrected on the CI-01 board using the inner correction code. Also, the data from the heads traversing a multiple number of tracks during stunt playback is assigned to their proper channels (channel exchanging) in accordance with the ID data extracted from the data.

Until this block, the audio data and video data are multiplexed and processed but the two types of data are separated and output from the CI-01 board. The separated video data is sent to the FM-09 board.

After it has been supplied to the FM-09 board, the video data is de-shuffled and sent to the outer decoder. In the outer decoder, based on the error flags generated by the inner decoder, erasures are corrected for up to 2 samples. Error flags are raised for the data which could not be corrected and the data is output to the VN-01 board. The video data is returned by their original data sequence by the FM-09 board and output.

After it has been supplied to the VN-01 board, the video data is de-mapped and then supplied to the concealment circuit. It is here that the data which could not be corrected by the outer decoder is interpolated or replaced using the surrounding data.

After the concealment process, the data is converted into parallel interface format data, divided into two and output. One set of data is output externally as is through the DIGITAL VIDEO OUTPUT connector. The other set is sent to the VA-45 board for conversion into analog signals and then output externally via the IV-14 (IV-20) board.

The following sections describe each board in detail. The IE-17, SY-70 and CI-01 boards are described in sections 4-4, 4-5 and 4-6, respectively.

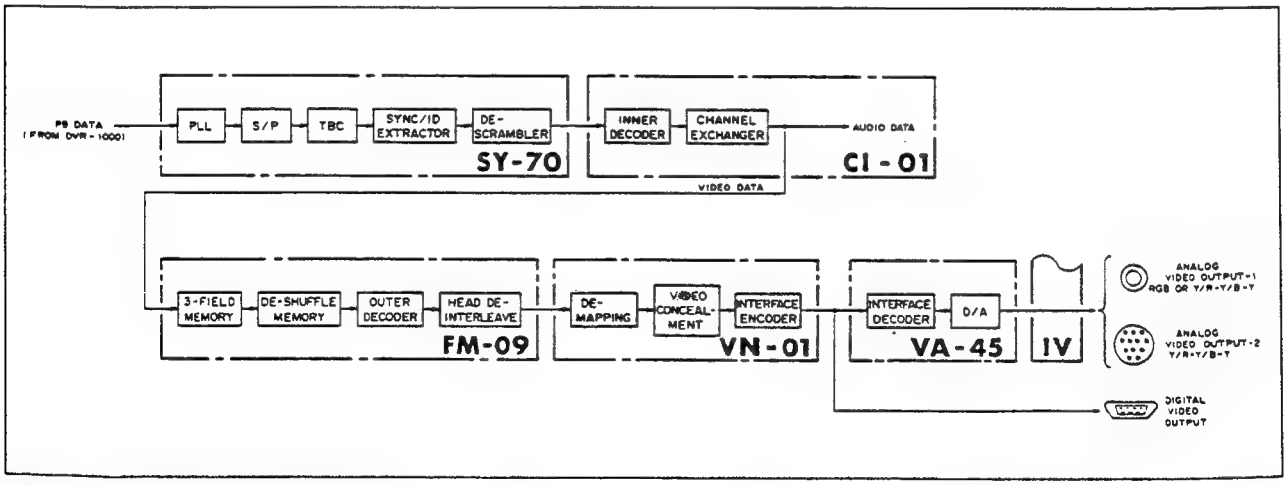



**Fig. 2-2. Video Signal Playback System**

## 4-2-2. IV-14 Board

The IV-14 board is composed of the following circuits.

- Analog video signal input/output circuits
- Reference sync selector
- Analog audio input circuit
- Digital audio signal input/output circuits
- Regulated power supply circuit

Only the video signal system is described in this section. For details on the audio signal system, refer to section 4-3-3.
In the DVPC-1000 with the serial numbers given below, the IV-14 board has been separated and the video signal system circuitry changed to the IV-20 board and the audio signal system circuitry changed to the IV-21 board. Sections 4-2-3 and 4-3-4 give details on the boards affected by these changes.

DVPC-1000(J): #11201 and Higher
DVPC-1000(UC): #11001 and Higher
DVPC-1000(EK): #11101 and Higher

### 1. Selection of Analog Video Input Signals (IV-14 board)

The following two sets of analog video signals are supplied to the IV-14 board.

- The R, G, B and SYNC or Y, R-Y and B-Y signals which are supplied to the ANALOG VIDEO INPUT-1 connectors (BNC connectors)
- The Y, R-Y and B-Y signals which are supplied from the Betacam to the ANALOG VIDEO INPUT-2 connector (12-pin multi-connector)

The analog video input signals are selected either in the local mode which is established from the DVPC-1000 or in the remote mode which is established from the control panel of the DVR-1000.

**(1) Signal selection in the local mode**

In the local mode, the input signals shown in table 2-2-1 are selected depending on the settings of RGB/Y, R-Y, B-Y selector switch S4 and BNC/MULTI selector switch S5 on the PG-13 board.

| S4/PG-13 RGB/Y, R-Y, B-Y | S5/PG-13 BNC/MULTI | SELECTED SIGNAL |
|---|---|---|
| RGB | - - - - - | R/G/B SIGNALS VIA BNC CONNECTORS |
| Y/R-Y/B-Y | BNC | Y/R-Y/B-Y SIGNALS VIA BNC CONNECTORS |
| Y/R-Y/B-Y | MULTI | Y/R-Y/B-Y SIGNALS VIA MULTI-CONNECTOR |

**Table 2-2-1. Video Input Signal Selection in the Local Mode (IV-14 Board)**

**(2) Signal selection in the remote mode**

The signals can be selected in the same way as in the local mode depending on the SETUP menu settings on the DVR-1000 control panel. For details, refer to the Operation Manual of the DVR-1000.

### 2. Selection of Analog Video Output Signals (IV-14 board)

Either the R, G, B and SYNC signals or the Y, R-Y and B-Y signals are output to the ANALOG VIDEO OUTPUT-1 connectors. The output signals are selected depending on the setting of output signal selector switch S3-5 on the PG-13 board. The Betacam Y, R-Y and B-Y signals are output to the ANALOG VIDEO OUTPUT-2 connector.

### 3. Analog Video Signal Input Circuit (IV-14 board)

The circuit configuration of each channel is virtually identical and so only a description of the R and R-Y channels will be given here.

The R or R-Y signal which has been supplied to the ANALOG VIDEO INPUT-1 connectors is input via buffer Q22 and Q23 to floating video amplifier IC79. Meanwhile, the R-Y signal from the ANALOG VIDEO INPUT-2 connector is input to floating video amplifier IC82. Each of these amplifiers is provided with variable resistor RV28 or RV34 for adjusting the offset and RV27 or RV33 for adjusting the gain of the signal, and these controls prevent a difference in level from arising when the input connector has been selected.

The video input signals whose level has been adjusted are supplied to input signal selector IC74 and 75, and one of the signals is selected in accordance with the status of the RGB/Y-1 signal and BNC/M signal supplied from the PG-13 board. The selected video signal is inverted and amplified by buffer amplifier IC73, and it is then sent to buffer IC72 and to the video monitor circuit.

After having passed through buffer IC72, the video signal is supplied to the A/D converter on the VA-45 board. Meanwhile, the signal sent to the video monitor circuit is used as the input check signal.

### 4. Reference Sync Separator (IV-14 board)

The selection of the reference sync signal is tied in with the selection of the analog video input signal in that it is selected by selector IC43, 44 and 45 depending on which video input signal has been selected.

When the R/G/B signals have been selected as the video input signal, the SYNC or black burst signal supplied to the ANALOG VIDEO INPUT-1 SYNC input connector is selected and input to sync separator circuit IC40; alternatively, when the Y/R-Y/B-Y signals have been selected, the Y input signal is selected and input to IC40.

The SYNC signal is then separated by the sync separator and after conversion to the TTL level by IC41, it is sent to the TG-28 board.

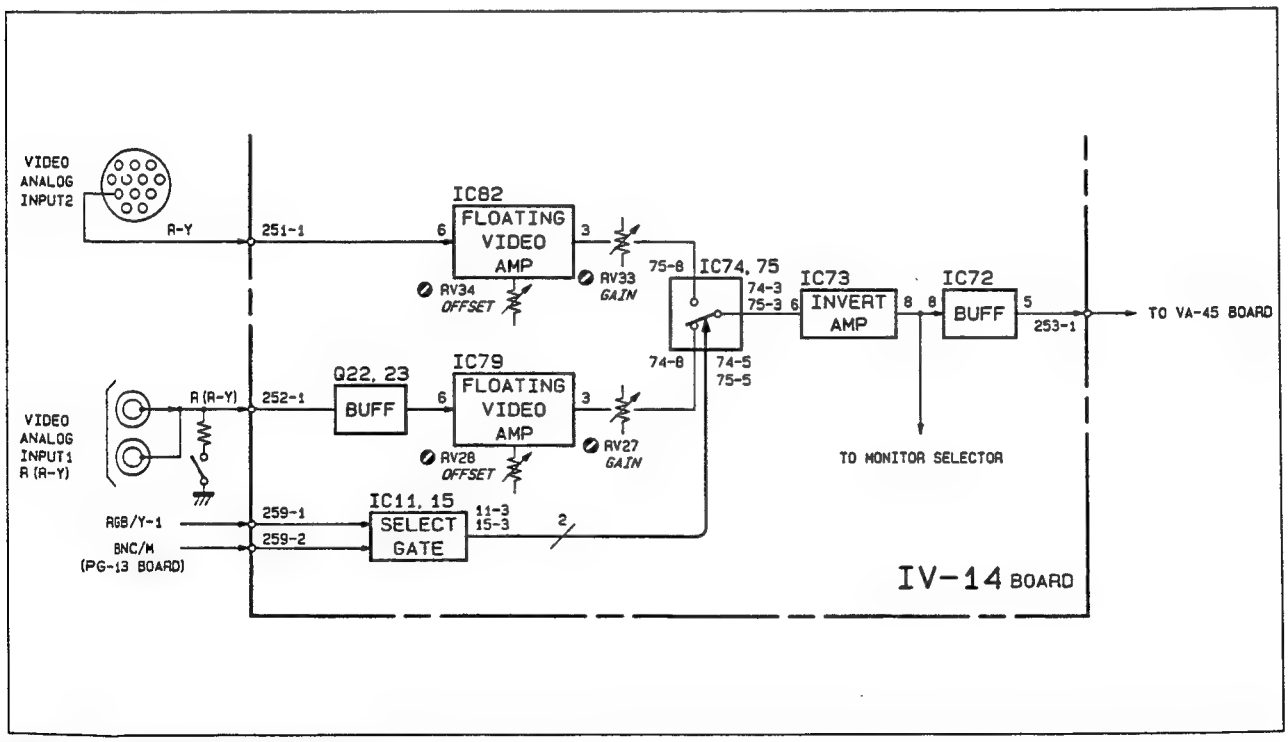



**Fig. 2-2-1. Analog Video Signal Input Circuit (IV-14 Board)**

### 5. Analog Video Signal Output Circuit (IV-14 board)

The R/G/B signals and Y/R-Y/B-Y signals D-to-A converted in the VA-45 board are supplied to this circuit. The circuit configuration of each channel is virtually identical and so only a description of the R and R-Y signals will be given here.

**(1) Main system analog video output (ANALOG VIDEO OUTPUT-1)**

After having been input from the VA-45 board to the IV-14 board, the R and R-Y signals pass through buffer amplifiers IC19 and IC35 to output signal selector IC20 and IC21. The video output signal is selected by this circuit depending on the status of the "G/Y" signal which is supplied from the PG-13 board. The level of the selected video signal is first adjusted by video amplifiers IC22 and 23 in the next stage and then the signal is output externally from the ANALOG VIDEO OUTPUT-1 connectors.

**(2) Betacam video output (ANALOG VIDEO OUTPUT-2)**

The Betacam Y/R-Y/B-Y signals are output from the ANALOG VIDEO OUTPUT-2 connector.

The output signals of buffers IC35 and 37, which are identical to the main system buffers, pass through video amplifiers IC34 and 36 and are output. However, the Y signal is supplied along a route which is different from the main system, and this is output from the ANALOG VIDEO OUTPUT-2 connector through video amplifier IC38.

In a 525/60 system, a 7.5% setup is added to the Betacam Y output signal.



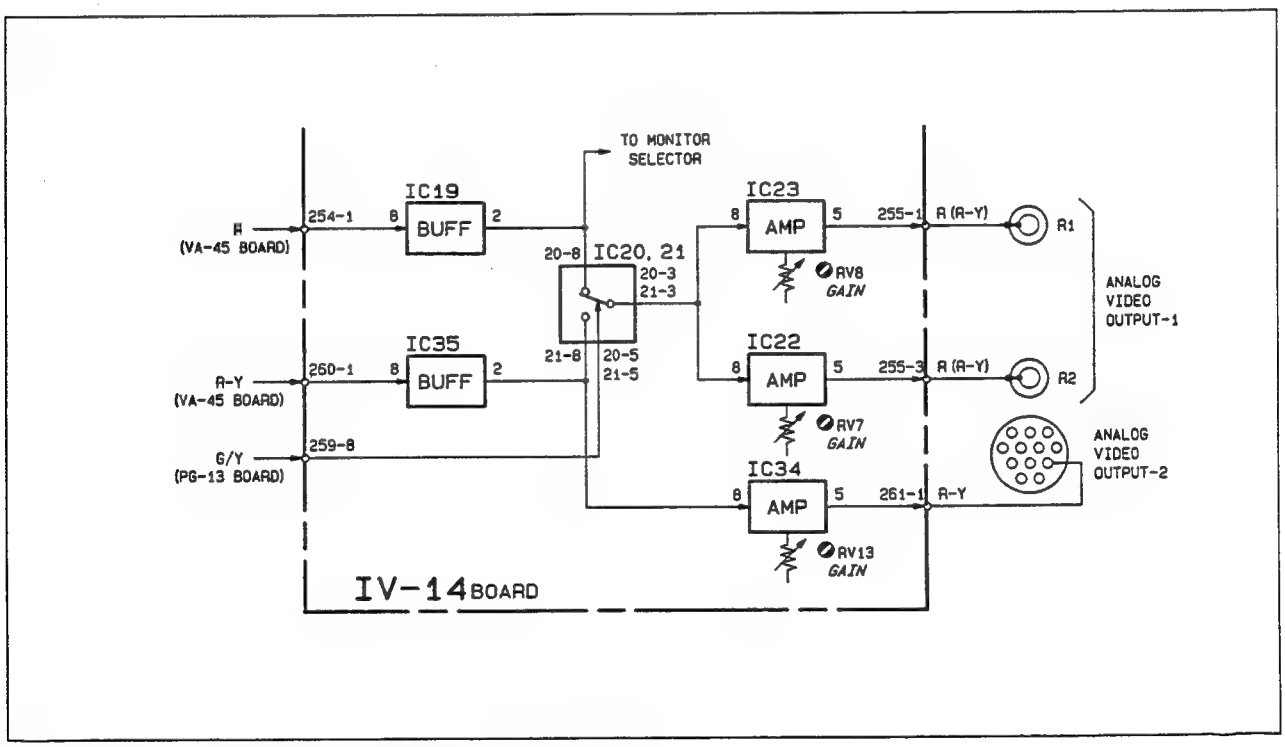



**Fig. 2-2-2. Analog Video Signal Output Circuit (IV-14 Board)**

### 6. Video Monitor Output Circuit (IV-14 board)

The R/G/B or Y/R-Y/B-Y signals from the analog video input circuit and the R/G/B signals from the analog video output circuit are supplied to this circuit. These signals are input to analog switches IC56/57, IC52/53 and IC48/49 and, depending on the status of the "BYPASS" signal supplied from the PG-13 board, one set of signals is selected. The selected signals pass through video amplifiers IC46, 50 and 54 and are output from the PICTURE MONITOR OUTPUT connectors.
When the analog video output signals have been selected as the monitor output, the character "CHR" signal supplied from the IF-139 board can be superimposed on the monitor output. The superimposition timing is controlled by the "CHR GT" signal supplied from the IF-139 board.

### 7. Waveform Monitor Output Circuit (IV-14 board)

The CTL signal or RF envelope which is supplied through the WFM IN connector from the DVR-1000 as well as the R (R-Y), G (Y) or B (B-Y) signals selected for the video monitor output are selected by analog switches IC59, 60, 61 and 62. The selected signals pass through video amplifier IC58 and are output from the WFM OUT connector.

### 8. Regulated Power Supply (IV-14 board)

This circuit creates the ± 12 V DC voltage from the ± 18 V DC voltage supplied from the power supply unit. The + 12 V system is composed of Q2, 3, 5 and IC9 while the − 12 V system is composed of Q1, 4, 6 and IC10 as well as the peripheral circuits.

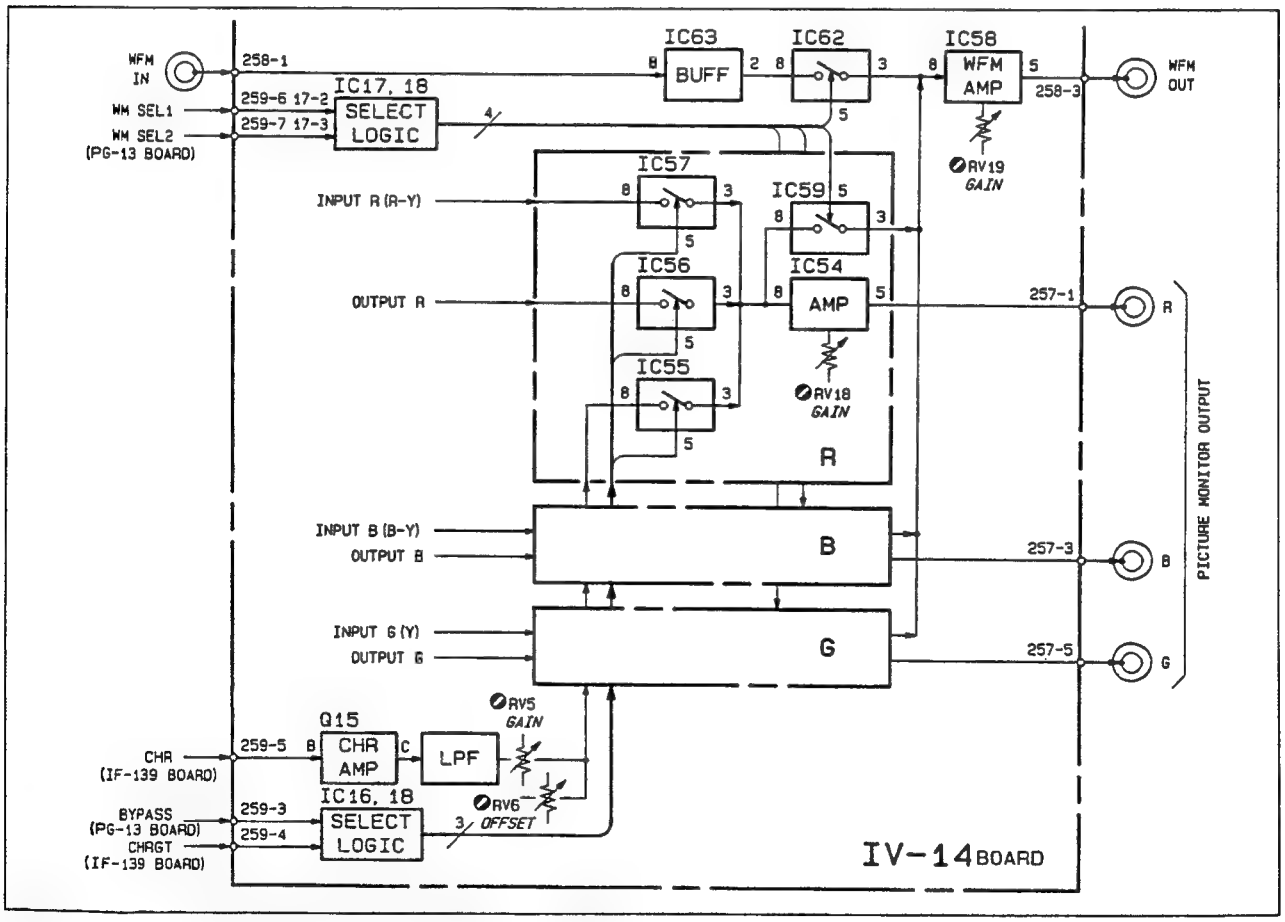



**Fig. 2-2-3. Video Monitor/WFM Output Circuit (IV-14 Board)**

## 4-2-3. IV-20 Board

The IV-20 board is composed of the analog video signal input/output circuits.
The IV-20 board is used in the DVPC-1000 with the serial numbers given below. For machines with prior serial numbers the IV-14 board is used. Details on the IV-14 board are given in section 4-2-2.

DVPC-1000(J): #11201 and Higher
DVPC-1000(UC): #11001 and Higher
DVPC-1000(EK): #11101 and Higher

### 1. Selection of Analog Video Input Signals (IV-20 board)

The following two sets of analog video signals are supplied to the IV-20 board.

- The R, G, B and SYNC or Y, R-Y and B-Y signals which are supplied to the ANALOG VIDEO INPUT-1 connectors (BNC connectors)
- The Y, R-Y and B-Y signals which are supplied from the Betacam to the ANALOG VIDEO INPUT-2 connector (12-pin multi-connector)

The video input signal is selected either in the local mode which is established from the DVPC-1000 or in the remote mode which is established from the control panel of the DVR-1000.

**(1) Signal selection in the local mode**

In the local mode, the input signals shown in table 2-3-1 are selected depending on the settings RGB/Y, R-Y, B-Y selector switch S4 and BNC/MULTI select switch S5 on the PG-13 board.

| S4/PG-13 RGB/Y, R-Y, B-Y | S5/PG-13 BNC/MULTI | SELECTED SIGNAL |
|---|---|---|
| RGB | ----- | R/G/B SIGNALS VIA BNC CONNECTORS |
| Y/R-Y/B-Y | BNC | Y/R-Y/B-Y SIGNALS VIA BNC CONNECTORS |
| Y/R-Y/B-Y | MULTI | Y/R-Y/B-Y SIGNALS VIA MULTI-CONNECTOR |

**Table 2-3-1. Video Input Signal Selection in the Local Mode (IV-20 Board)**

**(2) Signal selection in the remote mode**

The signals can be selected in the same way as in the local mode depending on the SETUP menu settings on the DVR-1000 control panel. For details, refer to the Operation Manual of the DVR-1000.

### 2. Selection of Analog Video Output Signals (IV-20 board)

Either the R, G, B and SYNC signals or the Y, R-Y and B-Y signals are output to the ANALOG VIDEO OUTPUT-1 connectors. The output signals are selected depending on the setting of output signal selector switch S3-5 on the PG-13 board. The Betacam Y, R-Y and B-Y signals are output to the ANALOG VIDEO OUTPUT-2 connector.

### 3. Analog Video Signal Input Circuit (IV-20 board)

The circuit configuration of each channel is virtually identical and so only a description of the R/R-Y and R-Y signals will be given here.

The R or R-Y signal which has been supplied to the ANALOG VIDEO INPUT-1 connectors is input via buffer Q201 and Q202 to floating video amplifier IC201. The R-Y signal from the ANALOG VIDEO INPUT-2 connector is input to floating video amplifier IC101. A 0.7Vp-p/75% color bars or 0.7Vp-p/100% color bars (EBU "N-10" standard) can be selected for the level of the color difference signals which are input to the ANALOG VIDEO INPUT-2 connector. This selection is undertaken by jumper CN101 which is set open for the former level and shorted for the latter.

The level of the signals output from the floating video amplifiers is adjusted by gain adjustment controls RV101 and RV201, after which the signals are supplied to input signal selector IC301 and 302. One of the signals is selected in accordance with the status of the RGB/Y-1 signal and BNC/M signal supplied from the PG-13 board.

The selected video signal is inverted and amplified by buffer amplifier IC303, and then sent to buffer IC305 and to the video monitor circuit.

After having passed through buffer IC305, the video signal is supplied to the A/D converter on the VA-45 board. Meanwhile, the signal sent to the video monitor circuit is used as the input check signal.

### 4. Reference Sync Separator Circuit (IV-20 board)

The selection of the reference sync signal is tied in with the selection of the analog video input signal in that it is selected by selector IC361, 362 and 363 depending on which video input signal has been selected.

When the R/G/B signals have been selected as the video input signal, the SYNC signal or black burst signal supplied to the ANALOG VIDEO INPUT-1 SYNC input connector is selected and input to sync separator IC365; alternatively, when the Y/R-Y/B-Y signals have been selected, the Y signal is selected and input to IC365.

The SYNC signal is then separated by the sync separator and after conversion to the TTL level by IC367, it is sent to the TG-28 board.

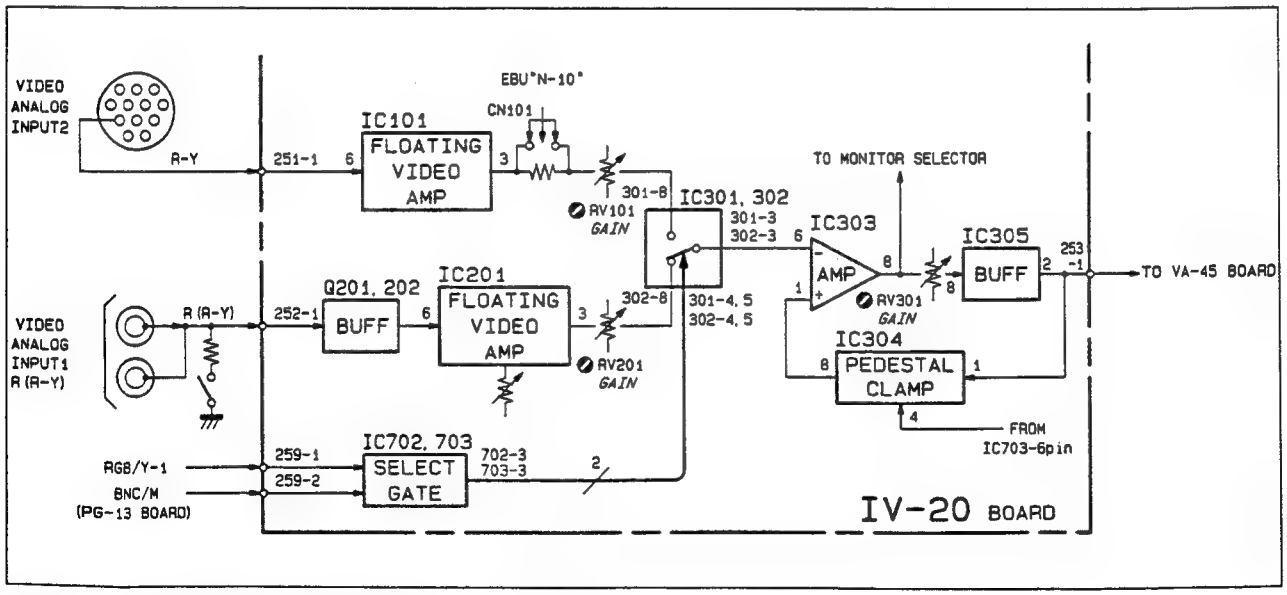



**Fig. 2-3-1. Analog Video Signal Input Circuit (IV-20 Board)**

### 5. Analog Video Signal Output Circuit (IV-20 board)

The R/G/B signals and Y/R-Y/B-Y signals are supplied from the VA-45 board to this circuit.
The circuit configuration of each channel is virtually identical and so only a description of the R and R-Y signals will be given here.

**(1) Main system analog video output (ANALOG VIDEO OUTPUT-1)**

After having been input from the VA-45 board to the IV-20 board, the R and R-Y signals pass through buffer amplifiers IC501 and 521 on their way to output signal selector IC502 and IC522 and to the video monitor circuit. The amplifier gain of the buffer amplifiers is 6 dB.
The video output signal is selected by the video signal selector depending on the status of the "G/Y" signal which is supplied from the PG-13 board. The level of the selected video signal is first adjusted by RV503 and RV523 and then the signal itself is output externally from the ANALOG VIDEO OUTPUT-1 connectors via buffers IC503 and 523.
Jumpers CN542/543 (R/R-Y), CN592/593 (B/B-Y) and CN642/643 (G/Y) serve to select whether the R/G/B or Y/R-Y/B-Y signals are to be output to the video monitor circuit. For further details, refer to the video monitor output circuit in item 6.

**(2) Betacam video output (ANALOG VIDEO OUTPUT-2)**

The Betacam Y/R-Y/B-Y signals are output from the ANALOG VIDEO OUTPUT-2 connector.
The output signals of buffers IC521 and 571, which are identical to the main system buffers, pass through buffers IC543 and 593 and are output to the R-Y and B-Y signals. It is possible to select a 0.7Vp-p/75% color bars or 0.7Vp-p/100% color bars (EBU "N-10" standard) for the level of the output color difference signals. In the former case, level select jumpers CN541 (R-Y) and CN591 (B-Y) are shorted; in the latter case, they are set open.
Meanwhile, the Y signal is supplied along a route which is different from the main system, and this is output from the ANALOG VIDEO OUTPUT-2 connector through video amplifiers IC641 and IC643.
In a 525/60 system, a 7.5% setup is added to the Betacam Y output signal.



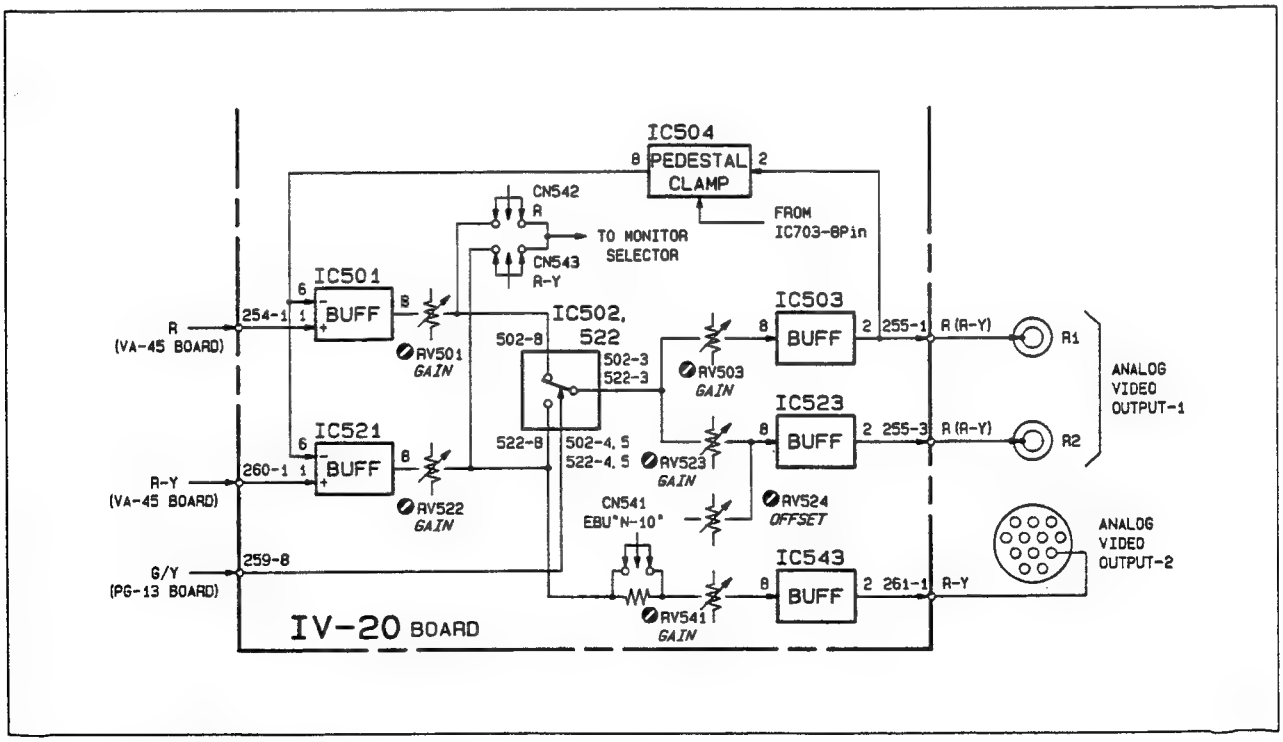



**Fig. 2-3-2. Analog Video Signal Output Circuit (IV-20 Board)**

### 6. Video Monitor Output Circuit (IV-20 board)

The R/G/B or Y/R-Y/B-Y signals from the analog video input circuit and the analog video output circuit are supplied to this circuit. These signals are supplied to analog switches IC401/402, IC421/422 and IC441/442 and, depending on the status of the "BYPASS" signal supplied from the PG-13 board, one set of signals is selected. The selected signals pass through video amplifiers IC404, 424 and 444 and are output from the PICTURE MONITOR OUTPUT connectors.
When the analog video output signals have been selected as the monitor output, the character "CHR" signal supplied from the IF-139 board can be superimposed on the monitor output. The superimposition timing of this "CHR" is controlled by the "CHR GT" signal from the IF-139 board.
When the analog video output has been selected, the settings of the jumpers below determine whether the R, G, B or Y, R-Y, B-Y signals are to be output.

| R-Y/R | B-Y/B | Y/G | SELECTED SIGNAL |
|---|---|---|---|
| CN542/543 | CN592/593 | CN642/643 | |
| CN542 | CN592 | CN642 | R-Y, B-Y, Y |
| CN543 | CN593 | CN643 | R, G, B |

**Table 2-3-2. Selection of Video Monitor Output Signals (IV-20 Board)**

### 7. Waveform Monitor Output Circuit (IV-20 board)

The CTL signal or RF envelope which is supplied through the WFM IN connector from the DVR-1000 as well as the R(R-Y), G(Y) or B(B-Y) signals selected for the video monitor output are selected by analog switches IC652, 653, 654 and 655 as the waveform monitor output signals. The selected signals pass through buffer IC656 and are output from the WFM OUT connector.

### 8. Regulated Power Supply (IV-20 board)

This circuit creates the ±12 V DC voltage from the ±18 V DC voltage supplied from the power supply unit.
The +12 V system is composed of Q1, 2, 3 and IC12 while the −12 V system is composed of Q51, 52, 53 and IC51 as well as the peripheral circuits.

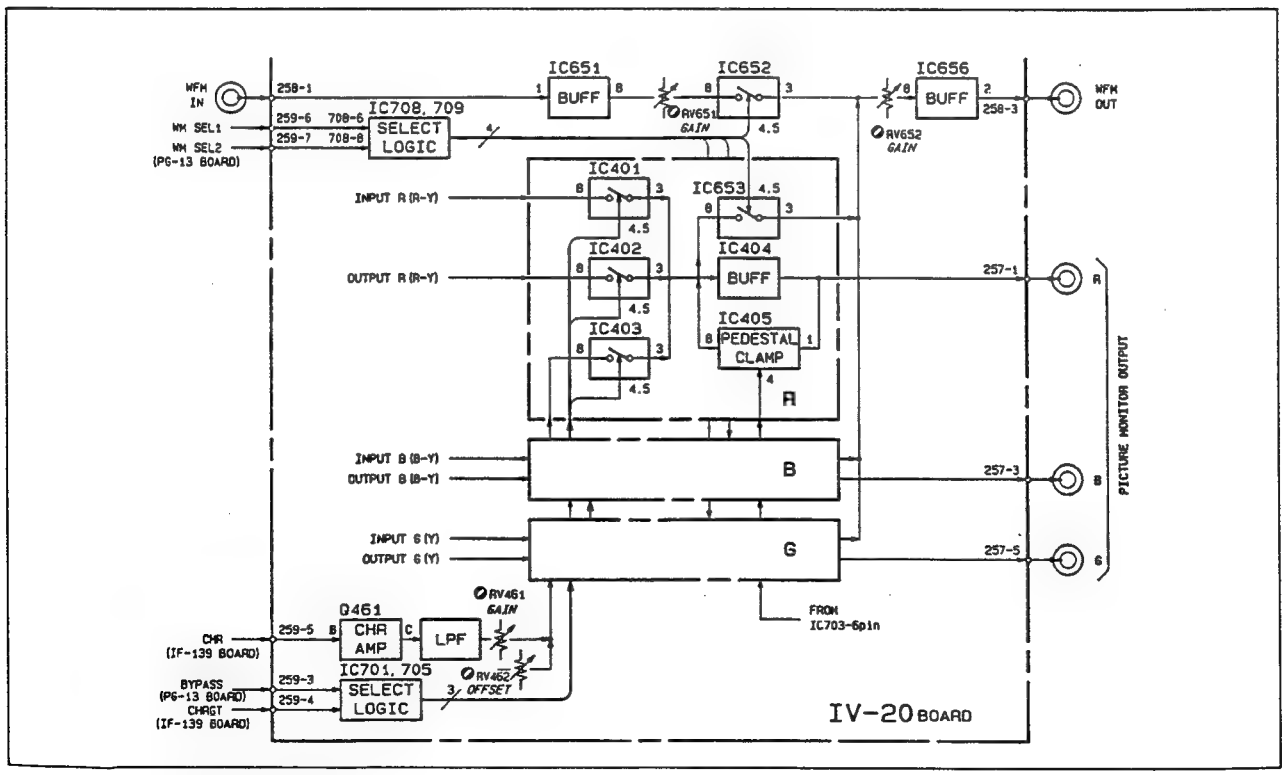



**Fig. 2-3-3. Video Monitor/Waveform Monitor Output Circuit (IV-20 Board)**

### 2. Matrix Circuit (VA-45 board)

If the R/G/B signals serve as the analog video input signals supplied from the IV board, the signals which have been converted into the Y/R-Y/B-Y signals by matrix circuit IC104, 204 and 304 are supplied to the A/D converter. The conversion matrix is given below.

$$\begin{vmatrix} Y \\ R\text{-}Y \\ B\text{-}Y \end{vmatrix} = \begin{vmatrix} 0.299 & 0.587 & 0.114 \\ 0.701 & -0.587 & -0.114 \\ -0.299 & -0.587 & 0.886 \end{vmatrix} \begin{vmatrix} R \\ G \\ B \end{vmatrix}$$

The R-Y signal supplied from the IV board and the R-Y signal provided by the matrix conversion are supplied to selector IC106 and 108, and one of these signals is selected depending on the status of the "RGB/Y" signal supplied from the PG-13 board. The polarity of the Y signal produced by the matrix conversion is inverted and after it has been made positive by inverting amplifier IC305, the signal is input to the selector.
The selected signal now passes through the next stage low-pass filter LPF101 for bandwidth limiting and then sent to the clamp circuit.
Low-pass filter LPF301 for the luminance signal features a flat frequency response up to 5.75 MHz and a response of under −12 dB at 6.75 MHz; low-pass filters LPF101 and 201 for the color difference signals feature a flat frequency response up to 2.75 MHz and a response of under −6 dB at 3.375 MHz. The frequency responses of these filters can be adjusted by RV106, 206 and 306.

### 3. Clamping Circuit (VA-45 board)

The video signals which have undergone the bandwidth limiting provided by the low-pass filters are now supplied to clamp circuit IC109, 110 and 111. This circuit serves to adjust the blanking levels of both the color difference signals to −1 V and of the luminance signal to −1.8 V.

### 4. A/D Converter (VA-45 board)

The analog video signal output from the clamp circuit is supplied to video A/D converter IC113 which converts it into digital data. The sampling frequency is 13.5 MHz for the luminance signal and 6.75 MHz for the color difference signals. The quantization level is 220 varying between 16 (10H) and 235 (EBH) for the luminance signal and 225 varying between 16 (10H) and 240 (F0H) and centering on 128 (80H) for the color difference signals. The number of samples per line is 720 for the luminance signal and 360 for the color difference signals. Fig. 2-4-2 shows the relationship between the input video signal and quantization levels.

Reference voltage generator IC112, Q106 and D104 serves to supply a DC reference voltage of −2 V to the A/D converter. The A/D converted signals are converted from the ECL to TTL level by ICA2 and A3, and supplied to the next stage limiter circuit.

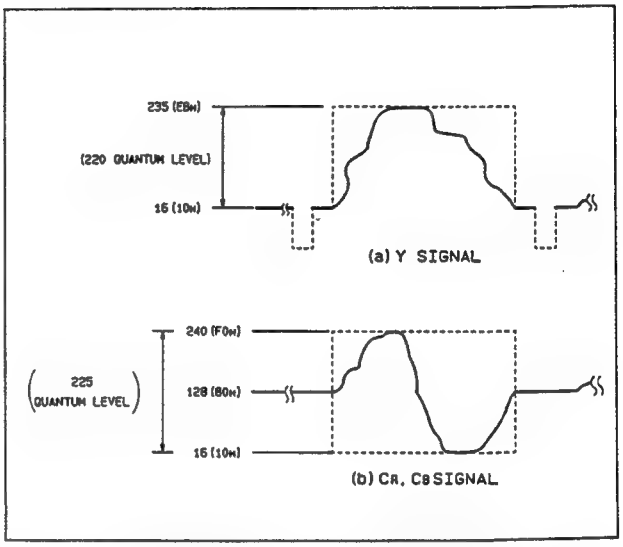



**Fig. 2-4-2. Relationship Between Input Video Signal Level and Quantization Level (VA-45 Board)**

### 5. Clock Generator (VA-45 board)

The 27 MHz clock pulse "27MI+/−" supplied from the TG-28 board is divided in ICC12 to produce the 13.5 MHz and 6.75 MHz clock signals. These signals are supplied to the video A/D converter, digital delay circuit and interface encoder on the board.
Counter ICC12 is reset by the H pulse "VAH" which is supplied from the TG-28 board.

### 6. Delay Circuit (VA-45 board)

This circuit compensates for the difference in the delay between low-pass filters LPF101 and 102 for the color difference signals and LPF301 for the luminance signal.
ICB6, C6, D5 and D6 compensate for the luminance signal delay in 13.5 MHz clock signal units. The 13.5 MHz and 6.75 MHz clock signals supplied to the video A/D converter are respectively delayed by the delay circuit configured with inverter ICD3 and jumpers CN25 through CN36. This process serves to compensate for the delay amount.

### 7. Limiter Circuit (ICB7, C7, D7/VA-45 board)

When "FF$_H$" or "00$_H$" data are contained among the A/D converted data, it means that they may be mistaken for the digital interface sync signal. This circuit serves to forcibly convert these data to "FE$_H$" and "01$_H$."

### 8. Test Signal Generator Circuit (ICB9, C9, D9, D10/VA-45 board)

This circuit outputs the test signals which are used for checking and adjusting the video signal system. The test signals and connector input signal are selected by TEST-6 switch S3-2 on the PG-13 board. The output test signals differ between boards with the "−11/12" suffix and the board with the "−13" suffix. For details, refer to the service information given in Section 2.

### 9. Parallel Video Interface Encoder (VA-45 board)

The Y/R-Y/B-Y digital video signals are supplied to interface encoder ICC12 where they are converted into signals conforming to the SMPTE RP-125/EBU TECH3246-E format. The encoder output is converted by ICA14 and B14 from the TTL to ECL level and then output to the VE-12 board. This signal is also supplied to the D/A converter on the VA-45 board as the "BYPASS-6" data.
The following control pulses are output from ICA11 (ROM) which is connected to the internal counter of encoder ICC12. The count start pulse is output from pin 13 of ICA11 to 1H counter ICD10 in the test signal generator. The clamping pulses are output from pin 79 of ICC12 and pin 14 of ICA11 to clamp circuit IC111, 211 and 311. Furthermore, when setup has been added to the Y input signal, a gate pulse is output from pin 15 of ICA11 so that the setup start and end sections will not fall below the black level (10$_H$).

### 10. Parallel Video Interface Decoder (VA-45 board)

The digital video signals, based on the SMPTE RP-125/EBU TECH3246-E format, is supplied from the VN-01 board and the interface encoder on the VA-45 board to this circuit.
The playback video signal from the VN-01 board is converted from the ECL to TTL level by ICD13, E14 and F13, and it is input to selector ICF14. In addition, the "BYPASS-6" data supplied from the interface encoder is input to selector ICD14. Depending on the status of the "BYPASS" signal supplied from the PG-13 board, the input signal for interface decoder ICG8 and the data clock signal are switched by selector ICD14, F14 and H14.
The control pulses of the clamping circuit and vertical blanking circuit are output from ICE7 (ROM) which are connected to the internal counter of interface decoder ICG8.

### 11. Smoothing and Vertical Blanking Circuit (ICE6, G6, H6/VA-45 board)

Ringing appears in the filter output after D/A conversion if the data vary suddenly when they change from the horizontal blanking section to an effective line or from an effective line to the horizontal blanking section. This circuit serves to suppress this ringing by generating transient data at the start and end of the effective lines.
The circuit uses the line gate pulse which is output from ICE10, G10 and G11 to mask the blanking lines. The blanking lines are selected by V BLANKING switches S1 and S2 on the VA-45 board.

| S2 | BLANKING LINE | |
|---|---|---|
| | 525/60 | 625/50 |
| S2-1 | ——— | ——— |
| S2-2 | 14 (276) | 11, 324 |
| S2-3 | 15 (277) | 12, 325 |
| S2-4 | 16 (278) | 13, 326 |
| S2-5 | 17 (279) | 14, 327 |
| S2-6 | 18 (280) | 15, 328 |
| S2-7 | 19 (281) | 16, 329 |
| S2-8 | 20 (282) | 17, 330 |

| S3 | BLANKING LINE | |
|---|---|---|
| | 525/60 | 625/50 |
| S3-1 | ——— | 18, 331 |
| S3-2 | ——— | 19, 332 |
| S3-3 | ——— | 20, 333 |
| S3-4 | ——— | 21, 334 |
| S3-5 | ——— | 22, 335 |
| S3-6 | ——— | ——— |
| S3-7 | ——— | ——— |
| S3-8 | ——— | ——— |

**Table 2-4-1. Blanking Line Selection (VA-45 Board)**

### 12. Digital Delay Circuit (IC901, E3, F4, G3, G4, H3, H4/VA-45 board)

In order to compensate for the difference between the delay amounts of low-pass filters LPF401 and 501 for the color difference signals and of LPF601 for the luminance signal, the Y signal in the interface decoder output is delayed by IC901 and ICH4. The very slight phase difference between the color difference and luminance signals is compensated to within 15 nsec by the delay circuit composed of inverter ICG12 and jumpers CN13 through CN24.

### 13. D/A Converter (VA-45 board)

The delayed video signal is converted from the TTL to ECL level by ICC1 and D1, and output to D/A converter IC409. RV401 functions to adjust the gain. When OUTPUT GAIN PRESET switch S101 on the front of the board is set to the "VAR" position, the output level of the 3 video channels are controlled simultaneously by RV701.

The R-Y signal provided by D/A conversion passes through low-pass filter LPF401 and buffer amplifier IC402, it is divided into two, and output to the IV-20 (or IV-14) board. One part of the signal is output without change to the IV board via buffer IC406 and the other part of the signal is first converted into the R signal by the de-matrix circuit and then sent to the IV board.

Two signals, the main system output signal (pin 13C of CN706) and the Betacam output signal (pin 12C of CN705), are output to the IV board as the Y signal. In the case of a 525/60 system, a 7.5% setup is added by IC607 and Q707 to the Betacam Y signal.

The level of the horizontal blanking period for the output signal is clamped to 0 V DC by clamping circuit IC402 and 403.

### 14. De-matrix Circuit (IC404, 504, 604/VA-45 board)

The conversion matrix is defined as follows.

$$\begin{vmatrix} R \\ G \\ B \end{vmatrix} = \begin{vmatrix} 0.999 & 1.402 & -0.001 \\ 1.000 & -0.714 & -0.344 \\ 1.000 & 0.001 & 1.172 \end{vmatrix} \begin{vmatrix} Y \\ R\text{-}Y \\ B\text{-}Y \end{vmatrix}$$

The Y/R-Y/B-Y signals which are output from the D/A converter are de-matrixed using the above coefficient and converted into the R/G/B signals. The de-matrixing processed R/G/B signals are output via buffers IC405, 505 and 605 to the IV-20 (IV-14) board.

### 15. Sync Addition Circuit (Q701-Q710/VA-45 board)

The TTL level "SYNC" signal supplied from the TG-28 board is converted by Q704 and 705 as well as by Q701 and 703, and it is added respectively to the main Y signal and Betacam Y signal. In the board with the "−13" suffix, the SYNC signal can be added to the R/G/B signals of the main system output by shorting solder bridges SL3, SL4 and SL5.

### 16. HALF H Blanking (VA-45 board)

In the digital video signals supplied by the digital interface, the data of lines 263 and 282 (525/60 system) or lines 23 and 623 (625/50 system) do not undergo HALF H blanking, as is the case with the other lines, and when these particular data are D/A converted, the equalizing pulse of line 263 is lost in the 525/60 system while that of line 623 is lost in the 625/50 system. Therefore, the D/A converter section on this board normally provides HALF H blanking for the above lines and D/A conversion. In the board with the "−13" suffix, when jumper CN5 is shorted, D/A conversion can be provided without HALF H blanking. Furthermore, when CN3 is open and CN4 is shorted, the equalizing pulse for the above line can be eliminated altogether.

### 17. Regulated Power Supply Circuit (VA-45 board)

A ±18 V DC voltage is supplied from the power supply unit to this circuit which produces a regulated +12 V DC voltage using Q801, 802, 804 and IC801. In the same way, a −12 V DC voltage is produced by Q831, 832, 834 and IC802, and a −5 V DC voltage is produced by Q861, 862 and IC802.

## 4-2-5. VE-12 Board

The VE-12 board may have the board suffix of "−11" and "−12". In each case, the configuration of the circuitry is virtually identical although the reference numbers of some parts differ between board with the "−11" and board with the "−12" suffix. The following description applies to the board with the "−11" suffix unless otherwise noted.

### 1. Outline (VA-12 board)

This board serves to convert the digital video signals conforming to the SMPTE RP-125/EBU TECH3246-E format into the program track format and to output the resulting signals. The program track is composed of the video signals, audio signals, sync, ID and edit gaps. On this board, only the video signals in the program track are processed; other signals are dealt with by releasing the slots.

The two signals listed below are supplied to this board. Both are in conformity with the SMPTE RP-125/EBU TECH3246-E format and are composed of 8-bit video data and a 1-bit sync clock. When the DVPC-1000 has been set to the local mode, the signal selected by VIDEO INPUT SELECT switch S2 on the VE-12 board is input; alternatively, when it is set to the remote mode, the signal selected on the control panel of the DVR-1000 is input.

- The signal produced by A/D converting the analog video signal, which has been supplied through the ANALOG VIDEO INPUT-1 and INPUT-2 connectors, on the VA-45 board and by encoding it in the SMPTE RP-125/EBU TECH3246-E format.
- The digital video signal which is supplied from the external equipment through the DIGITAL VIDEO INPUT connector.

As part of the main system signals, the program track format signal is output from the VE-12 board to the IE-17 board. As part of the bypass system signals, the 8-8 mapping circuit output signal (BYPASS-5) is sent to the VN-01 board and the video outer encoder output (BYPASS-4) is output to the FM-09 board.



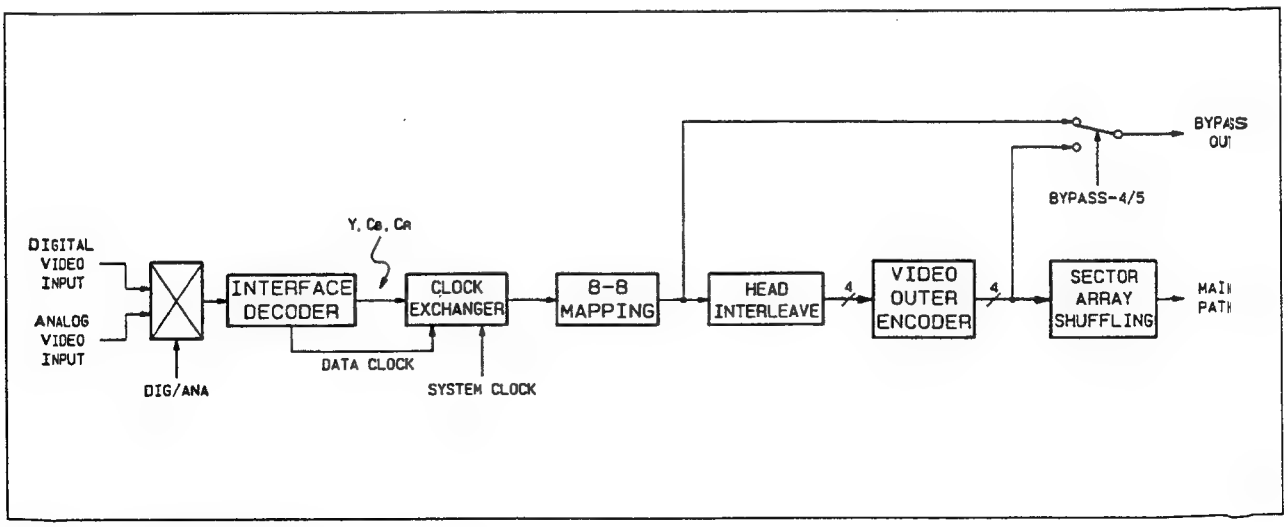



**Fig. 2-5-1. Function Diagram (VE-12 Board)**

**2. Interface Decoder (ICA33, B32/VE-12 board)**

The VE-12 board receives the differential input of the 8-bit video data and 1-bit data clock of the two signals at the ECL level. Inserted into the respective input circuits are the RC block (CP13-CP21) for eliminating the high-range in-phase components, the 10-ohm resistance for input protection and the diode array (CP1-CP12). The input data are first converted from the ECL to TTL level by ICA37, A38, B35, B36 and B38 and then supplied to selector ICA35 and A36. Depending on the contents of the "VIDEO SELECT D/A" signal output from pin 38 of UPI ICC36, this circuit selects either the digital video input or analog video input, and it outputs the selected signal to interface decoder ICA33.

The interface decoder serves to decode the signal with the SMPTE RP-125/EBU TECH3246-E format and outputs the $Y/C_B/C_R$ data signals (sampling frequency $Y = 13.5$ MHz, $C_B/C_R = 6.75$ MHz) and the F/V/H signals. Fig. 2-5-2 is a timing chart of the interface decoder output signals.

The total number of effective samples in one digital active line is 1,440, and this figure breaks down into 720 samples for Y and 360 samples each for $C_B$ and $C_R$. With Y conversion (13.5 MHz sampling), the digital horizontal blanking width works out to be 138 samples for a 525/60 system and 144 samples for a 625/50 system. The data start point is synchronized with the fall of the H pulse.

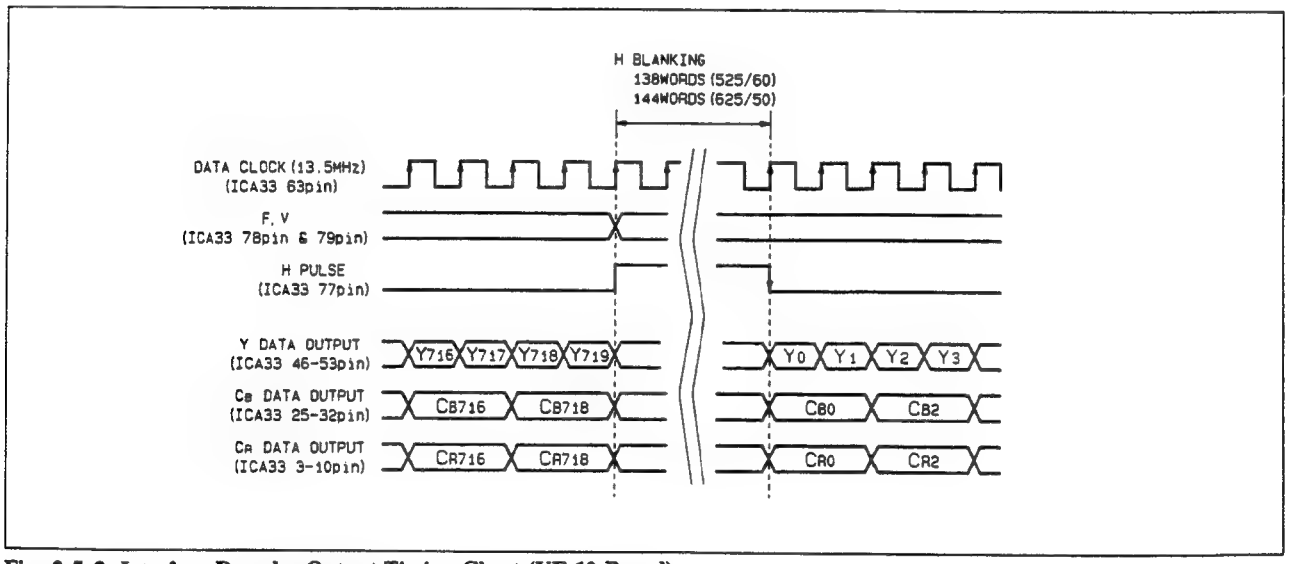



**Fig. 2-5-2. Interface Decoder Output Timing Chart (VE-12 Board)**

### 3. Clock Replacement Circuit (ICA30, B30, B33, C32/VE-12 board)

The output data of interface decoder ICA33 has a clock signal which is synchronized with the input data but it is characterized by a phase which is indefinite as regards the system clock pulse. Consequently, in order for data processing to be undertaken in the 13.5 MHz system, the data must be replaced by the 13.5 MHz system clock pulse "CK135" which is generated by the TG-28 board. This processing is done by FIFO memory ($\mu$PD41101C; NEC) ICA30, B30, B33 and C32.

Inside the FIFO memory are read address and write address pointers. These pointers are counted up in synchronization with the read clock pulse "RCK" (system clock pulse) and write clock pulse "WCK" (data clock pulse) and they are reset to zero by the reset pulse which is supplied to the RSTR terminal (pin 6) and the RSTW terminal (pin 19). Since the nature of the FIFO memory is such that a "300 nsec + 1/2 write cycle" is required for reading out data which have been written in the memory, the output timing of the "RE" pulse is controlled based on the pointer reset pulse.

In the case of an analog video input, a stable clock pulse is input provided that the VA-45 board is functioning normally.

Alternatively, in the case of a digital video input, since the input data and clock are supplied from an external unit, the input clock pulse (WCK) will be lost if the connector has been disconnected. However, since the "RCK" pulse from the TG-28 board is supplied continuously, the relationship between the address pointer positions shifts out of alignment and the FIFO operation can no longer be guaranteed.

In order to safeguard against this, ICE33 monitors the abnormality of the input clock pulse, and in case of any abnormality in the data clock pulse, it resets the address pointers.

For the VE-12 board with the "−11" suffix, ICE33 monitors the data clock pulse (FIFO write clock pulse) and outputs reset pulse when the data clock is stopped, power is switched on or when the system is changed.

For the VE-12 board with the "−12" suffix, the circuitry has been modified. ICE33 monitors the phases of the 1/16 cycle ICE34 counter supplied by the data clock (FIFO write clock) and 1/16 cycle ICD35 counter supplied by the system clock (FIFO read clock) and outputs read address pointers reset pulse when the relation ship between the phases shifts out of alignment. If an abnormality is detected in the clock pulse, reset pulse is continuously supplied in order to stabilize the data clock pulse and during this period the screen will be unstable. However, once the data clock pulse is stabilized, normal operation will be restored.



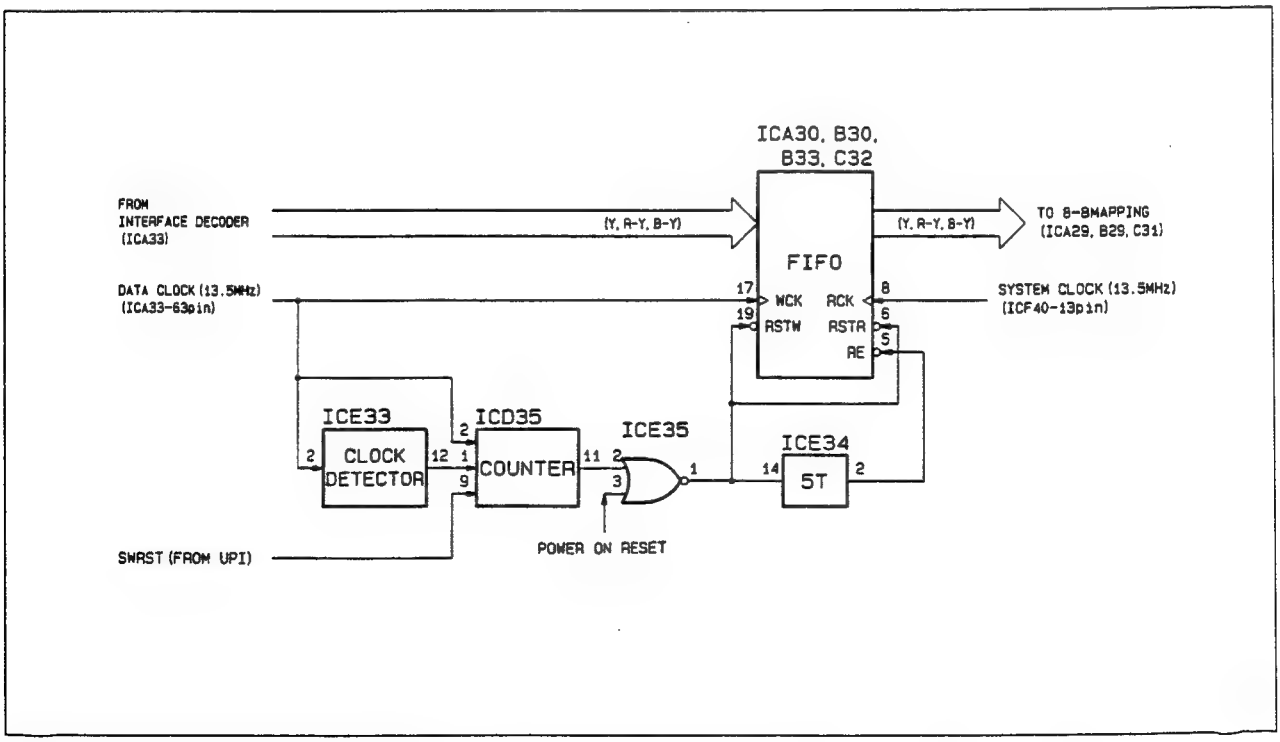



**Fig. 2-5-3. Block Diagram of Clock Replacement Circuit (VE-12 Board)**

### 4. 8-8 Mapping Circuit (ICA29, B29, C30/VE-12 board)

This is the source mapping circuit which is based on the D-1 format. If there is a bit error in the two most significant bits (MSB and MSB-1), errors in the 128 or 64 quantization level will respectively occur at the maximum level. The process of 8-8 mapping enables this maximum error level to be reduced. Mapping proceeds in accordance with the contents of Table 2-5-1 and conversion is provided for the 01H — FEH data.

Mapping concerns only the video data, and the data of the following lines are processed.

Lines 21 to 263, 283 to 525 for a 525/60 system

Lines 23 to 310, 336 to 623 for a 625/50 system

In the test mode, the mapping process can be set ON or OFF using MAPPING ON/OFF switch S1-1 connected to pin 33 of UPI ICC36. In addition, this circuit also outputs the period check signal applying during editing in accordance with the status of the "VBV" (black-video-black) signal which is supplied from the TG-28 board.

| MS WORD (4 BITS) \ LS WORD (4 BITS) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 00 | 80 | 40 | 20 | 10 | 08 | 04 | 02 | 01 | C0 | A0 | 90 | 88 | 84 | 82 | 81 |
| 1 | 60 | 50 | 48 | 44 | 42 | 41 | 30 | 28 | 24 | 22 | 21 | 18 | 14 | 12 | 11 | OC |
| 2 | 0A | 09 | 06 | 05 | 03 | E0 | D0 | C8 | C4 | C2 | C1 | B0 | A8 | A4 | A2 | A1 |
| 3 | 98 | 94 | 92 | 91 | 8C | 8A | 89 | 86 | 85 | 83 | 70 | 68 | 64 | 62 | 61 | 58 |
| 4 | 54 | 52 | 51 | 4C | 4A | 49 | 46 | 45 | 43 | 38 | 34 | 32 | 31 | 2C | 2A | 29 |
| 5 | 26 | 25 | 23 | 1C | 1A | 19 | 16 | 15 | 13 | 0E | 0D | 0B | 07 | F0 | E8 | E4 |
| 6 | E2 | E1 | D8 | D4 | D2 | D1 | CC | CA | C9 | C6 | C5 | C3 | B8 | B4 | B2 | B1 |
| 7 | AC | AA | A9 | A6 | A5 | A3 | 9C | 9A | 99 | 96 | 95 | 93 | 8E | 8D | 8B | 87 |
| 8 | 78 | 74 | 72 | 71 | 6C | 6A | 69 | 66 | 65 | 63 | 5C | 5A | 59 | 56 | 55 | 53 |
| 9 | 4E | 4D | 4B | 47 | 3C | 3A | 39 | 36 | 35 | 33 | 2E | 2D | 2B | 27 | 1E | 1D |
| A | 1B | 17 | 0F | F8 | F4 | F2 | F1 | EC | EA | E9 | E6 | E5 | E3 | DC | DA | D9 |
| B | D6 | D5 | D3 | CE | CD | CB | C7 | BC | BA | B9 | B6 | B5 | B3 | AE | AD | AB |
| C | A7 | 9E | 9D | 9B | 97 | 8F | 7C | 7A | 79 | 76 | 75 | 73 | 6E | 6D | 6B | 67 |
| D | 5E | 5D | 5B | 57 | 4F | 3E | 3D | 3B | 37 | 2F | 1F | FC | FA | F9 | F6 | F5 |
| E | F3 | EE | ED | EB | E7 | DE | DD | DB | D7 | CF | BE | BD | BB | B7 | AF | 9F |
| F | 7E | 7D | 7B | 77 | 6F | 5F | 3F | FE | FD | FB | F7 | EF | DF | BF | 7F | FF |

**Table 2-5-1. 8-8 Mapping Table (VE-12 Board)**

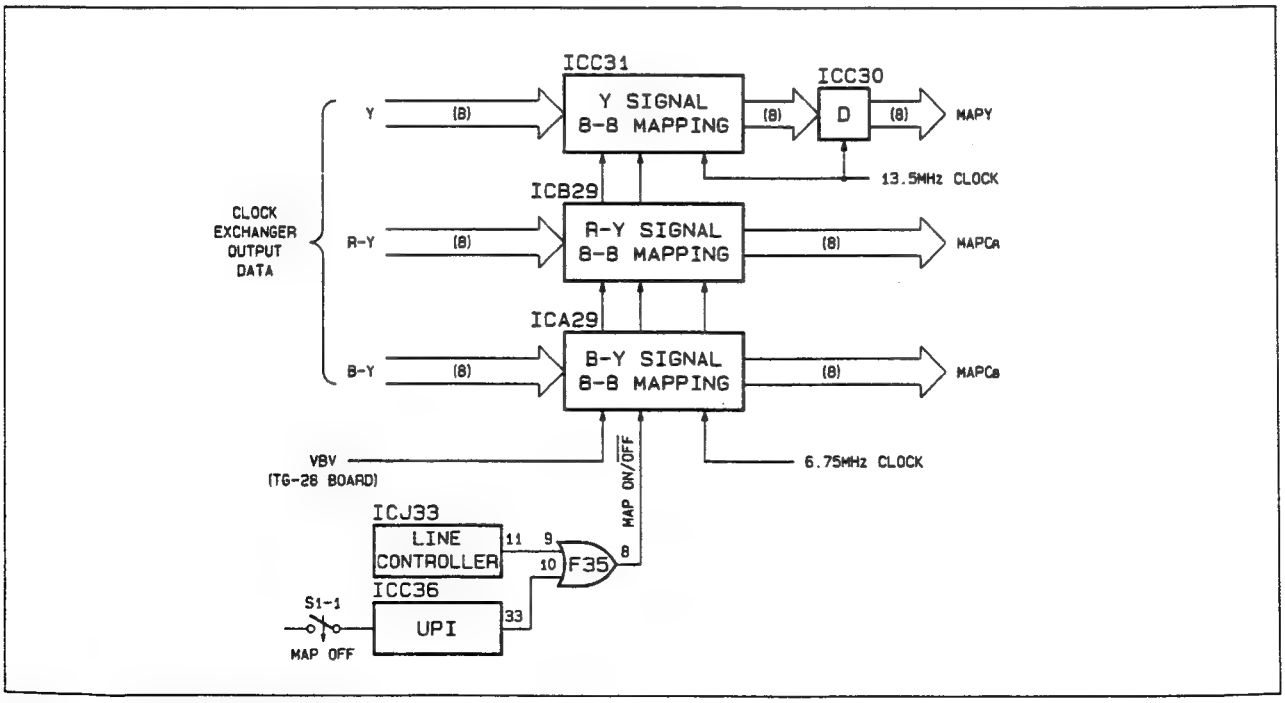



**Fig. 2-5-4. 8-8 Mapping Circuit (VE-12 Board)**

**5. Head Interleave (Inter-Line Shuffling) (ICA23, A25, A27, A28, B23, B25, B27, B28, C23, C25, C27, C28/VE-12 board)**

This is an operation in which the input data are re-arranged line by line in sample units at the 4 heads (channels). As a result of this operation, the $C_B$, $C_R$ and Y data in the same sample enter the same inner code block and even when individual $C_B$, $C_R$ and Y data enter different outer code blocks. So, when inner errors cannot be corrected, the data can still be corrected by outer error correction. Furthermore, even when a head is clogged, adequate concealment is still possible.
Since there are 4 channels, the number of samples per line for each channel is 360 (1440 divided by 4). Included in this are the $Y_{ODD}$, $Y_{EVEN}$, $C_R$ and $C_B$ data which respectively comprise 90 samples each. The input data, which have been sampled at Y = 13.5 MHz and CB/CR = 6.75 MHz, are sampled in this circuit at 6.75 MHz and output in the sequence of "$C_B$, Y, $C_R$, Y ...".

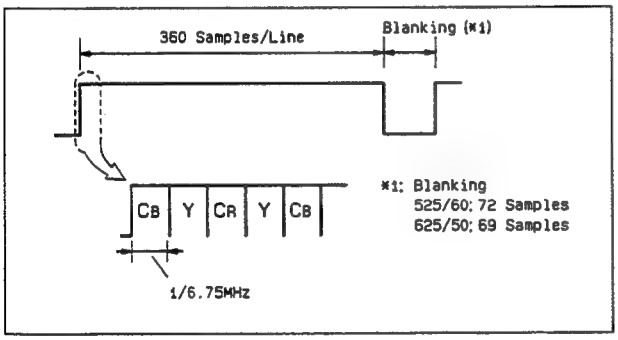



**Fig. 2-5-5. Head Interleaving Output Data Stream (VE-12 Board)**

The method by which the data are allocated to each channel differs according to the number of scanning lines, the field number, segment number and odd/even-numbered lines. Table 2-5-2 shows the relationship between the fields and segments while Table 2-5-3 shows how the data are allocated to each channel. One video segment is composed of 50 lines, and a field is composed of 5 segments (250 lines) for a 525/60 system and 6 segments (300 lines) for a 625/50 system.

525/60 SYSTEM

| FIELD | SEGMENT | LINE | |
|---|---|---|---|
| 0 | 0 | 14-63 | (A) |
| | 1 | 64-113 | (B) |
| | 2 | 114-163 | (A) |
| | 3 | 164-213 | (B) |
| | 4 | 214-263 | (A) |
| 1 | 0 | 276-325 | (B) |
| | 1 | 326-375 | (A) |
| | 2 | 376-425 | (B) |
| | 3 | 426-475 | (A) |
| | 4 | 476-525 | (B) |

625/50 SYSTEM

| FIELD | SEGMENT | LINE | |
|---|---|---|---|
| 0 | 0 | 11-60 | (A) |
| | 1 | 61-110 | (B) |
| | 2 | 111-160 | (A) |
| | 3 | 161-210 | (B) |
| | 4 | 211-260 | (A) |
| | 5 | 261-310 | (B) |
| 1 | 0 | 324-373 | (A) |
| | 1 | 374-423 | (B) |
| | 2 | 424-473 | (A) |
| | 3 | 474-523 | (B) |
| | 4 | 524-573 | (A) |
| | 5 | 574-623 | (B) |

**Table 2-5-2. Relationship Between Segments and Lines (VE-12 Board)**

| PIXEL INDEX | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | ••• |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (A) | EVEN LINE | Y | A | C | B | D | A | C | B | D | A | C | B | D | A | C | B | D | A | |
| | | CR/CB | A | | C | | B | | D | | A | | C | | B | | D | | A | |
| | ODD LINE | Y | B | D | A | C | B | D | A | C | B | D | A | C | B | D | A | C | B | |
| | | CR/CB | B | | D | | A | | C | | B | | D | | A | | C | | B | |
| (B) | EVEN LINE | Y | C | A | D | B | C | A | D | B | C | A | B | D | C | A | B | D | C | |
| | | CR/CB | C | | A | | D | | B | | C | | A | | D | | B | | C | |
| | ODD LINE | Y | D | B | C | A | D | B | C | A | D | B | C | A | D | B | C | A | D | |
| | | CR/CB | D | | B | | C | | A | | D | | B | | C | | A | | D | |

(Note) A. B. C. D: Channel (head) numbers
(A); 525/60: When the field numbers and the segment numbers are (0.0), (0.2), (0.4), (1.1) and (1.3)
625/50: For even segments
(B); 525/60: For the exception of (A)
625/50: For odd segments

**Table 2-5-3. Data Allocation (VE-12 Board)**

Fig. 2-5-6 is a block diagram of the head interleaving circuit and Fig. 2-5-7 is a timing chart of the head interleaving.
In order to adjust the delay for the luminance data "MAPY" which are output from the 8-8 mapping circuit, the data are first delayed 3T (1T = 1/13.5 MHz) by ICC29 and then input into series-parallel converter ICC23, C25, C27 and C28. The input data are delayed by 6T inside the ICs and latched by the "HI YPCK" signal. The chroma data "MAPCB" and "MAPCR" are delayed by 4T' (1T' = 1/6.75 MHz) inside ICA23, A25, A27 and 28 and inside ICB23, B25, B27 and B28 respectively, and they are latched by the "HI CPCK" signal.

The video data which have been latched inside the converter are output in the data sequence of "$C_B$, Y, $C_R$, Y ... " sampled by 6.75 MHz by the "HIYSEL," "HICBCEL" and "HICRSEL" output enable signals. The control signals "HIYPCK," "HICPCK," "HIYSEL," "HICBSEL" and "HICRSEL" are generated by PROM ICJ27 and counter ICK27. These ICs use the signal, which is produced by differentiating the fall of the H pulse which in turn is used inside the board, as the load pulse.

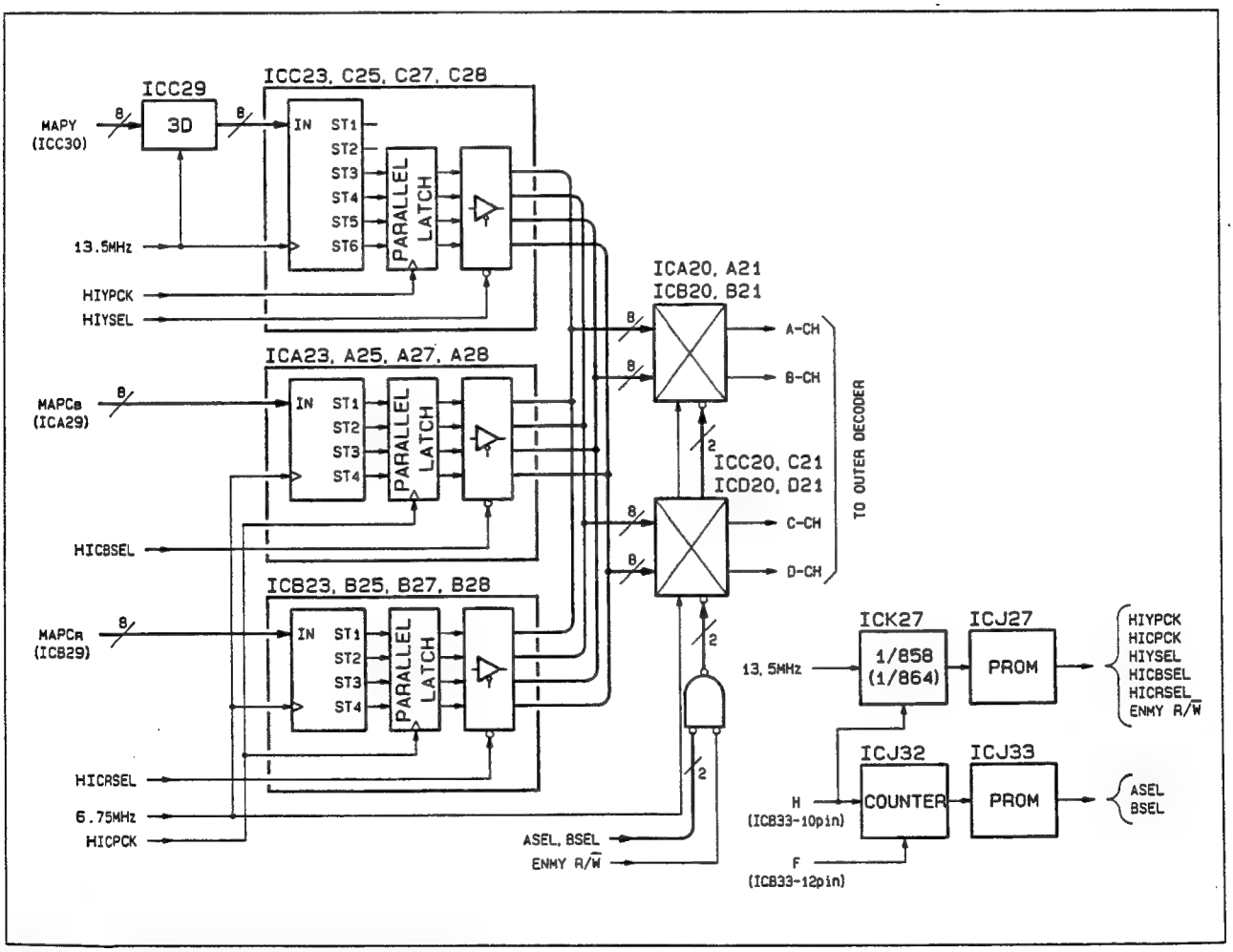



**Fig. 2-5-6. Head Interleaving Circuit (VE-12 Board)**

In accordance with line-by-line signals "A SEL" and "B SEL," next selector ICA20, A21, B20, B21, C20, C21, D20 and D21 serve to allocate the data to each channel so that the relationships shown in Tables 2-5-2 and 2-5-3 will be satisfied. "A SEL" and "B SEL" are generated by PROM ICJ33 and counter ICJ32. These ICs use the signal, which is produced by differentiating the fall of the frame pulse which in turn is used inside the board, as the load pulse.

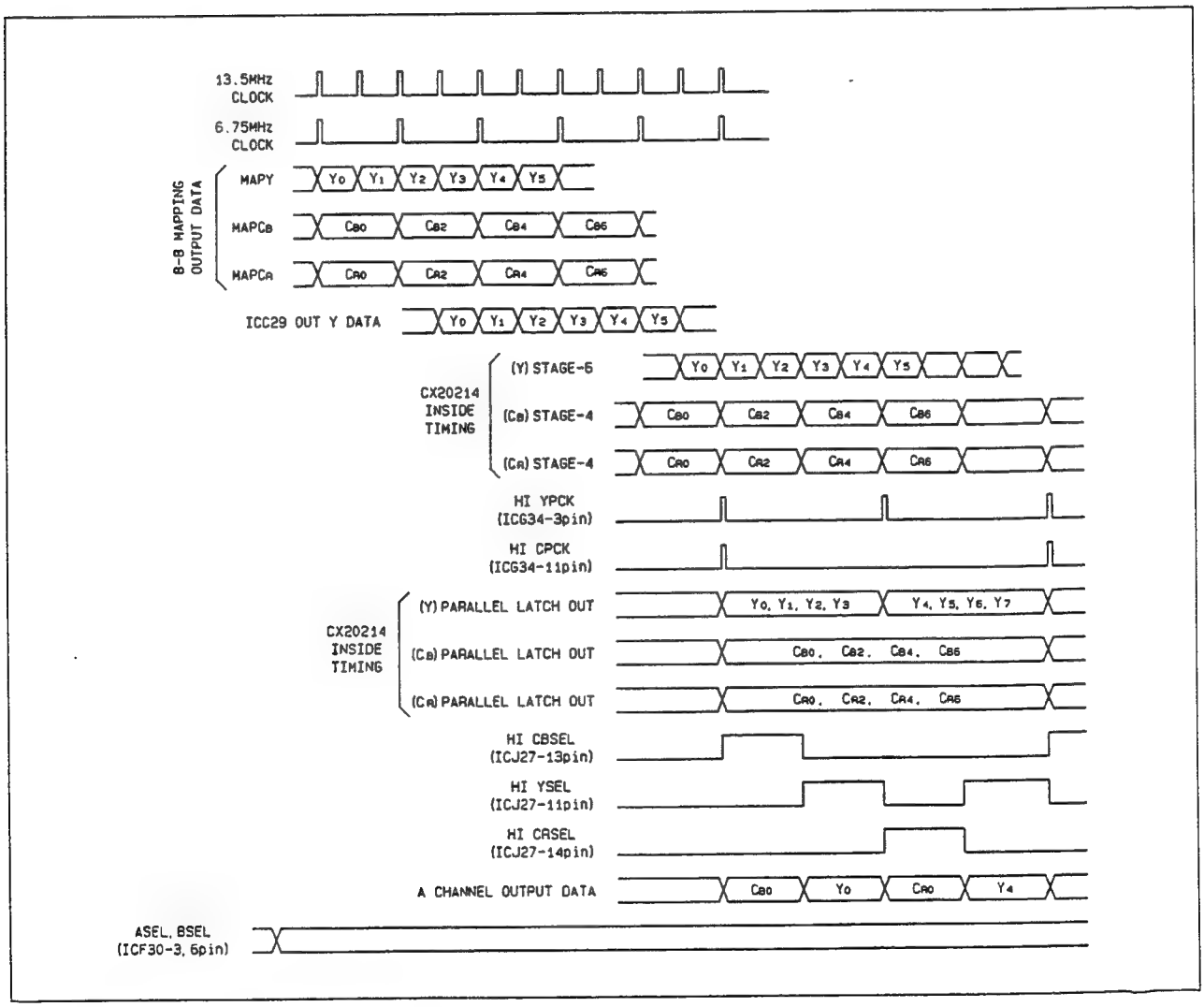



**Fig. 2-5-7. Head Interleaving Timing Chart (VE-12 Board)**

### 6. Video Outer Encoder (ICF20, H20, J20, K20/VE-12 board)

After having been processed by the head interleaving circuit, the data enter the outer encoder for each channel. Used for the correction code is a (32, 30) Reed-Solomon code with a 2-byte parity.

As shown in Fig. 2-5-5, data equivalent to 360 samples per line are continuously supplied to each of the outer encoder channels. The (32, 30) Reed-Solomon code is used for these data and so, as shown in Fig. 2-5-8, one line is composed of 12 outer code blocks.

The actual data stream is multiplexed by $C_B$, Y, $C_R$, Y'. This means that the outer code blocks in Fig. 2-5-8 are sampled vertically, one line is divided into 3 blocks as shown in Fig. 2-5-9 and the number of effective samples in one line is 384.

Channel A is used as the example in the description below. Fig. 2-5-10 is a block diagram of the outer encoder and Fig. 2-5-11 is a timing chart of this encoder.

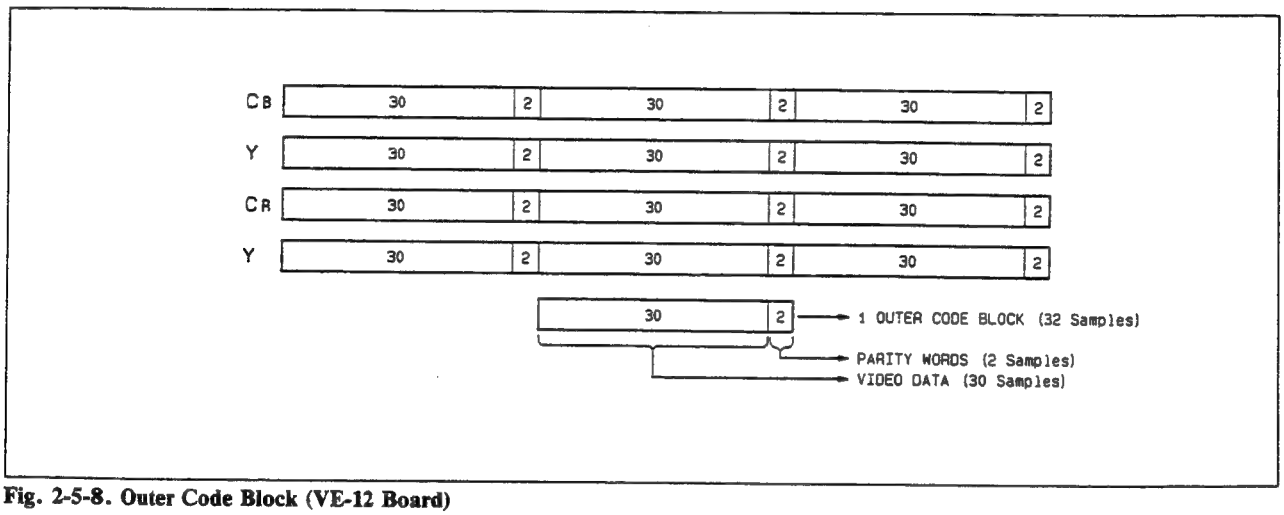



**Fig. 2-5-8. Outer Code Block (VE-12 Board)**

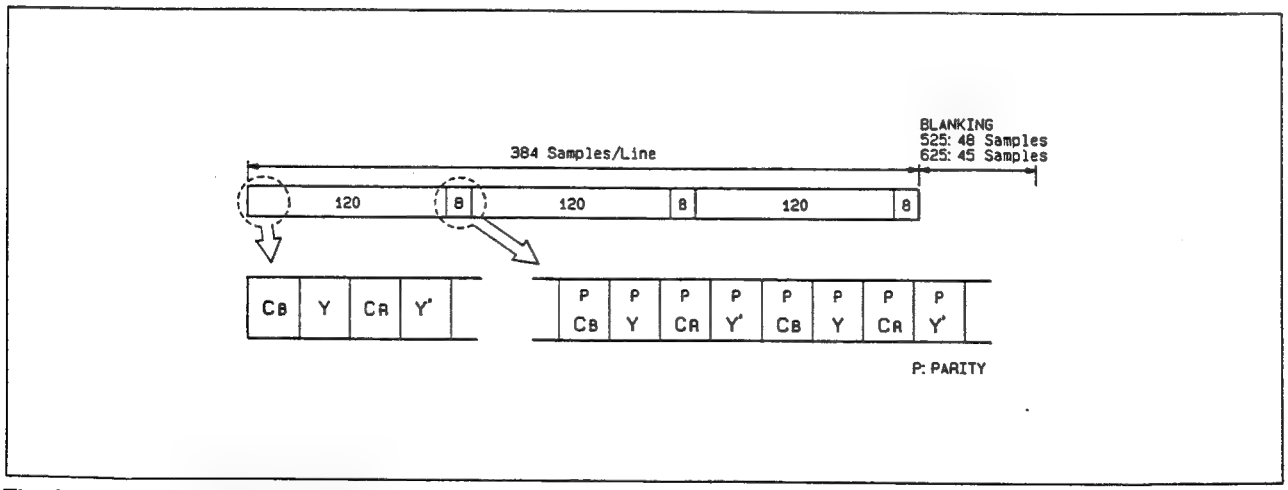



**Fig. 2-5-9. Outer Encoder Data Stream (VE-12 Board)**

After head interleaving, the data continue for 360 samples, and the parity slot must be installed so that the parity will be added by the outer encoder. This slot is installed by controlling the addresses of SRAM ICF24 in the previous stage of the outer encoder.

Write address counter ICK27 provides straight counting but read address counter ICK26 uses the "ENRAD CNT EN" signal which is output from pin 17 of ICJ27 to provide straight counting in the data section and address holding in the parity section. This means that the final Y data of each block are held in the parity slot of the outer encoder input data.

The CXD1037G manufactured by SONY is employed for outer decoder ICF20. It features 2 parity words and 4 interleaving lengths in its operation mode.

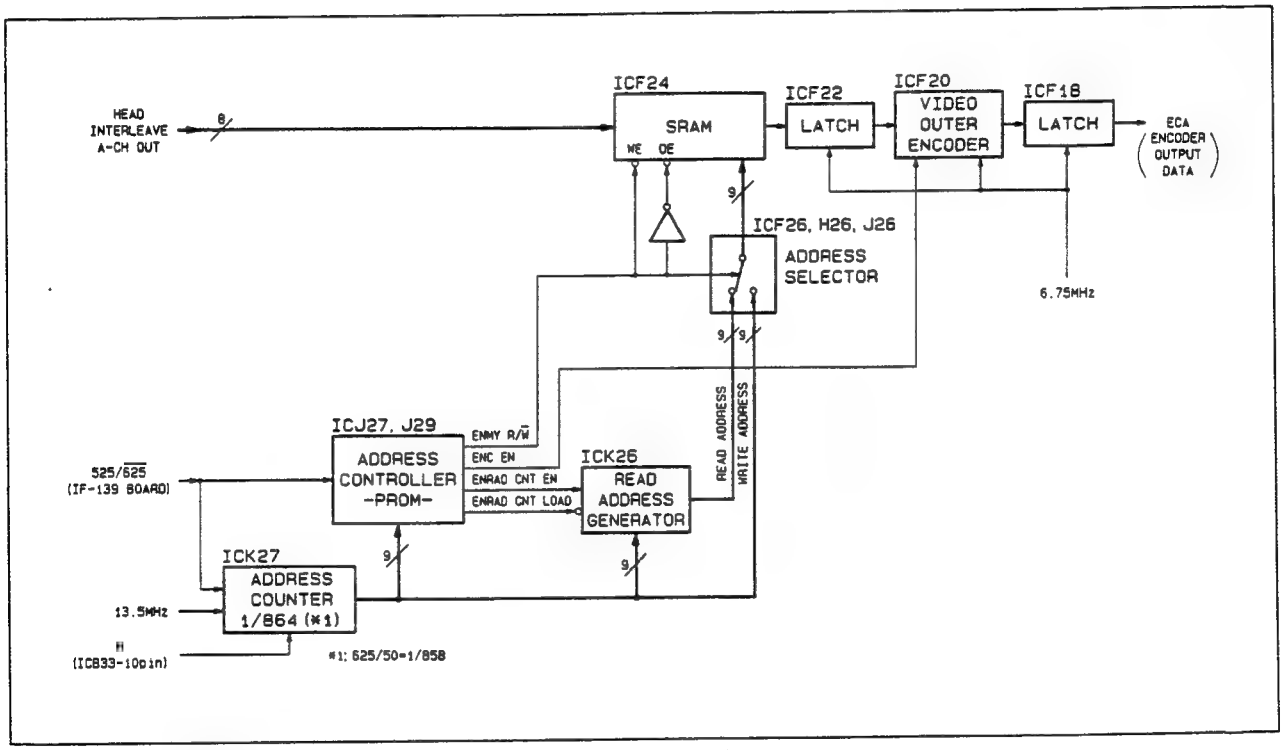



**Fig. 2-5-10. Block Diagram of Outer Encoder (Channel A/VE-12 Board)**

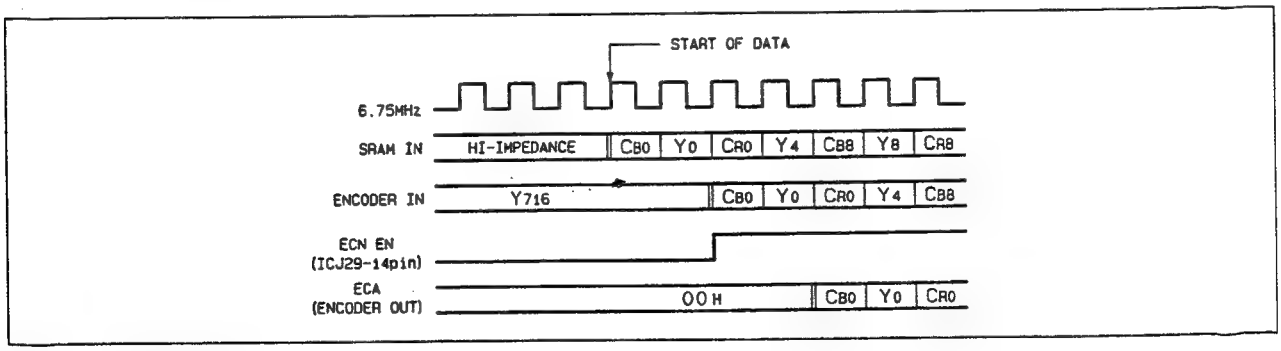



**Fig. 2-5-11. Timing Chart of Outer Encoder (VE-12 Board)**

### 7. Sector Array Shuffling Circuit (VE-12 board)

This data interleaving circuit is based on the D-1 format and it has a 1-segment (50-line) shuffling size. Processing applies to each channel individually, and the number of data samples per channel is equivalent to 18,000 (1440/4 × 50). If the outer error code is included, the number is equivalent to 19,200 [18,000 + (2×4×3×50)].

This circuit conducts shuffling by controlling the write address for the shuffling memory (SRAM).

Fig. 2-5-12 shows the structure of the sector array, Fig. 2-5-13 is a block diagram of the data processing section and Fig. 2-5-14 is a block diagram of the address generator circuit.

The data output from the outer encoder are allocated by serial-parallel-serial converter ICF13, F14, F15 and F16 and written into the SRAM for each $C_B$, Y, $C_R$ and Y' signal. During the write process, the write address counter ICA15 and A16 output is converted by PROM ICB13, B14, B15 and B17 so that it conforms to the D-1 format, and then shuffled. The first 3 "$C_B$, Y, $C_R$" data of the "$C_B$, Y, $C_R$, Y' ..." output data of the outer encoder are written with the same address but the fourth "Y"' data is processed with a different address from that of the other data.

The respective SRAMs are divided into 3 banks, with 1 bank corresponding to 1 segment. When data have been written into a specific bank, they are read out from a different bank. The start timing for reading is determined as referenced to the fall of the "SHSA: Shuffling Start A/B Channels" and "SHCC: Shuffling Start C/D Channels" signals which are sent from the TG-28 board. Fig. 2-5-15 is a timing chart of the shuffling memory bank selection and Fig. 2-5-16 shows both the memory control circuit and its timing.

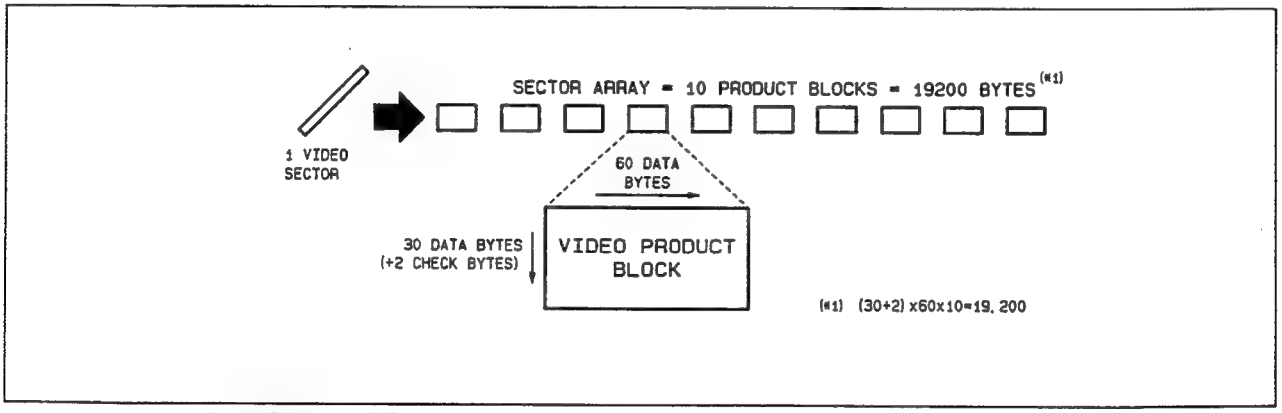



**Fig. 2-5-12. Sector Array Structure (VE-12 Board)**

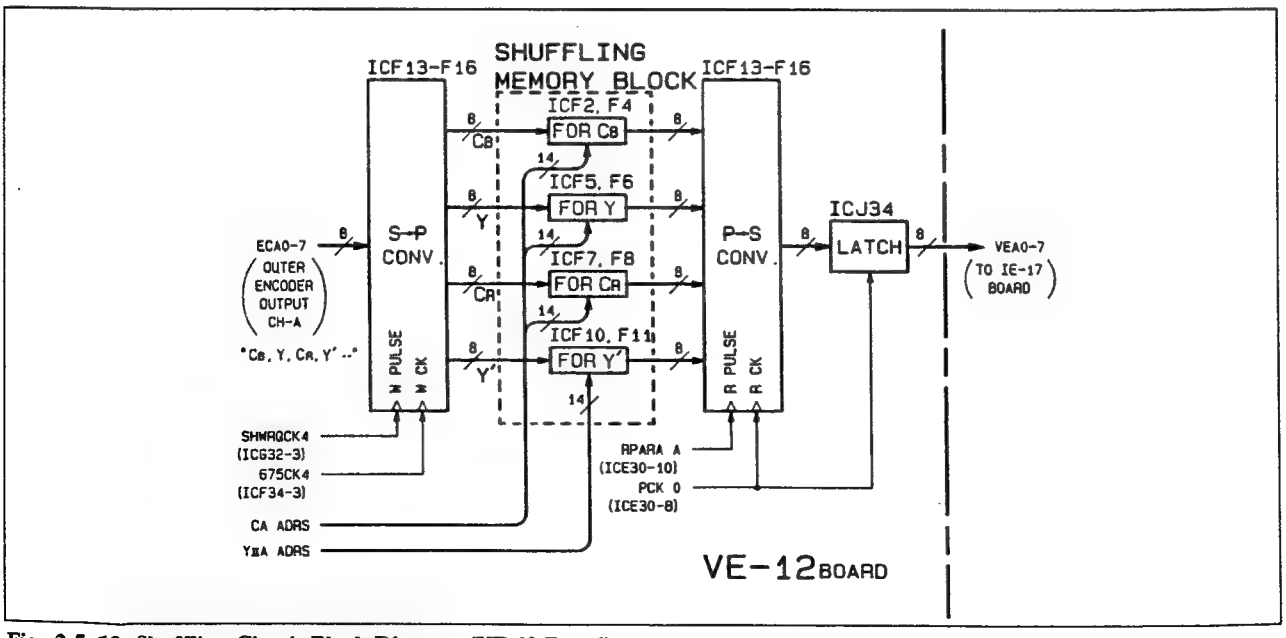



**Fig. 2-5-13. Shuffling Circuit Block Diagram (VE-12 Board)**

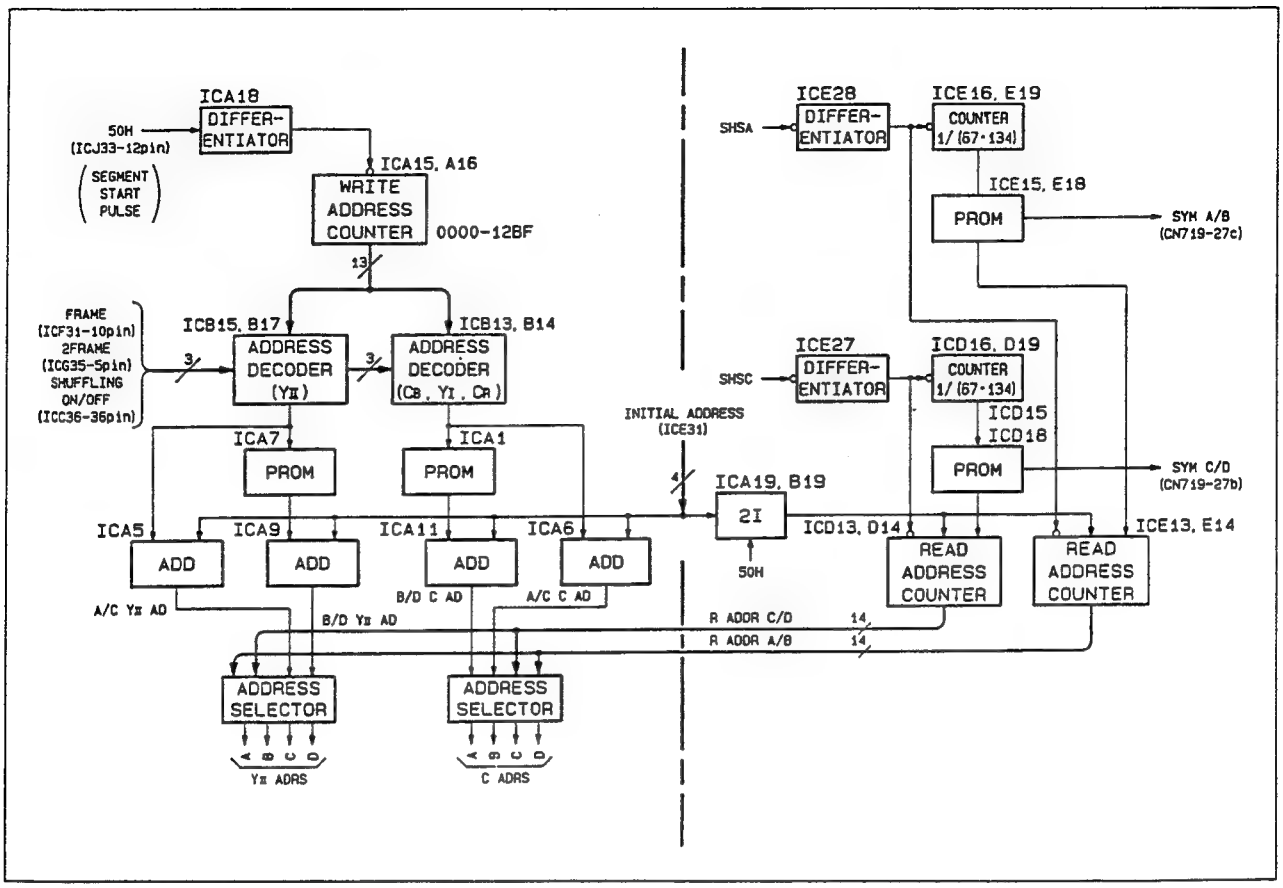



**Fig. 2-5-14. Address Generator Circuit Block Diagram (VE-12 Board)**

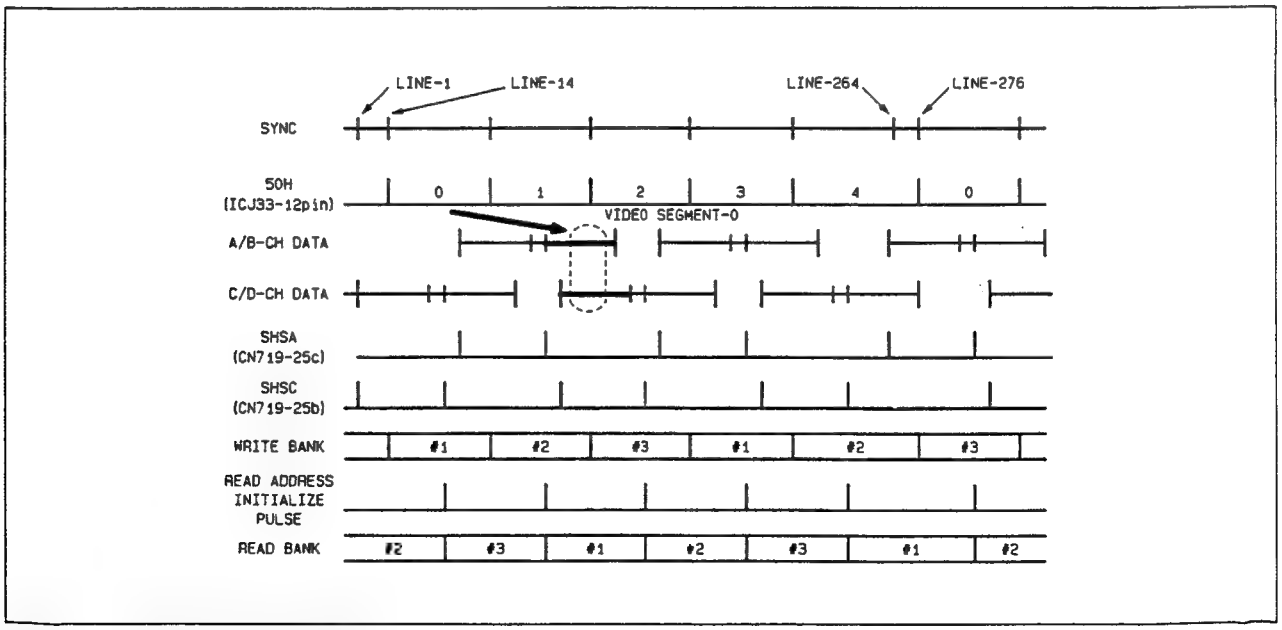



**Fig. 2-5-15. Shuffling Memory Bank Selection Timing Chart (VE-12 Board)**

In order for the data stream to be converted into the program track format when data are read from the memory, the enable pin (EN1, EN2) inputs of write address counter ICD13, D14, E13 and E14 are controlled, and slots are released for the inner error code, ID data, sync and audio data which are added by the IE-17 board.

The data which have been read out from the SRAM are converted into the serial data by serial-parallel-serial converter ICF13, F14, F15 and F16, and they are output to the IE-17 board. The data which have been input by the 6.75 MHz clock pulse are replaced by the 9.83682 MHz clock pulse in this circuit and then output.

At the same time as the data are converted into the program track format and output to the IE-17 board, this board also outputs the sync pulses (SYM A/B, SYM C/D) of channels A and C. These correspond to the sync blocks in the video data and they are output to the IE-17 board as the data position reference pulses. Fig. 2-5-17 shows the relationship between the shuffling start pulse "SHSA" and the sync pulse "SYM A/B."

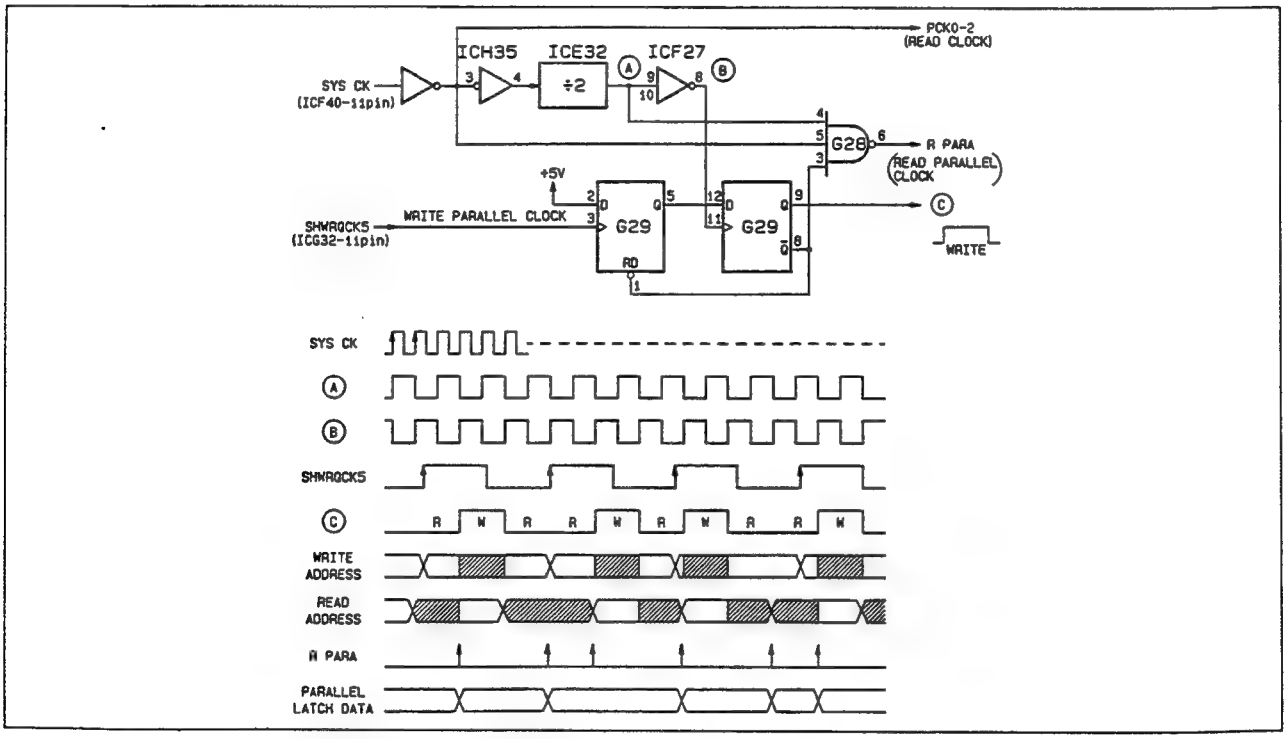



**Fig. 2-5-16. Read/Write Control Circuit (VE-12 Board)**

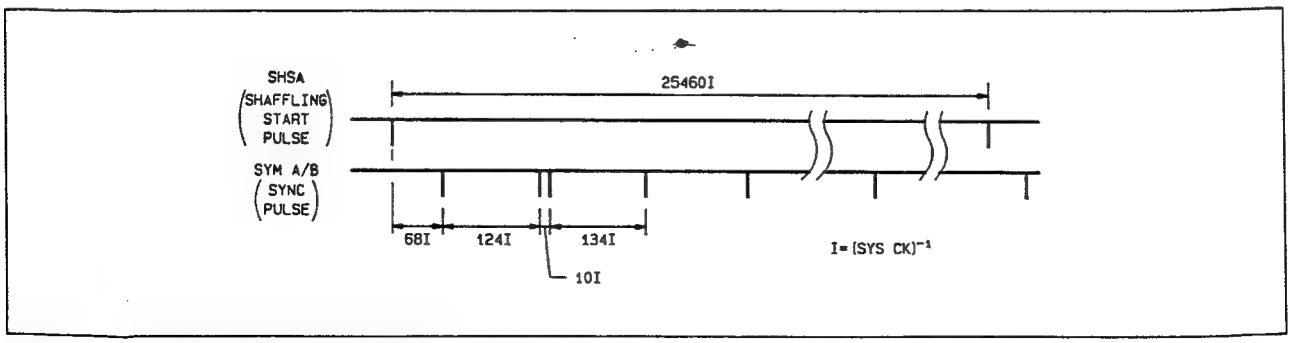



**Fig. 2-5-17. Relationship Between "SHSA" and "SYM A/B" (VE-12 Board)**

### 8. Bypass Circuit (VE-12 board)

The BYPASS-5 (8-8 mapping output) data are output from the VE-12 board to the VN-01 board for circuit checks while the BYPASS-4 (outer encoder output) data are output to the FM-09 board. Test switch S1 on the IF-139 board and test switches S1-3, S1-4 and S1-5 on the VE-12 board are used to specify the bypass mode and determine the bypass system.
The BYPASS-3 mode and BYPASS-2 mode control signals are output to the IE-17 board from the VE-12 board.
Fig. 2-5-18 is a timing chart of the BYPASS-4 and BYPASS-5 outputs.

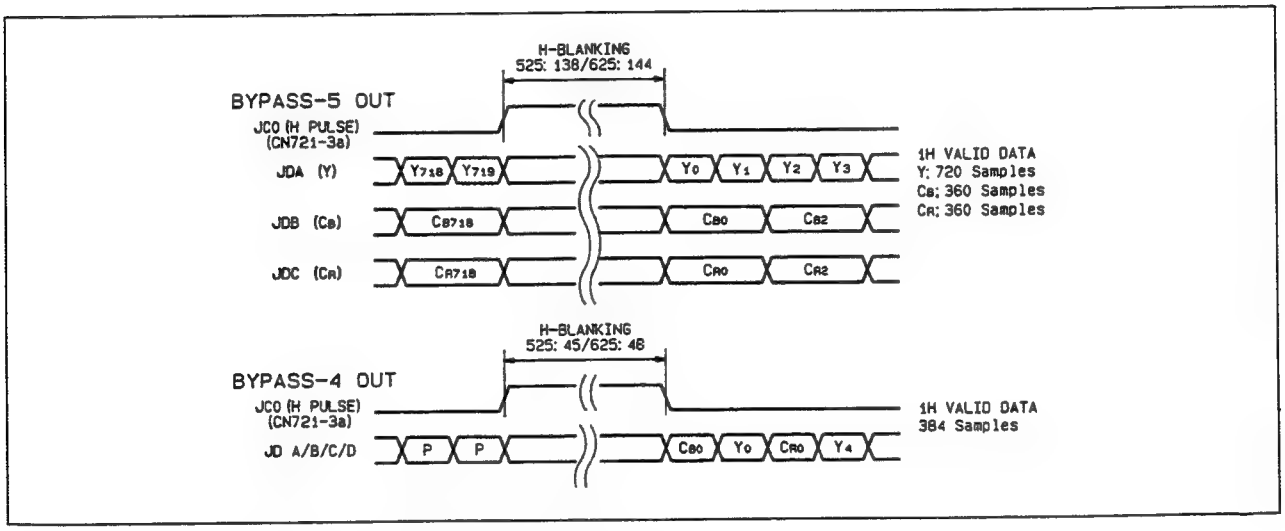



**Fig. 2-5-18. BYPASS-4/BYPASS-5 Timing Chart (VE-12 Board)**

## 4-2-6. FM-09 Board

Two FM-09 boards are used in each DVPC-1000. One board processes the signals for channels A and B; the other processes the signals for channels C and D.

### 1. Outline (FM-09 board)

The FM-09 board is composed of the following circuits. A circuit accompanied by an asterisk signifies that two identical circuits are mounted.

- 3-field memory * (Video deshuffling memory)
- 1H deshuffling memory *
- Outer decoder *
- Head de-interleaving circuit *
- 3-field memory control circuit
- Data output circuit
- Test circuit
- UPI

The sync data and video data in sync block units are supplied from the CI-01 board to the FM-09 board, the identification data (ID) in the data lines are extracted based on the sync phase, and the video data are fetched to the prescribed position in the 3-field memory. The video data, which are equivalent to 1 segment (50 lines) and which have been fetched to the 3-field memory, are first read out from that memory line by line. This stage deals only with generalized deshuffling in 1-line units; more detailed deshuffling within the lines is conducted in the next 1H deshuffling memory where a return is made to the outer code data series.

The errors in the deshuffled video data are corrected in the next stage outer decoder. The errors in two samples per outer block can be corrected in the outer decoder, error flags are raised for data which cannot be corrected and these are sent to the error concealment circuit on the VN-01 board.

After they have left the outer decoder, the video data are returned to their original data stream by the head de-interleaving circuit in the next stage, they are multiplexed on the motherboard with the data of the other two channels which have been output from the other FM-09 board, and they are then supplied together with the error flags to the VN-01 board.

During stunt playback, the data are played back in fragments and the amount of data changes according to the tape speed. For instance, with normal playback, the amount of information relating to the images input to the frame memory is equivalent to the amount of information relating to the images output from the frame memory. However, with slow playback, the amount of information relating to the images output from the frame memory is slightly less than that applying during normal playback, which makes it difficult to compose an image. Consequently, in the frame memory the data are read out from the same memory until a single field is almost totally composed. A single-chip microcomputer is employed for the 3-field memory and it is switched by the software used.

### 2. 3-Field Memory (FM-09 board)

The 3-field memory is composed of the following circuits.

- Data delay control circuit
- ID check circuit
- Write address generator
- 3-field memory
- Read address generator
- Flag memory

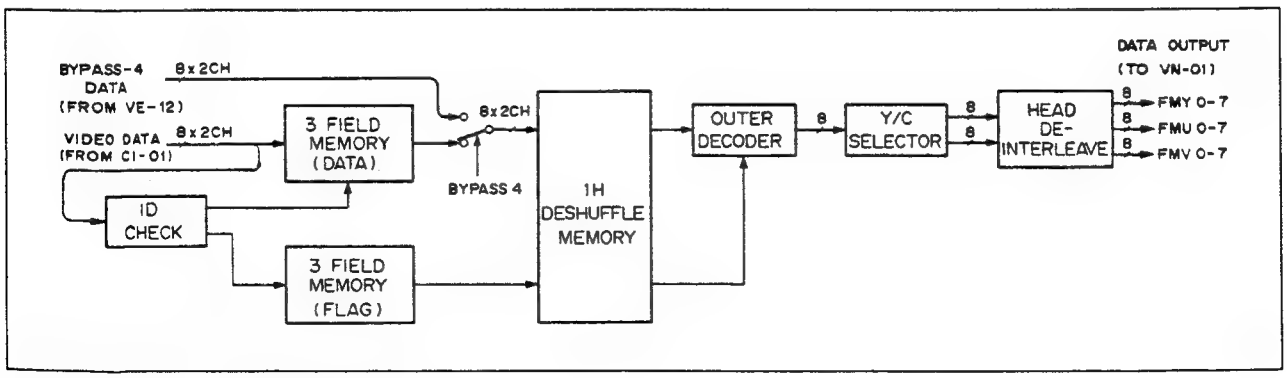



**Fig. 2-6-1. Function Diagram (FM-09 Board)**

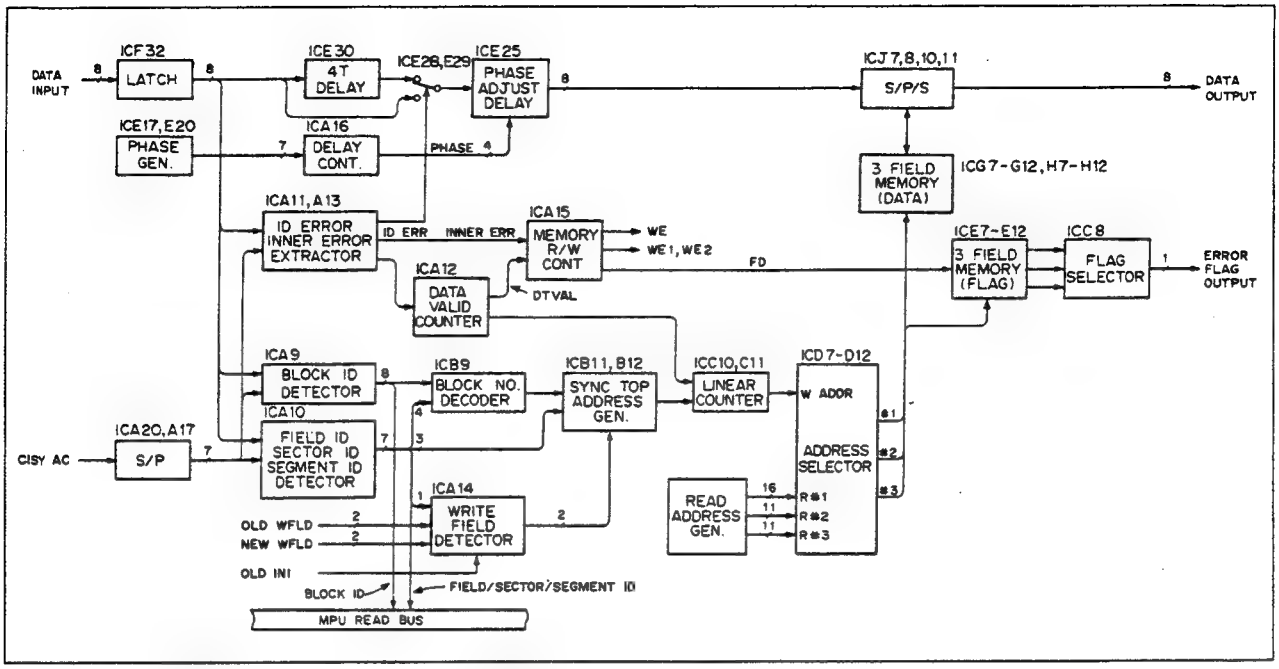



**Fig. 2-6-2. 3-Field Memory (Channels A/C, FM-09 Board)**

**(1) Data Delay Control Circuit (FM-09 board)**

The sync intervals are known to undergo change when stunt playback is conducted or when bit slip occurs.

Since the 3-field memory employs DRAMs, the data of 6 samples are parallel processed and also, in order for the input data to be written at the prescribed position in the 3-field memory, it is necessary for the phase of the serial-parallel converter to be initialized by the sync signal or for the phase of the input data to be aligned with the phase of the serial-parallel converter.

In this circuit, the input data are delayed by ICE25 (ICE27) and synchronized with the phase of the free-running serial-parallel converter ICJ7, J8, J10 and J11 (ICJ1, J2, J4, J5). Prior to proceeding with the delay control, 4 inner code words in the input data between the first inner code block and second inner code block are removed by ICE28-E30 (ICF28-F30), they are converted into 1 sync block/120 samples continuous data, and then fetched to the 3-field memory. If there are no sync data among the input data, the data will not be fetched to the memory.

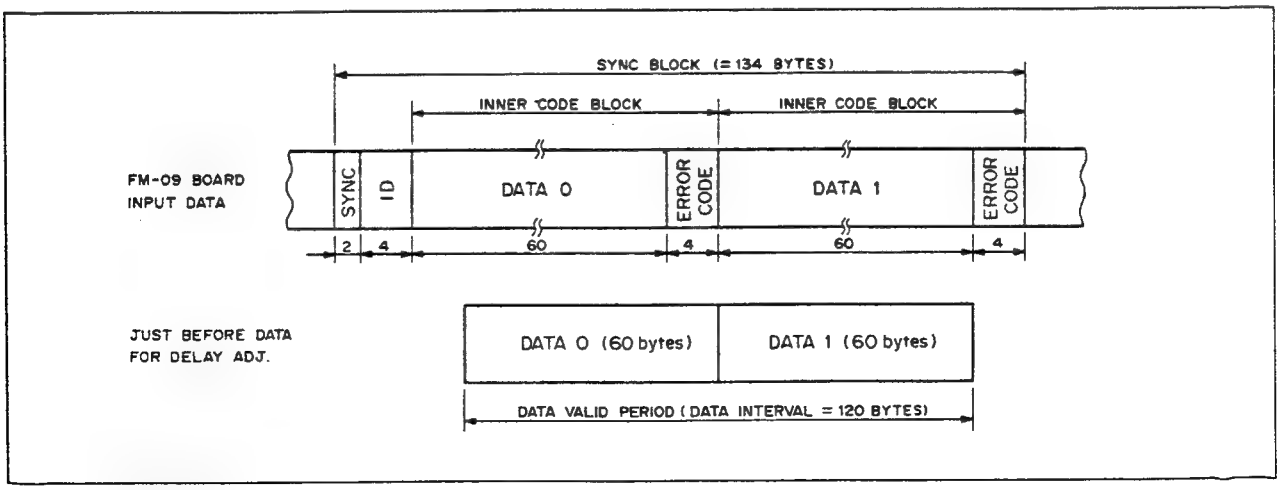



**Fig. 2-6-3. Data Delay Control (FM-09 Board)**

**(2) ID Check Circuit (FM-09 board)**

When the data reach ICA11 and A13 (ICA3, A5), the ID data among the data are extracted, based on the phase of the "CISY AC/BD" sync pulse which is supplied from the CI-01 board, the ID error data (sector ID error, block, ID error) is checked, a check is made of whether or not the extracted ID is a sector ID that actually exists, and the ID error flags "*IDERA" (TP14) and "*IDERB" (TP24) are output.

Inner error flags "*INERA" (TP15) and "*INERB" (TP25) are extracted from among the data lines. If there is an ID error or inner block error, data writing into the 3-field memory is prohibited, only the proper data are written into the memory as a result, and temporary concealment takes place in the time base direction. If the processor is operating in the test mode and switch S1-3 is set to ON, it is still possible to fetch the data to the memory even when errors have occurred in the inner blocks.

**(3) Write Address Generator (FM-09 board)**

In this block, the field ID, sector ID, segment ID and sync block ID in the data lines are referenced and the top write address of the sync block is generated. There are 4 fields in the field ID, fields 0 through 3 (525/60 system). For the 625/50 system, there are 8 fields in the field ID, field 0 through 7. The data are shuffled in this 4-field sequence.

The first process to be undertaken is 4-field sequence deshuffling in which the block numbers are converted into one type of block ID by ICB9 (ICB2) from the field ID and block ID latched by ICA9 and A10 (ICA1, A2). The block IDs used internally range from 2 to 162. When any other block ID is input, the write addresses are all set to "1" (invalid addresses) and memory writing is prohibited. The same operation results with a value in which the segment ID does not exist.

When 1 field area in the 3-field memory is specified by the single-chip microcomputer (3-field memory controller, ICJ14), the top address of the sync block is determined. What happens to the 120 sample (120 samples/6 parallel) data in the sync block is that linear addresses are output from the address counter IC10 and C11 (ICC5, C6).

Since, in the case of slow motion, the data must be written alternately into a multiple number of field memories, two field addresses, "OLD WFLD" and "NEW WFLD," are output from the single-chip microcomputer to the field memories. The "OLD WFLD" and "NEW WFLD" addresses are initialized in the vicinity of the write side field center, and they are subsequently switched by the hardware at the field ID (LSB) edge section.

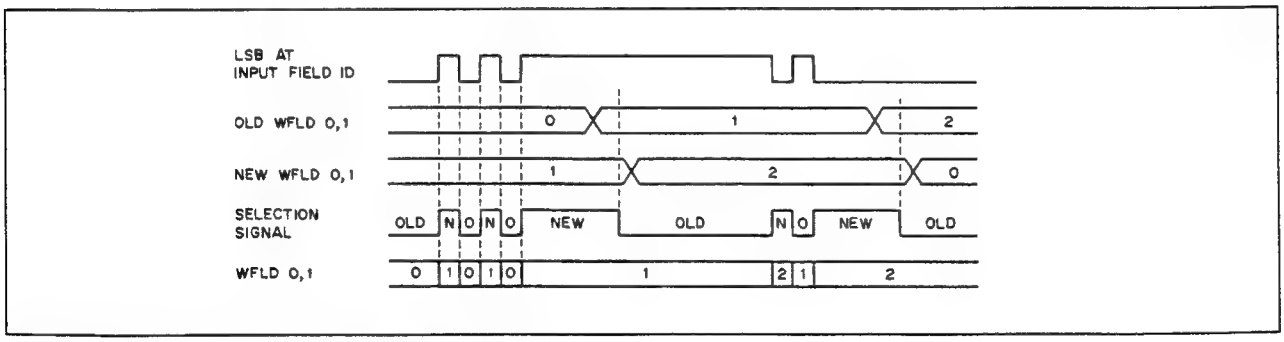



**Fig. 2-6-4. Field Memory Switching (FM-09 Board)**

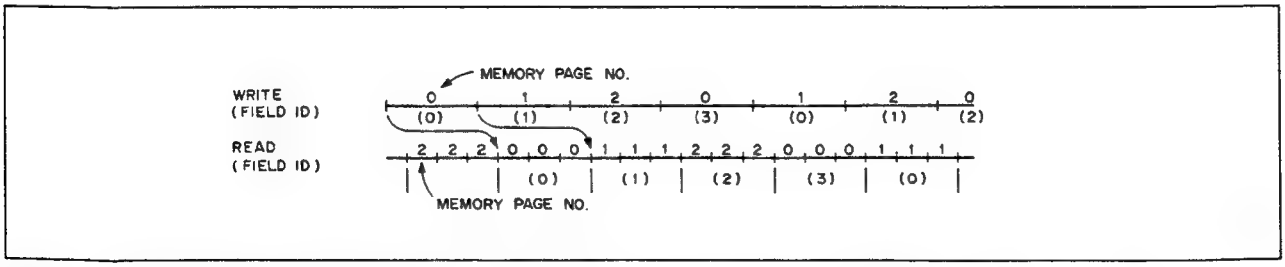



**Fig. 2-6-5. 3-Field Memory Control (Slow Motion at 1/3 Normal Tape Speed/FM-09 Board)**

**(4) 3-Field Memory (FM-09 board)**

The frame-feed images of fields during slow motion are created by the 3-field memory.

One example of this is the timing chart for the 3-field memory in Fig. 2-6-4 which indicates what happens during slow motion at one-third of normal tape speed. It shows that while a specific field is being read out, the other two fields must be written.

A total of 6 64K × 4-bit DRAMs are connected in parallel with the 3-field memory for one channel, making a total of 12 DRAMs used overall. This means that the memory size for one channel is 384K bytes. This machine has two FM-09 boards and features memories for 4 channels in all.

**(5) Read Address Generator (FM-09 board)**

The read addresses are controlled and deshuffling is performed. As described in the VE-12 board section, the video data shuffling pattern is such that $C_B/Y/C_R$ are put altogether and Y' provides a fixed offset for these. In addition, the 3-field memory provides parallel processing for the 6-sample data, there is no relationship between the multiples of the $C_B/Y/C_R/Y'$ 4 samples, and a total of 3 read addresses are made available for every 2 samples.

The video shuffling size is 1 segment (50H) and this is composed of data amounting to 18,000 samples per channel. The 3-field memory provides parallel processing for 6 samples, which makes it difficult to provide the kind of detailed shuffling specified by the format. The 3-field memory therefore reads out the data required line by line and performs generalized deshuffling, after which detailed deshuffling is undertaken by the 1H deshuffling memory.

First, the reference address is generated by ROM ICE13 and E15. Next, the other two addresses are generated by ICC13-C15.

In order to facilitate the generation of the read addresses, the outer direction of the memory map is made identical with the low-order bits (A0-A10) of the addresses. This means that only the most significant bits of the address are counted up in sequence by the counter so that the outer data can be read out. As a result, only the most significant addresses in the row direction (outer direction) are generated from ROM ICE13 and E15.

An example of this is shown in Fig. 2-6-6 which indicates the memory map in a segment of a field. The explanation below follows the figure.

The first samples of sync blocks 0, 5, 10 to 155 are assigned addresses $0000_H$, $0800_H$, $1000_H$ to $F800_H$.

Therefore, the initial value $0000_H$ is first assigned by ROM ICE13 and E15, the counter subsequently starts counting up and the read addresses are generated. In order for only the most significant bits to be counted up, the counter output is supplied to multiplexer ICD13 and the addresses are replaced.

The read address counter is composed of the 50H counter and the segment counter which are initialized every field, and the outer counter which is initialized every line.

FIELD = 0 SEGMENT = 0

| SYNC | 0 | 1 | 2 | 3 | 4 |
|---|---|---|---|---|---|
| 0 | 0000-0013 | 0014-0027 | 0028-0038 | 003C-004F | 0050-0063 |
| 5 | 0800-0813 | 0814-0827 | 0828-0838 | 083C-084F | 0850-0863 |
| 10 | 1000-1013 | 1014-1027 | 1028-1038 | 103C-104F | 1050-1063 |
| 15 | 1800-1813 | 1814-1827 | 1828-1838 | 183C-184F | 1850-1863 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 135 | D800-D813 | D814-D827 | D828-D838 | D83C-D84F | D850-D863 |
| 140 | E000-E013 | E014-E027 | E028-E038 | E03C-E04F | E050-E063 |
| 145 | E800-E813 | E814-E827 | E828-E838 | E83C-E84F | E850-E863 |
| 150 | F000-F013 | F014-F027 | F028-F038 | F03C-F04F | F050-F063 |
| 155 | F800-F813 | F814-F827 | F828-F838 | F83C-F84F | F850-F863 |

OUTER DIRECTION

**Fig. 2-6-6. Address Map (FM-09 Board)**

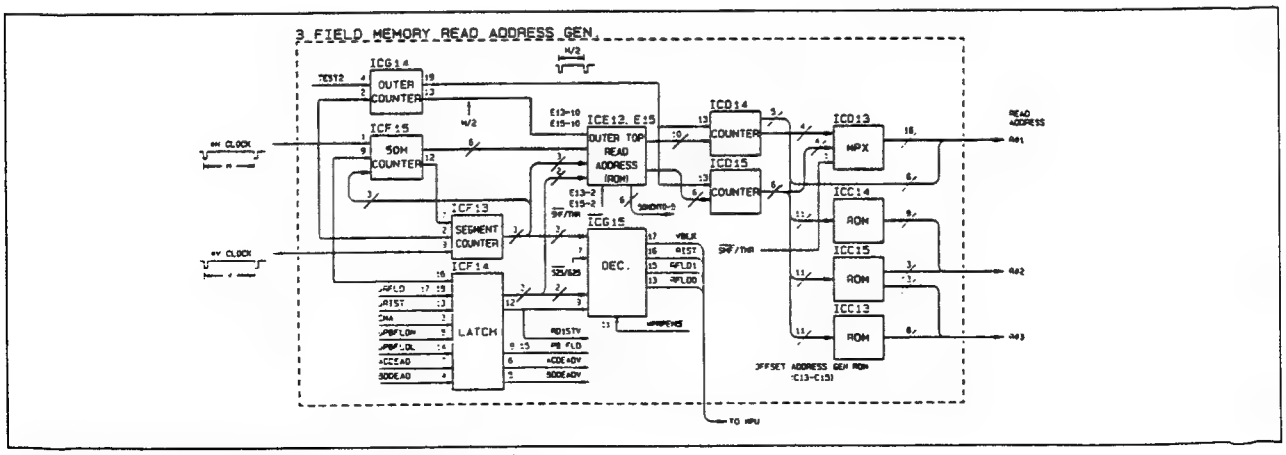



**Fig. 2-6-7. Read Address Generator (FM-09 Board)**

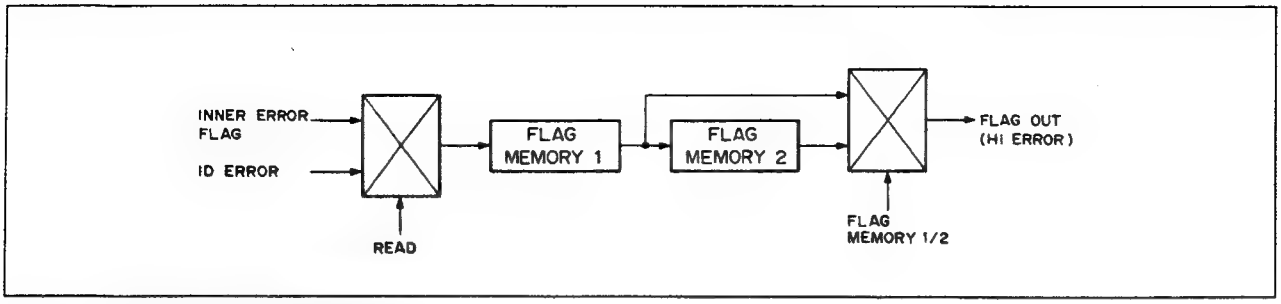



**Fig. 2-6-8. Flag Memory (FM-09 Board)**

**(6) Flag Memory (FM-09 board)**

In order to perform temporary concealment, all the data which have once been read out from the memory are treated as error data (OLD) by the 3-field memory. When new data are fetched to the memory, no error (NEW) is indicated by the flag of the address concerned.

Since there may be cases with slow motion when the same field memory is read any number of times, error flags are sent to succeeding flag memory 2 ICE8, E10 and E12 (ICE2, E4, E6) from flag memory 1 ICE7, E9 and E11 (ICE1, E3, E5) every time a flag is read out from flag memory 1. With slow motion, error flag are read out from flag memory 1 only once at the outset and on all subsequent occasions they are read out from flag memory 2 until the read field is switched.

In order for the flag memory addresses and data memory addresses to be used in common, 3 load addresses must be supplied to the flag memory as with the data memory. This is why six 64K × 1-bit SRAMs are employed as the flag memory for each channel.

**3. 1H Deshuffling Memory (FM-09 board)**

In the 3-field memory, the 50H shuffling data are roughly shuffled and then read out from the memory line by line. After they have been read out, they are supplied to the 1H deshuffling memory ICH29 and H30 (ICJ29, J30) where more detailed deshuffling within the lines is conducted in accordance with the line numbers.

The read address generator of the 1H deshuffling memory is composed of ROM ICE23 for generating the row start pointers, counter ICF23 and F25 for determining the row numbers in the outer blocks, and ROM ICF26 for determining the final deshuffling pattern by the row numbers.

In order to facilitate the processing at the Y/C selector which is placed before the head de-interleaving circuit described below, the readout sequence for the outer block data differs for channels A/C and for channels B/D.

The Y/C data in the channel A data and channel B data (or in the channel C data and channel D data) are separated by the Y/C selector, and the Y or C data must not be read out simultaneously for channels A and B for writing into the head de-interleaving memory. Consequently, control is exercised so that the Y and C data are not duplicated onto each other in channels A and B (or channels C and D) respectively.

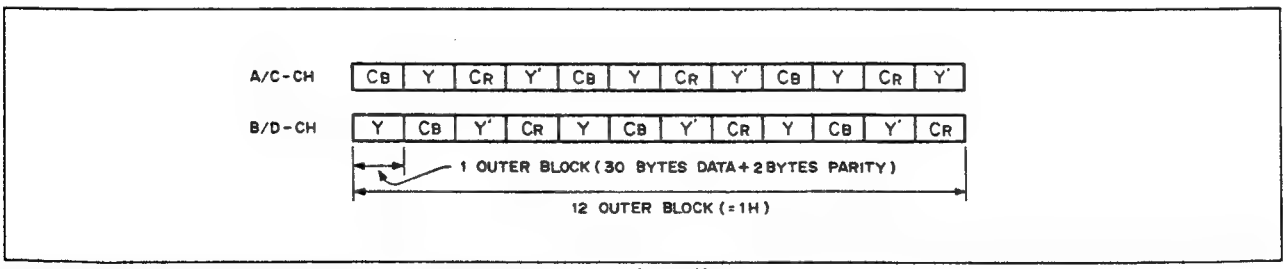



**Fig. 2-6-9. Readout Sequence From 1H Deshuffle Memory (FM-09 Board)**

### 4. Outer Decoder (FM-09 board)

- Galois field: GF(256)
- Field generating polynomial: $P(X) = X^8 + X^4 + X^3 + X^2 + 1$
- Code generating polynomial: $G(X) = (X + \alpha^0)(X + \alpha)$
  Where $\alpha^0$ and $\alpha$ are the root of G(X)
- Companion matrix

$$\alpha = \begin{vmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{vmatrix}$$

The outer decoder decodes Reed Solomon code (32, 30) that is determined by the above formula. It uses the pointer flags generated by the inner code, and permits erasure correction of up to two samples.

When errors have occurred in 2 samples at the outer code block, the syndromes can be expressed as follows.

If it is assumed that the error positions are "i" and "j" and that the error sizes are "ei" and "ej," then syndromes "S0" and "S1" are as follows:

$S0 = ei + ej$

$S1 = \alpha^i ei + \alpha^j ej$

Both "i" and "j" are already known by the inner code and so the error sizes can be calculated as below.

$$ei = \frac{S0\,\alpha^j + S1}{\alpha^i + \alpha^j}$$

$$ej = \frac{S0\,\alpha^i + S1}{\alpha^i + \alpha^j} = S0 + ei$$

The above processing is accomplished by ICH21 and H25 (CXD1038G manufactured by SONY). In the normal playback mode, EE mode and in any slow playback mode at speeds of less than half the normal tape speed, the outer correction function is set to ON. In any shuttle mode at speeds of more than half the normal tape speed, however, the 3-field memory is operated in the 1-field mode so that the data inside the memory are composed of the data of a multiple number of fields. This means that there will be a difference between the data which result from encoding the data which were first input to the outer decoder and the data which are freshly input to the outer decoder and that a discrepancy will also arise in the syndromes. The outer correction function is set OFF since erroneous correction is performed when correction is undertaken in any shuttle mode with a speed of more than half the normal tape speed.

When the number of input erasure flags is 3 or more, the ICH21 and H25 erasure correction mode is automatically suspended and the error is identified from the syndrome. If all the syndromes are zero, this is taken to indicate that there is no error and output follows without any flags being raised.

When the head of a particular channel is damaged, the data in the channel where the damage has been suffered are not updated and all the flags of this particular channel input to the outer decoder are set to the error status. However, since the error data are fetched to the memory, the old data are read out. As a result, the syndrome is set to zero and concealment is not performed without the output flags of the outer decoder being raised. Consequently, the data of only one channel are output a freeze picture.

In order to avoid the problems outlined above, the input erasure flags are selected and the output flags which are obtained by the outer decoder are not selected, when the number of the erasure flags is 3 or more.

### 5. Head De-interleaving Circuit (FM-09 board)

This circuit functions to return the data, which have undergone head interleaving on the VE-12 board, to the original time series.

In the input section of this circuit, the Y data/$C_B$, $C_R$ data are respectively separated for channels A and B (or for channels C and D) and they are written into the Y (luminance) memory ICA30 or C (chroma) memory ICB29. The data are written linearly into the memories and when they are read out from the memories, the memory addresses are controlled and the data are restored to the original time series.

The C (chroma) data are further separated by ICB31 into the $C_B$ and $C_R$ data and output.

### 6. 3-Field Memory Control (FM-09 board)

This circuit determines the field switching from the field ID, segment ID and block ID in the input data and it controls which of the fields of the 3-field memory the data are to be written into or read out from. This control is exercised in every respect by the ICJ14 single-chip microcomputer. Furthermore, it is here that the freeze picture output is controlled.

Based on the status and continuity of the field ID and segment ID which have been fetched, the ICJ14 single-chip microcomputer determines the direction in which the tape is running and it also determines whether it has been possible to secure the data of the previous field throughout the entire field when the data of the following field have been input. Another function of ICJ14 is field memory switching. When the tape is traveling in a shuttle mode at more than half the normal tape speed, it is not possible to acquire data throughout the entire screen area and, therefore, only the memory for 1 field is used to emphasize the movements of the images.

### 7. Data Output Circuit (FM-09 board)

The DVPC-1000 is provided with two FM-09 boards. The video data, error flags and control signals (F, V and H) are output from these boards. They all feature wired OR connections on the motherboard (MB-132) and they are supplied to the VN-01 board.

The rate of the data supplied to the VN-01 board is 13.5 MHz (Y) but since there are two FM-09 boards, this gives a rate of 6.75 MHz (Y) for each board.

The output enable status of the output driver is switched ON/OFF every 6.75 MHz. The signal on the motherboard identifies whether the FM-09 board for channels A and B or whether the FM-09 board for channels C and D is selected.

Whether or not two FM-09 boards are provided is determined in each respective board and in cases where only one FM-09 board has been provided, output enable control is prohibited. In this case, therefore, 2:1:1 images are output.

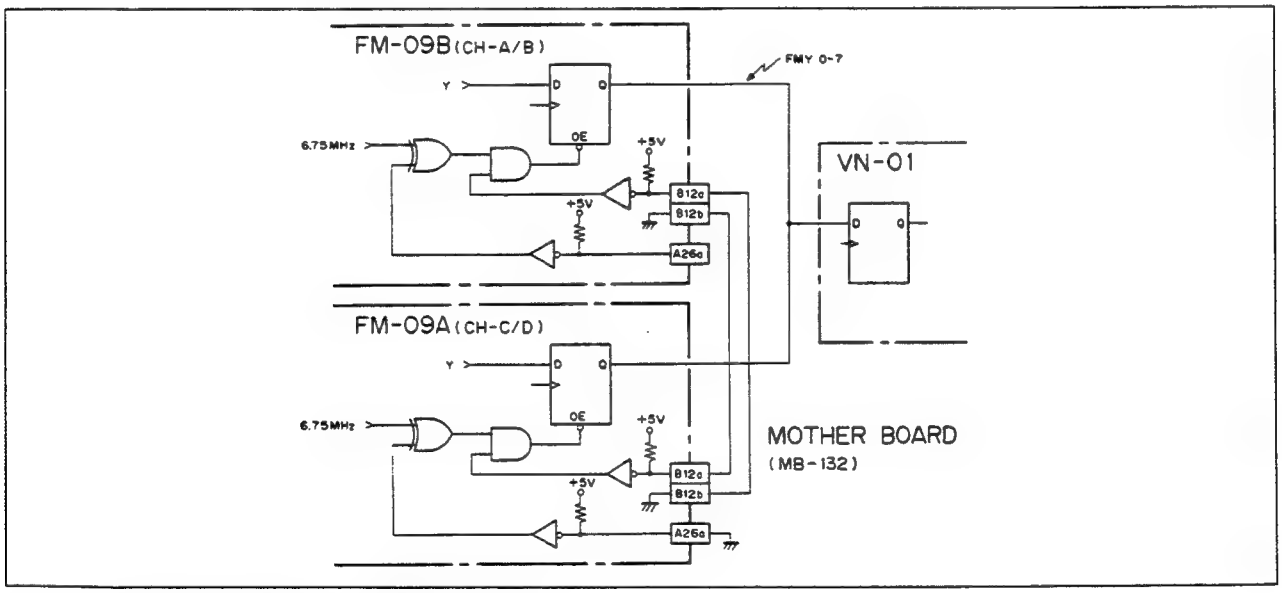



**Fig. 2-6-10. Output Channel Control (FM-09 Board)**

## 4-2-7. VN-01 Board

The VN-01 board may have the board number suffix of "−11," "−12" or "−13." In each case, the configuration of the circuitry is virtually identical although the reference numbers of some parts differ between boards with the "−11/12" suffix and boards with the "−13" suffix. The following description applies to a board with the "−11" suffix unless otherwise noted.

The VN-01 board is composed of the following circuits.

- 8-8 demapping circuit
- Concealment circuit
- Interface decoder

The Y, $C_R$ and $C_B$ video signals and the error flags are supplied from the FM-09 board to the VN-01 board. These data are first demapped and then supplied to the spatial concealment circuit. Based on the input error flags, the concealment circuit functions to correct any outer residual errors.
After the errors in the video data have been corrected, the horizontal and vertical blanking data are added, they are converted into the SMPTE RP-125 (or EBU TECH3246E) format by the following interface encoder, and they are supplied to the VA-45 board. At the same time, these signals are output externally through the DIGITAL VIDEO OUTPUT connector on the connector panel.
Furthermore, the BYPASS-5 (8-8 mapping output) data are input from the VE-12 board to the 8-8 demapping circuit on this board.

### 1. Data Input Circuit (VN-01 board)

Supplied to the VN-01 board are not only the BYPASS-5 Y(JDA)/$C_B$(JDB)/$C_R$(JDC) video data and the horizontal pulses (BP5HSTA) from the VE-12 board but also the main line Y(FMY)/$C_B$(FMU)/$C_R$(FMV) video data and horizontal pulses (FMHSTA) from the FM-09 board. The frame pulse (FMFRM) supplied from the FM-09 board are used communally.
These signals are input to input selector circuit ICC31-C33 and ICJ31-J32, one of these options is selected and the signals are supplied to the 8-8 demapping circuit.



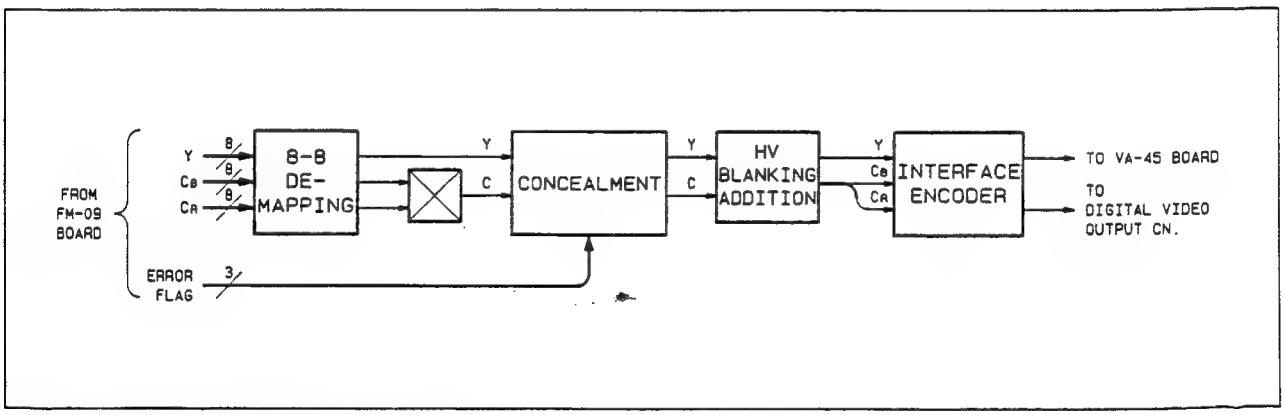



**Fig. 2-7-1. Function Diagram (VN-01 Board)**

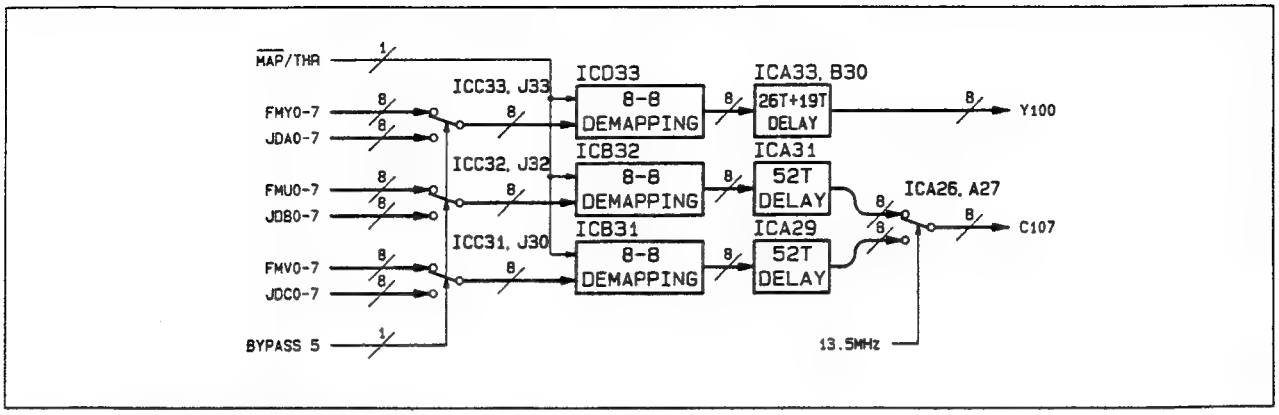



**Fig. 2-7-2. Data Input Circuit and Demapping Circuit (VN-01 Board)**

### 2. 8-8 Demapping Circuit (VN-01 board)

This conducts processing which is the reverse of that provided by the 8-8 mapping which takes place on the VE-12 board. The Y, $C_B$ and $C_R$ data supplied from the FM-09 board are supplied to the least significant 8 bits (A0-A7) of the PROMs. The 8-8 demapping on/off control signal "MAP/THR" is supplied to the most significant bit (A8). As mentioned in the description of the VE-12 board, the process of mapping applies only to the video data portion. Consequently, the process of demapping also applies to the same portion and for any other data portions, the "MAP/THR" signal is set high and the data are output without any modification whatsoever.

The demapped data are supplied to the delay circuit for preparation of the interpolation data and replacement data. The $C_B$ and $C_R$ data are time division multiplexed in multiplexer ICA26 and A27 in the stage prior to the delay circuit by means of the 13.5 MHz clock pulse, and they are processed as chroma (C) data.

### 3. Error Flag Control Circuit (VN-01 board)

The error flags (FM FLG Y/U/V; ERROR = "High") constitute the reference information for the concealment process. Concealment processing itself is undertaken only when the error flags have been raised. In addition, only the video line data conduct the actual concealment and it is not possible to use for the concealment any data except the video data which cannot be correlated. This means that an error flag will be raised immediately if data other than the video line data are supplied. When the test mode is established, it is possible to set the concealment to OFF by setting concealment off switch S1-2 to the ON position. This will results in forcibly setting the error flags to the low level (no error) by means of ICC28 in this circuit.

The "FM FLG Y" error flag is supplied to the VN-01 board with 13.5 MHz sampling, and the "FM FLG U" and "FM FLG V" error flags are supplied to the same board by 6.75 MHz sampling. The "FM FLG U" and "FM FLG V" error flags are multiplexed by ICB27 at the 13.5 MHz frequency in the same way as with the video data and they are sent to the delay circuit in the next stage.

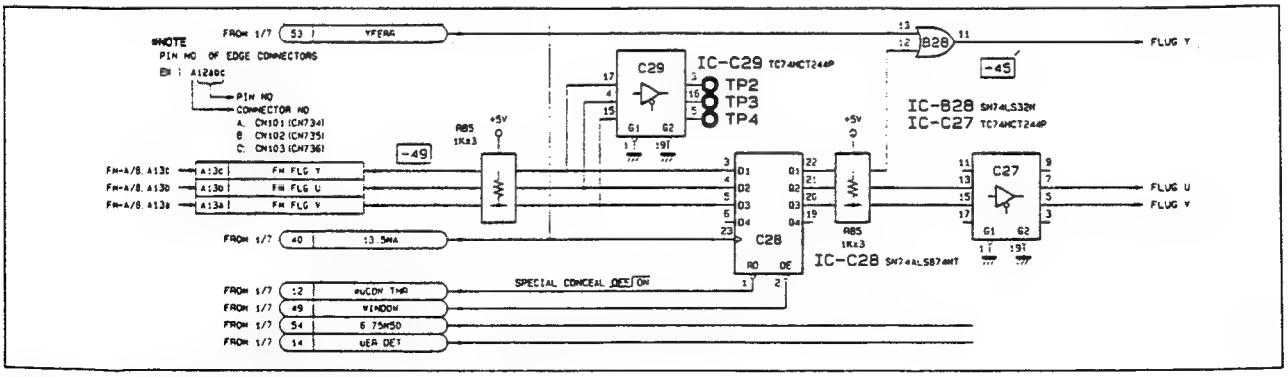



**Fig. 2-7-3. Error Flag Control Circuit (VN-01 Board)**

**4. Delay Circuit (VN-01 board)**

The demapped Y data and C data are then supplied to this circuit which prepares the interpolation data and replacement data.

The circuit provides amounts of delay equivalent to $\tau/10\tau/19\tau/1H\text{-}4\tau/1H\text{-}15\tau/3\tau/4\tau$. The circuit diagram gives 3-digit numbers which indicate the amounts of delay, with "Y100" as standard, a 3-digit number indicates the delay in 1H unit, and a 2-digit and 1-digit numbers denote the delay in $\tau$ units. For instance, "Y213" denotes data which have been delayed by an amount equivalent to "$1H + 13\tau$."

Given as an example below are the replacement data and interpolation data for "Y213."

As shown in Fig. 2-7-4, the data of the 8 proximity points required for replacement, namely the "Y112," "Y113," "Y114," "Y212," "Y214," "Y312," "Y313" and "Y314" data, are created by the delay circuit.

The following data are prepared by the adder circuit as the interpolation data.

Y213H = (Y212 + Y214)/2
Y213V = (Y313 + Y113)/2
Y213D− = (Y314 + Y112)/2
Y213D+ = (Y312 + Y114)/2

The "Y213H" interpolation data in the horizontal direction are created by ICB5 (CXD1039G).

The above details apply to the video data and in the same way the necessary data for the error flags are created by delay circuit ICB17, B18, C17, C18, D17, G16 and H16.

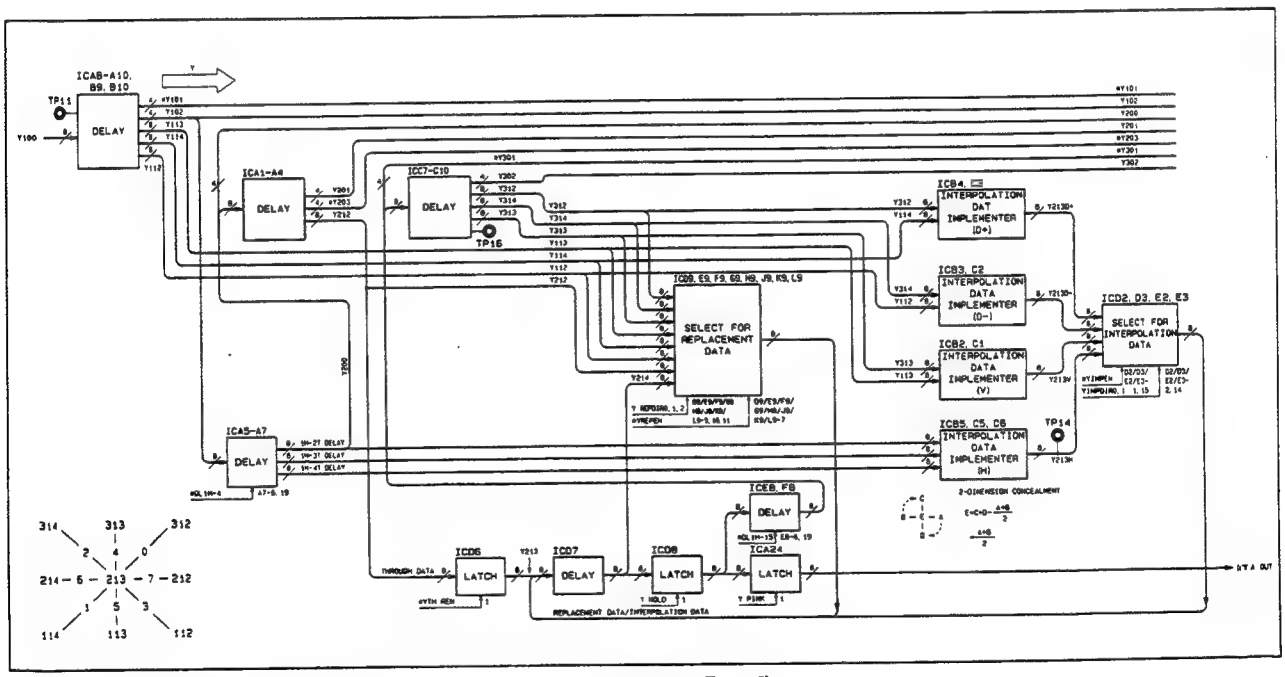



**Fig. 2-7-4. Delay Circuit and Concealment Circuit (For Y Data/VN-01 Board)**

### 5. Ideal Direction Detector (VN-01 board)

This circuit serves to reference the values of the adjacent pixels for each of the pixels on the screen and calculate the ideal direction. Concealment is provided on the basis of the error flags of the various points and the ideal direction is determined by this calculation.

There are four directions: horizontal (H), vertical (V), top left diagonal (D−) and top right diagonal (D+). The ideal direction detector circuit calculates the correlation values of the directions (H, V, D− and D+) and it selects the direction of the minimum correlation value as the ideal direction. When the correlation values are identical, the direction is determined in the sequence of H, V, D− and then D+. The correlation values are calculated using the most significant 4 bits of the luminance (Y) signal.

The error data are not used for calculating the correlation values. Even if there is one direction for which the correlation value cannot be calculated, it means that it is not possible to calculate the ideal direction and the GIVE UP flag "YGUP09/10" (GIVE UP = low) is output.

### 6. Concealment Circuit (VN-01 board)

Based on the ideal direction (H, V, D−, D+ or give-up) which has been determined by the calculation and the error flags of the 8 points around the object point, the concealment circuits serve to check out the possibility of interpolation and replacement and to correct the error data. There are two concealment circuits, one for the Y data and the other for the C data, and their configuration is identical. The description here is confined to the concealment circuit for the Y data.

Fig. 2-7-6 shows the concealment algorithm. ICB20 and D20 (G18 and K18) serve to identify whether interpolation is possible whereas ICB21 and D21 (G19 and K19) identify whether replacement is possible. The signal denoting the ideal direction and the error flags of the 8 points (8-neighborhood) around the object point are supplied to this identification circuit. Based on these informations, the possibility of concealment (interpolation or replacement) is identified and the interpolation/replacement direction is determined. If the VN-01 board has the "−13" suffix, ICC4 (E4) is responsible for the above identification.

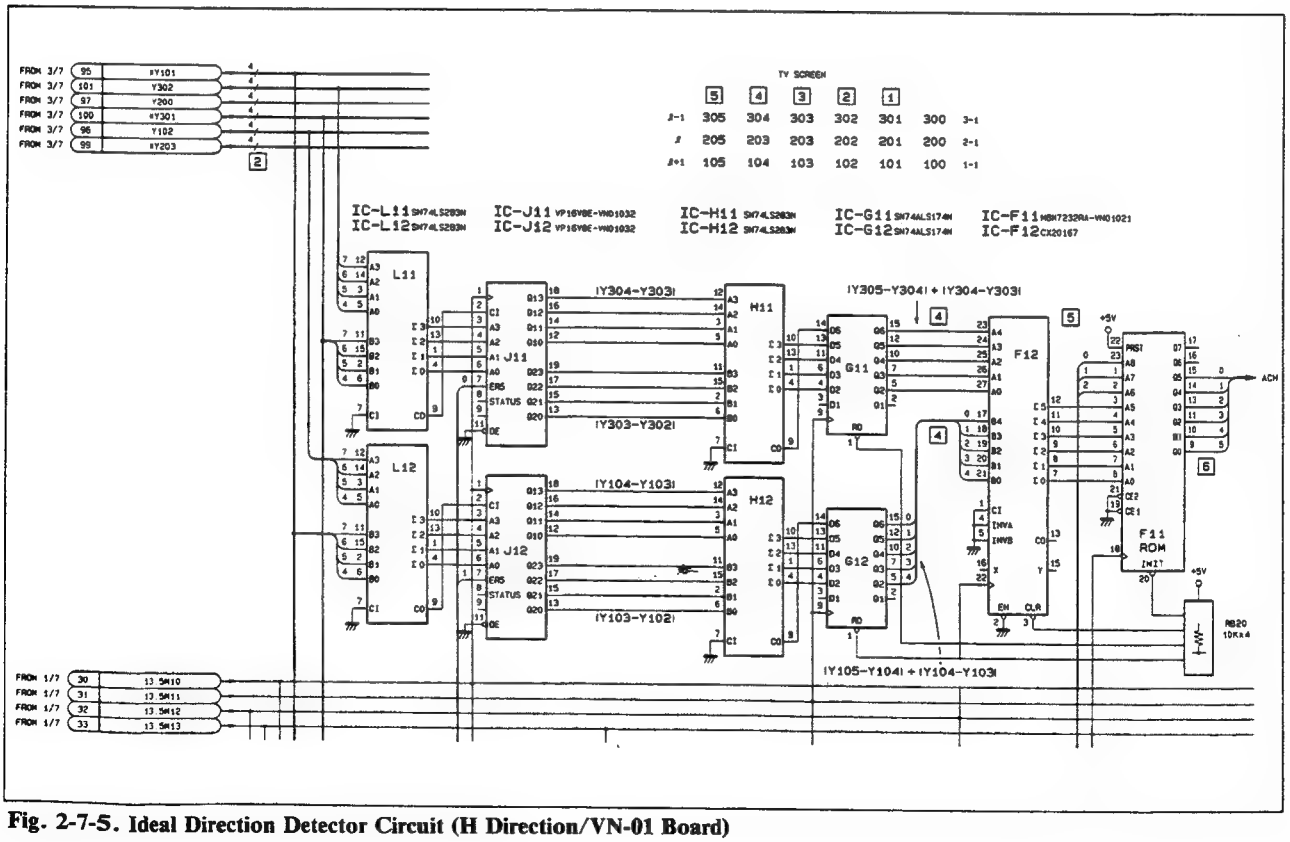



**Fig. 2-7-5. Ideal Direction Detector Circuit (H Direction/VN-01 Board)**

By "interpolation" is meant 2-point interpolation. For instance, the fact that interpolation is possible in the V direction is denoted by the status in which both "a" and "b" in Fig. 2-7-6 are error-free.

By "replacement" is meant simple replacement. For instance, the fact that replacement in the D− direction is possible is denoted by the status in which any one direction of "c" or "d" in Fig. 2-7-6 is error-free.

Interpolation takes precedence in identifying the concealment mode. The sequence of priority for the directions is the ideal direction followed by H, V, D− and D+, in that order.

ICC19 (D19) determines the ultimate concealment mode from the error flags and enable signals corresponding to the various modes.

Fig. 2-7-6 shows an algorithm which is processed in the shuttle mode at a speed of less than ±10 times normal tape speed. As indicated by the algorithm, the concealment circuit operates unless errors occur for all 8 points (8-neighborhood) around the object point. At a speed of less than ±10 times normal tape speed in the shuttle mode, there is very little likelihood that errors will occur for all 8 points. In contrast, it is virtually impossible to obtain correct data in a high-speed shuttle mode. As a result, concealment is not possible with the algorithm indicated in Fig. 2-7-6, the data of the previous frame are output in their original form and the information required for a picture with accompanying movement is lost. Information which is not detailed (with a high spatial frequency) but vague (with a low spatial frequency) is required in a high-speed shuttle mode.



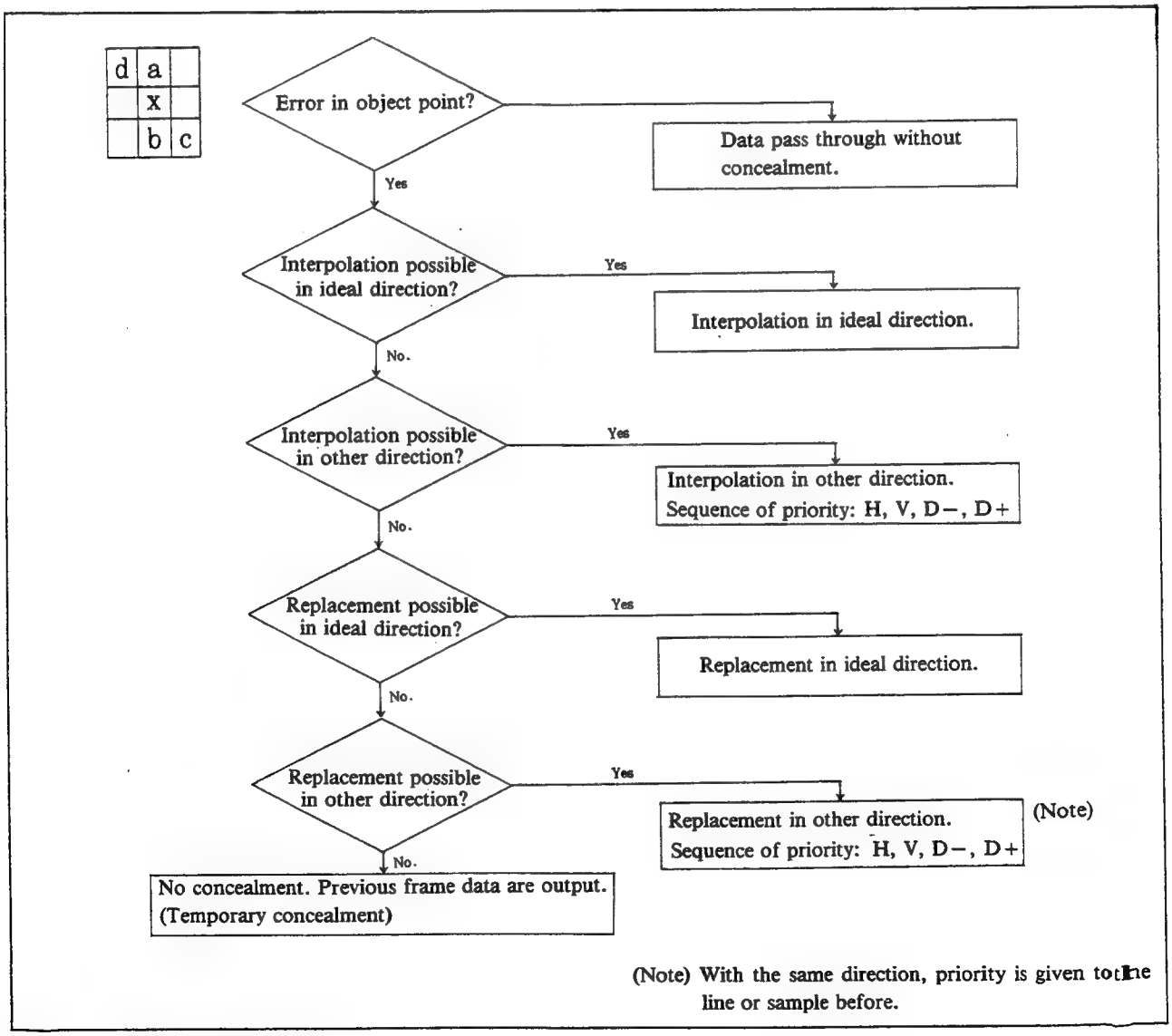



**Fig. 2-7-6. Concealment Algorithm (VN-01 Board)**

Consequently, recursive replacement is undertaken in a high-speed shuttle mode, and the data other than the data of the 8 points around the object point are used for the replacement. The points which can be used for recursive replacement are those error-free points of one or more samples and one or more lines prior to the object point.

The number of times they are used for replacement is counted, and it is possible for the same data to be used for recursive replacement up to 6 times. However, in a high-speed shuttle mode, it is virtually impossible to obtain correct data, and so even the correction data obtained by the interpolation and replacement are weighted for the count and used.

When even recursive replacement cannot be undertaken, there is no concealment processing and the data of the previous frame are output.

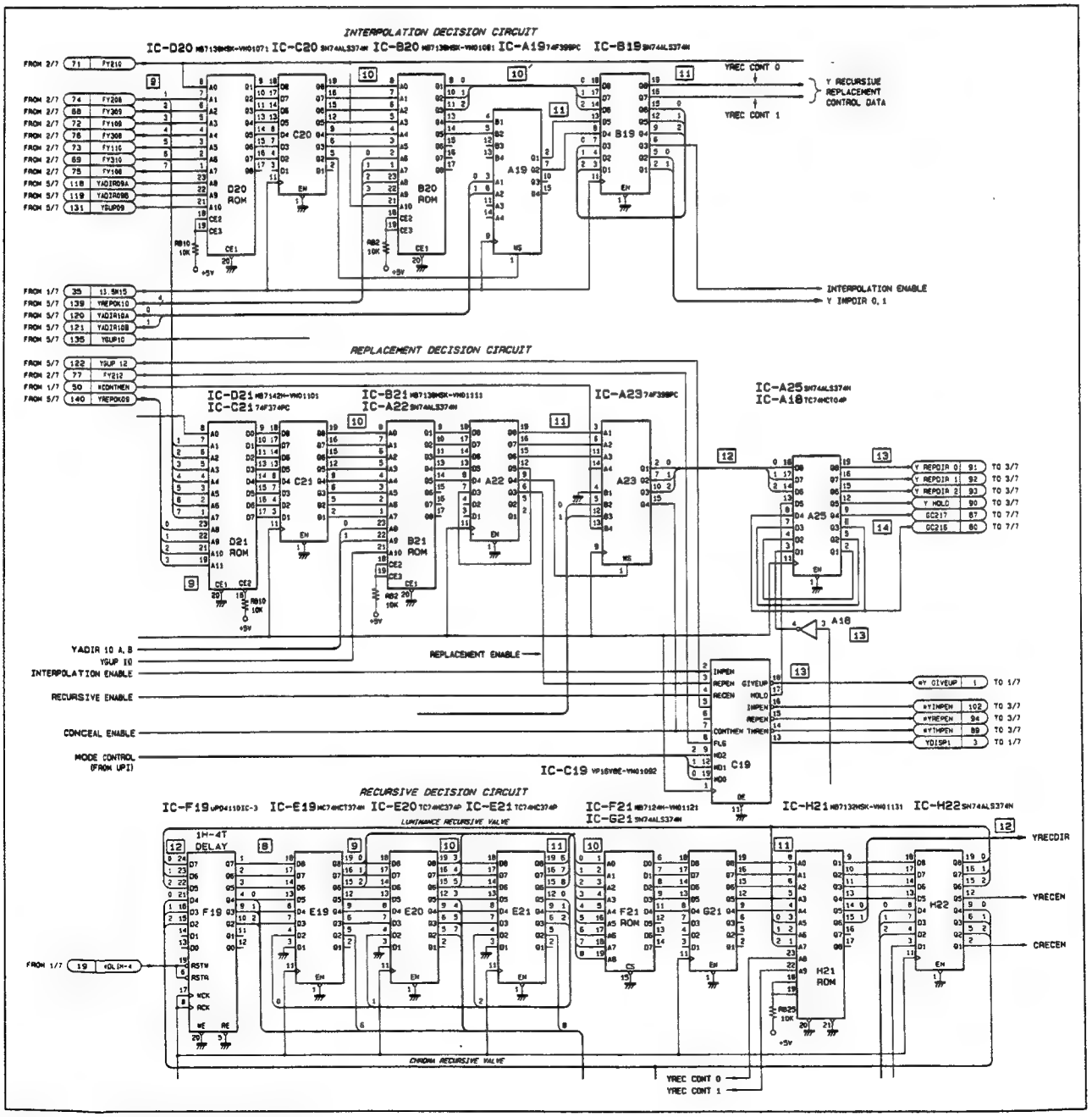



**Fig. 2-7-7. Concealment Circuits (VN-01 Board)**

### 7. H/V Blanking Addition Circuit (ICB24, B25/VN-01 board)

After the data have undergone concealment processing but before they are supplied to the interface encoder, the black level data (Y:$10_H$, $C_R/C_B$:$80_H$) are added to these data at the positions corresponding to horizontal and vertical blanking. When the input data are $00_H$ and $FF_H$, the use of these values is prohibited by the next stage interface encoder and so they are converted respectively into $01_H$ and $FE_H$.

### 8. Interface Encoder (VN-01 board)

In this circuit, the Y (13.5 MHz), $C_B$ (6.75 MHz) and $C_R$ (6.75 MHz) signals which have undergone the concealment processing as well as the control signal, frame pulse and H pulse are multiplexed and converted into signals conforming to the RP-125/TECH3246-E format.

Two RP-125/TECH3246-E format signals are output from interface encoder ICG26. One signal is ECL converted by ICG32 and G33 and sent to the VA-45 board. This signal is first D/A converted on the VA-45 board and then output externally via the ANALOG VIDEO OUTPUT connector. The other signal is first delayed by an amount equivalent to several samples (in order to provide the delay using the analog filter) in consideration of the delay applying when the analog video signal is processed on the VA-45 board, it is ECL converted by ICF29 and F31 and then output from the DIGITAL VIDEO OUTPUT connector on the connector panel. The bit rate is 27 Mbps under the RP-125 standard and it is here that the signal is delayed in 13.5 MHz sampling clock units and the delay amount is provided by switch S4/S5. In actual fact, the data with the 27 Mbps bit rate are de-multiplexed by the 13.5 MHz clock pulses and the writing into FIFO ICH28 and G29 is delayed. The data read out from FIFO are returned to the data with a 27 Mbps bit rate by multiplexer ICE28, E29 and F29, and then output.

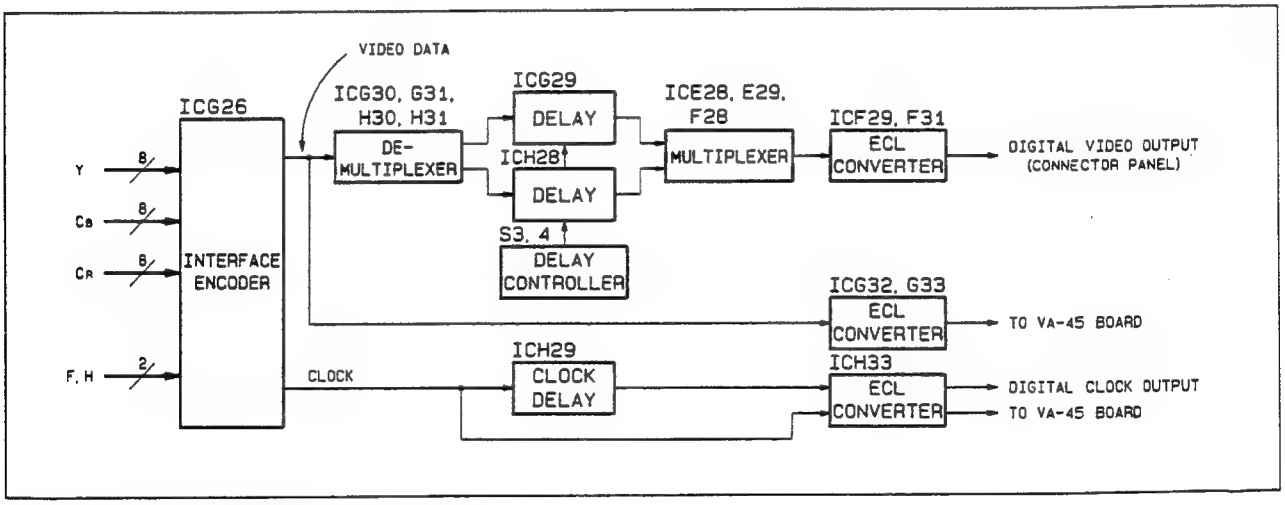



**Fig. 2-7-8. Interface Encoder (VN-01 Board)**

## 4-3. AUDIO SIGNAL SYSTEM

### 4-3-1. Outline of Audio Signal System

The audio signal system is composed of the following circuit boards. The functions of each board are as follows.

AT-45 board:
- Audio line output amplifier
- Audio monitor output amplifier

IV-14 board/IV-21 board:
- Analog/digital audio input processing

AA-29 board:
- Audio A/D, D/A conversion

PG-13 board:
- Peak level hold circuit, digital filter

AU-86 board:
- Clock exchanging, recording signal selection, recording level control

AE-06 board:
- Cross fade
- Audio data word mode setting
- Addition data/user data adding
- Outer encode

AP-14 board:
- Addition data/user data extracting
- Audio data time base conversion
- Channel status re-blocking

AN-01 board:
- Error concealment
- Output mode setting
- Output level control, peak level holding
- Advance return data processing

The audio data and video data undergo multiplexing and subsequent processing on the following boards.

IE-17 board:
- Audio shuffling memory
- Inner encode
- SYNC/ID adding
- Scrambling, serializing

SY-70 board:
- PLL, SYNC/ID extraction

CI-01 board:
- Inner decode
- Audio LIP sync memory
- Audio outer decode

The analog audio input signals are supplied to the AA-29 board through the IV-14 (IV-21) board and are A/D converted for each channel. The A/D converted audio data is encoded in the AES/EBU format by the PG-13 board and supplied to the AU-86 board.
Besides this data, the AES/EBU format digital audio data supplied to the DIGITAL AUDIO INPUT connector is input to the AU-86 board through the IV-14 board (IV-21 board), and the signal corresponding to the control panel setting is selected.
The selected audio data is exchanged for the internal clock signal and sent to the recording signal selector. In this circuit, the advance return data which is supplied from the AN-01 board of the playback system and the input data are selected in accordance with the VTR mode. After the audio data has left the select circuit, its level is adjusted by the level controller and it is output to the AE-06 board.
Cross fading for editing is undertaken on the AE-06 board. The addition data, user data and outer correction code are added to the audio data which is then output to the IE-17 board.
The audio data supplied to the IE-17 board is shuffled and multiplexed with the video data. The subsequent processing is the same as that for the video signals in that the data is formed into the program track format, converted into serial data and supplied to the DVR-1000.

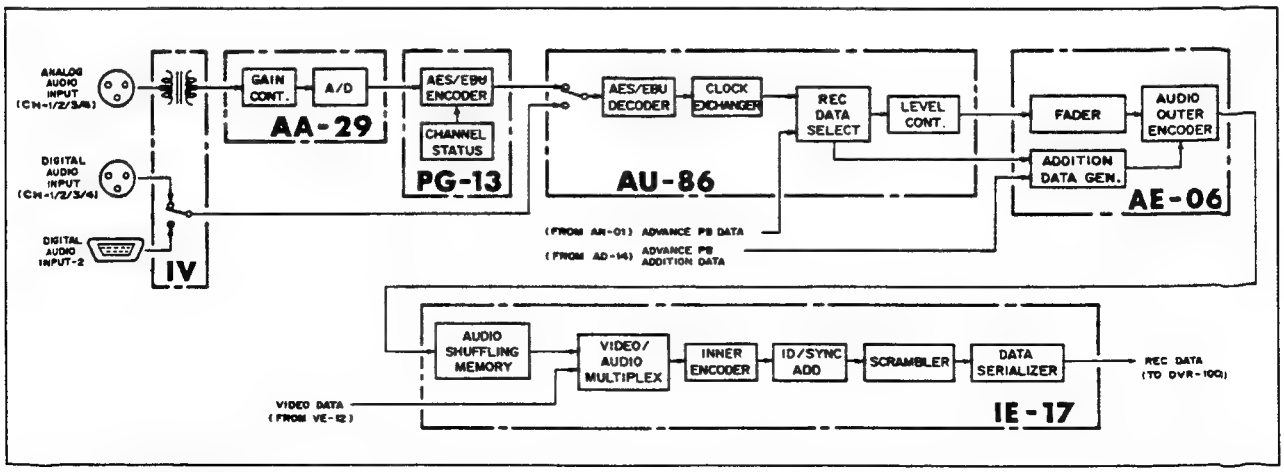



**Fig. 3-1. Audio Signal Recording System**

The playback system for the audio signals has all the circuits as far as the channel exchanger on the CI-01 board in common with the video signal system and so these circuits will not be described here.

After it has been separated from the channel exchanger output, the audio data is supplied to the LIP sync memory. The phases of the audio signals and video signals are aligned here. At the same time, audio de-shuffling is done. Errors in the de-shuffled audio data are corrected by the outer decoder and the data is sent to the AP-14 board.

On the AP-14 board, the addition data among the playback data is extracted, the audio data is controlled by this data and it is then converted to the original data sequence. Channel status re-blocking is also done on this board. After it has been output from the AP-14 board, the audio data is supplied to the AN-01 board. The error data which could not be corrected by the outer decoder is compensated here. After errors in the audio data have been compensated, its level is adjusted, the data is divided into the CONFI head playback data and ADVANCE head playback data, it is converted into the AES/EBU format and output.

The CONFI head playback data is also supplied to the AA-29 board via the 2-times oversampling filter on the PG-13 board. This signal is converted into an analog signal and output via the AT-45 board.

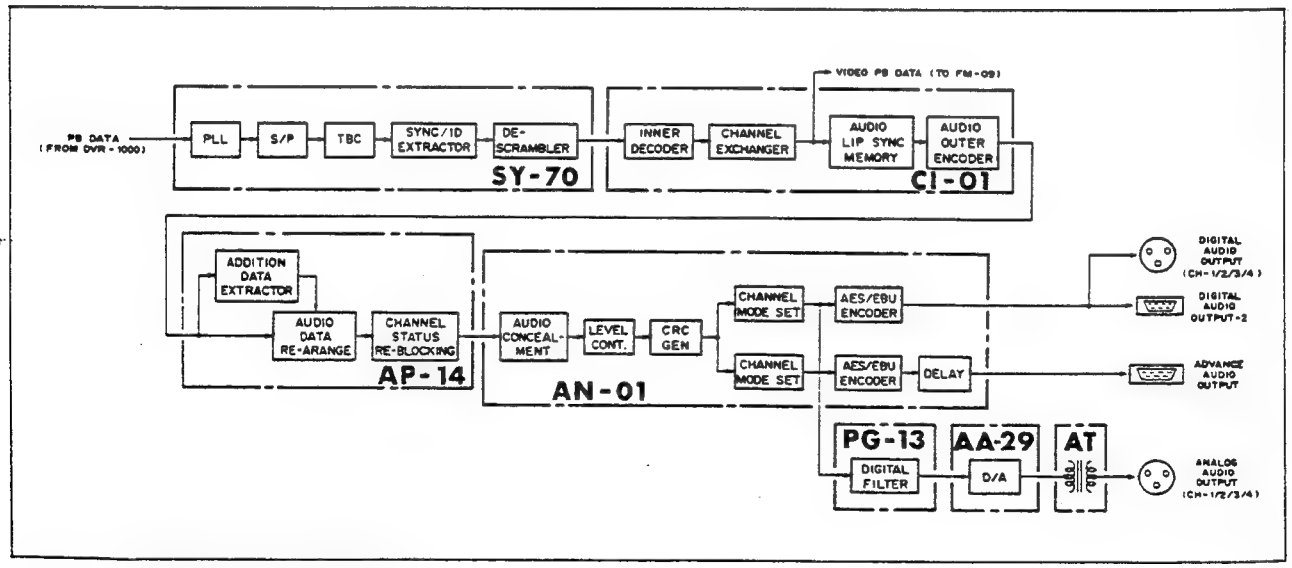



**Fig. 3-2. Audio Signal Playback System**

## 4-3-2. AT-45 Board

The AT-45 board is composed of the audio line output amplifier, monitor system output amplifier and analog muting circuit. A balanced type of output based on a transformer is featured in each case.

### 1. Audio Line Output Amplifier (AT-45 board)

Since analog audio output channels 1, 2, 3 and 4 all have the same circuitry configuration, the description below is restricted to CH-1.

After it has been output from the D/A converter block on the AA-29 board, the audio line output signal has its output level and output impedance set in this circuit, and it is then output via the ANALOG AUDIO OUPUT connector on the connector panel.

The reference input level of the signal supplied to this circuit is −6.0 dBs (between pins 1 and 2 of CN301), regardless of the level when it is output. The signal itself is supplied to the differential amplifier which is composed of IC102 and R111-R114. RV101 on the output side of this amplifier is for adjusting the output level of the signal. The output level is set by adjusting this variable resistor in combination with gain control jumpers JP101 and 102. When the output reference level is between +8 dBm and −6 dBm, JP102 is shorted; when it is between −6 dBm and −20 dBm, JP101 is shorted.

After its level has been adjusted, the audio line output signal has its phase compensated by C107 and R101, and it is then supplied to the output drive circuit. Q102, 103, 105 and Q106 configure a current mirror circuit, and while Q101 and Q104 are operating, they provide a constant current and suppress the generation of distortion caused by changes in $V_{BE}$.

IC101, C101, C104 and R106, 107 and 108 configure a DC servo circuit which prevents the generation of direct current at the primary transformer.

The impedance of the output transformer is 40 ohms at the primary and 37.5 ohms (per circuit) at the secondary. The output impedance can be switched to 600/150 ohms or 37.5 ohms by combining the series-parallel connection of the secondary winding.

The muting circuit mentioned below is provided at the final output end.

Fig. 3-2-1. is a level diagram of the audio line output circuit.



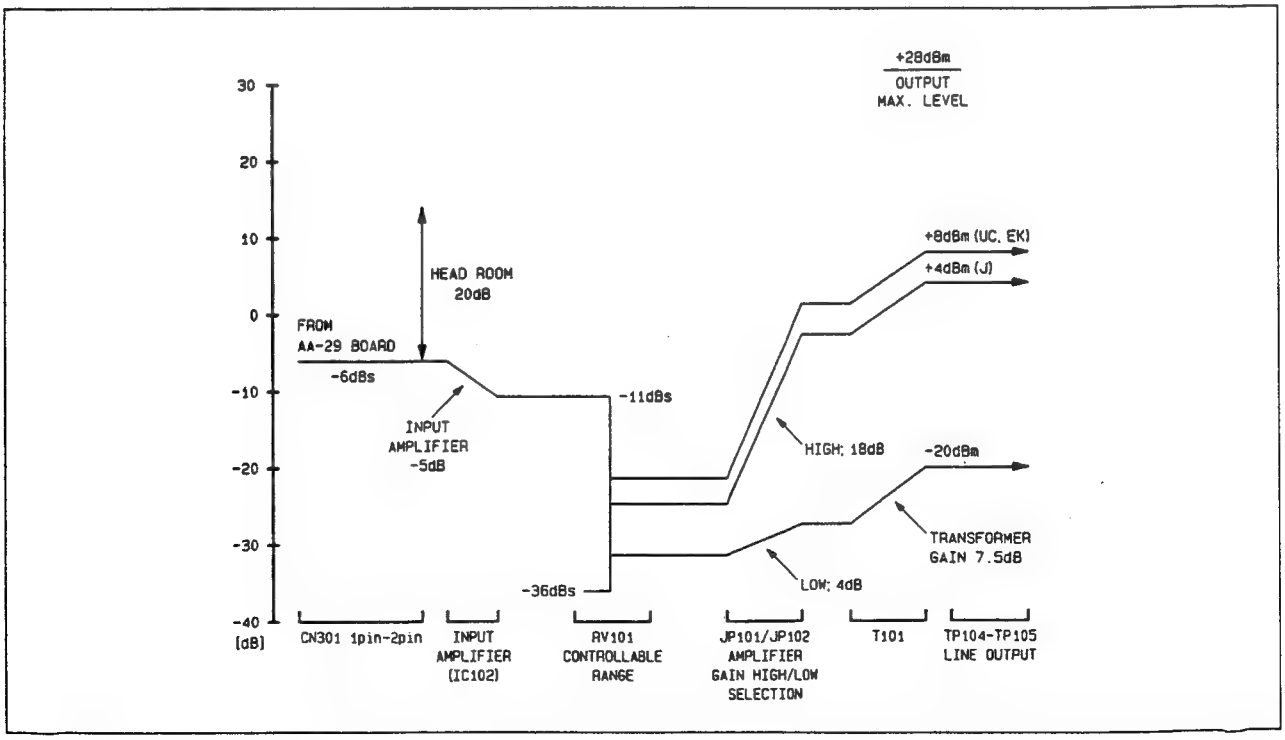



**Fig. 3-2-1. Audio Line Output Circuit Level Diagram (AT-45 Board)**

### 2. Monitor Output Amplifier (AT-45 board)

Supplied to this circuit are the audio monitor output signals L-CH and R-CH which have been selected by the AA-29 board and also the digital mix signal "D-MIX" which is supplied from the PG-13 board. The level of these signals is adjusted by this circuit, and then the signals are output to the DVR-1000 through the TO VTR (CN-A) connector on the connector panel. The monitor output L-CH, R-CH and D-MIX channels have the same circuit configuration, and this is why only the monitor output L-CH will be described below.

The L-CH monitor output signal, which was supplied to the AT-45 board, enters the differential amplifier composed of IC501 and R502-R505. The reference input level here is fixed at −10 dBs (between pins 1 and 2 of CN305). The level of the signal which is output by this amplifier is adjusted by RV501, and the signal is then sent to primary output transformer drive amplifier IC501, R508, R509 and C505. C505 keeps the DC component gain down to "1" and prevents a high-level DC current from flowing to the transformer.

The output impedance of the output transformer is 600 ohms. A muting circuit is provided at the output end.

Fig. 3-2-2 is a level diagram of this circuit.

### 3. Analog Muting Circuit (Q1, 2, 3, 4/AT-45 board)

When the power is switched on, unusual sounds may be heard because the operation inside the machine has not stabilized. This is why an analog muting circuit using a relay is provided on this board. The muting time is approximately 8 to 18 seconds after the power has been switched on. The relay is set off as soon as the power is switched off.

This circuit serves to mute the noise in accordance with the status of the power ON/OFF information "RMT" (pin 4 of CN050; high level when power is ON) which is supplied from the power supply section. When the power is switched on, Q1 and Q2 are both driven into conduction, the base potential of Q3 rises with the time constant determined by R10 and C17, Q3 is driven into conduction, Q4 is set off, and the muting function is released.

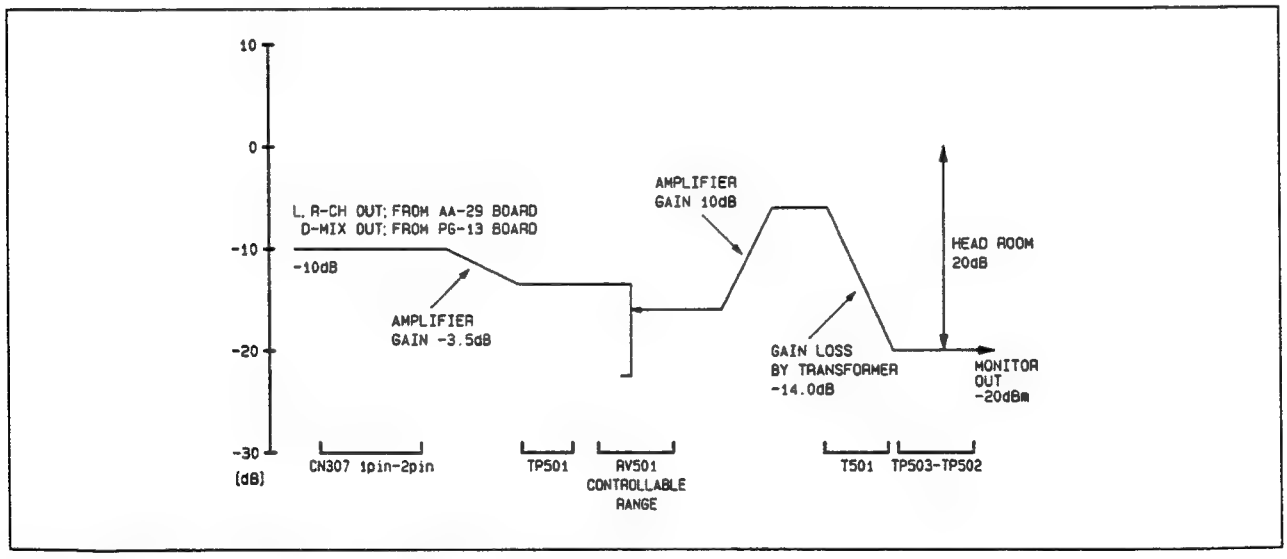



**Fig. 3-2-2. Monitor Output Circuit Level Diagram (AT-45 Board)**

## 4-3-3. IV-14 Board

The IV-14 board is composed of the following circuits.

- Analog video signal input/output circuits
- Reference sync selector
- Analog audio input circuit
- Digital audio signal input/output circuits

Only the audio signal system is described in this section. For details on the video signal system, refer to section 4-2-2.
In the DVPC-1000 with the serial numbers given below, the IV-14 board has been changed, the video signal system circuitry has been separated on the IV-20 board and the audio signal system circuitry has been separated on the IV-21 board. Sections 4-2-3 and 4-3-4 give details for those boards affected by these changes.

DVPC-1000(J): #11201 and Higher
DVPC-1000(UC): #11001 and Higher
DVPC-1000(EK): #11101 and Higher

### 1. Analog Audio Input Circuit (IV-14 board)

The analog audio signal, which is supplied to the ANALOG AUDIO INPUT connector on the connector panel, is input to this circuit. Since analog audio input channels 1, 2, 3 and 4 have the same circuit configuration, only CH-1 will be described below.
After it has been supplied to this circuit, the analog audio signal passes through the attenuator circuit composed of R384, R385 and R386 on its way to input transformer T4. Input transformer primary jumpers JP21-JP24 serve to select the input level and they are set in accordance with the reference input level. When the reference audio input level is between +8 dBm and −6 dBm, JP22 and JP23 are shorted and JP21 and JP24 are kept open. In this state, the audio input signal is attenuated by about 16.5 dB by the attenuator circuit and then it is sent to the transformer. When the reference audio input level is between −6 dBm and −20 dBm, JP21 and JP24 are shorted, and JP22 and JP23 are kept open. In this state, the input signal is sent straight to the transformer as it is without passing through the attenuator circuit. After it has been output from the input transformer, the audio signal is output via balanced output amplifier IC89 to the AA-29 board. This is a balanced output signal with a level of 0 dBs. Variable resistor RV38 enables the input level to be adjusted across a range extending from +5.7 dB to +27.9 dB.
The line input impedance can be set to 150 ohms, 600 ohms or 10 kohms, depending on the combination of the settings of the slide switch at the side of the ANALOG AUDIO INPUT connector and of jumpers JP19 and 20 on the IV-14 board.
Fig. 3-3-2 is a level diagram of the audio line input section.

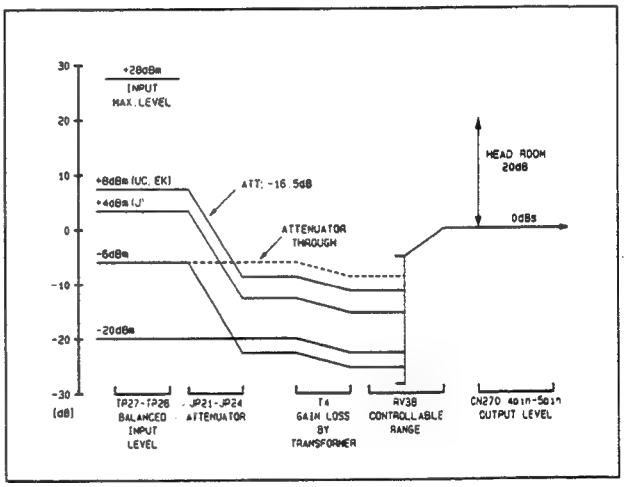



**Fig. 3-3-1. Analog Audio Input Circuit (IV-14 Board)**

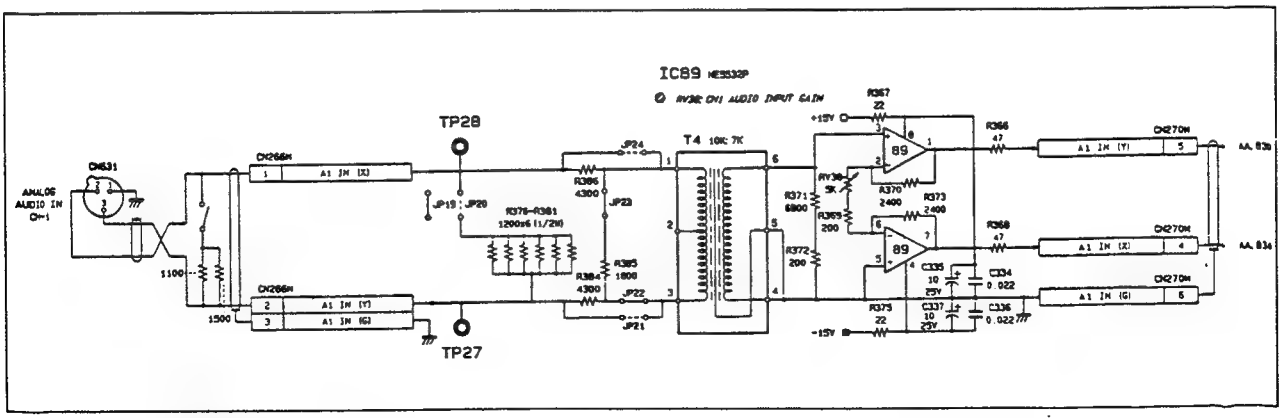



**Fig. 3-3-2. Level Diagram of Audio Line Input Section (IV-14 Board)**

**2. Digital Audio Input/Output Circuits (IV-14 boards)**

**(1) Digital audio input circuit**

Two digital audio signals based on the AES/EBU format are supplied to this circuit from the DIGITAL AUDIO INPUT-1 connector (XLR, 3 pins) and DIGITAL AUDIO INPUT-2 connector (DSUB, 15 pins) on the connector panel.

The digital audio input signal is selected using AUDIO INPUT XLR/DSUB selector switch S2 on the AU-86 board when the machine is in the local mode and using the control panel of the DVR-1000 when it is in the remote mode. However, the actual selection of the signals is undertaken by this circuit.

Depending on the contents of the "AXD/SEL" signal which is supplied from the AU-86 board, this circuit selects one of the two digital audio signals using selector circuit IC1 and 2, and it outputs the selected signal to the AU-86 board.

Diodes for input protection are connected to the respective input circuit sections, and the signals are terminated with a 51-ohm resistance.

**(2) Digital audio output circuit**

The main digital audio signals "DA OUT #1 – #4" and the advance audio signals "EADV #1 – #4" are supplied to this circuit from the AN-01 board.

The main digital audio signal is output via inverter IC6 and line driver IC3 and 5 to the DIGITAL AUDIO OUTPUT-1 connector (XLR, 3 pins) and DIGITAL AUDIO OUTPUT-2 connector (DSUB, 15 pins) on the connector panel.

The advance audio signal passes through inverter IC6 and line driver IC4, and it is output from the ADVANCE AUDIO OUTPUT connector (DSUB, 15 pins) on the connector panel.

Diodes for output protection are connected to the respective output circuits.

## 4-3-4. IV-21 Board

The IV-21 board is composed of the analog audio input circuit and digital audio input/output circuits.

The IV-21 board is used in the DVPC-1000 with the serial numbers given below. For earlier DVPC-1000 machines, the IV-14 board is used. For a detailed description of the audio signal system on the IV-14 board, refer to section 4-3-3.

DVPC-1000(J): #11201 and Higher
DVPC-1000(UC): #11001 and Higher
DVPC-1000(EK): #11101 and Higher

**1. Analog Audio Input Circuit (IV-21 board)**

The analog audio signal, which is supplied to the ANALOG AUDIO INPUT connector on the connector panel, is input to this circuit. Since analog audio input channels 1, 2, 3 and 4 have the same circuit configuration, only CH-1 will be described below.

After it has been supplied to this circuit, the analog audio signal passes through the attenuator circuit composed of R807, R808 and R809 on its way to input transformer T801. Input transformer primary jumpers CN803-CN806 serve to select the input level and they are set in accordance with the reference input level. When the reference audio input level is between +8 dBm and −6 dBm, CN804 and CN805 are shorted and CN803 and CN806 are kept open. In this state, the audio input signal is attenuated by about 16.5 dB by the attenuator circuit and then it is sent to the transformer. Alternatively, when the reference audio input level is between −6 dBm and −20 dBm, CN803 and CN806 are shorted and CN804 and CN805 are kept open. In this state, the input signal is sent straight to the transformer as it is without passing through the attenuator circuit.

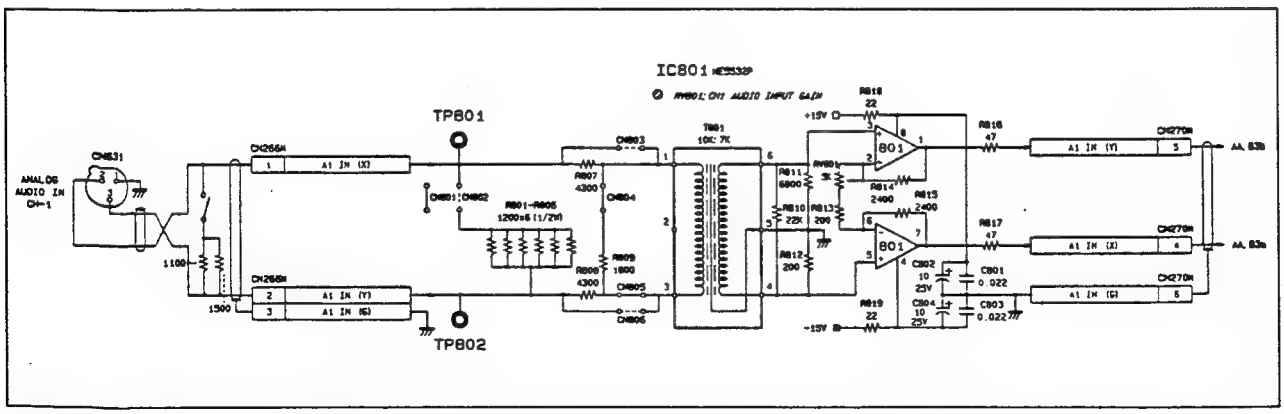



**Fig. 3-4-1. Analog Audio Input Circuit (IV-21 Board)**

After it has been output from the input transformer, the audio signal is output via balanced output amplifier IC801 to the AA-29 board. This is a balanced output signal with a level of 0 dBs. Variable resistor RV801 enables the input level to be adjusted across a range extending from +5.7 dB to +27.9 dB. The line input impedance can be set to 150 ohms, 600 ohms or 10 kohms, depending on the combination of the settings of the slide switch at the side of the ANALOG AUDIO INPUT connector and of jumpers CN801 and CN802 on the IV-21 board. Fig. 3-4-2 is a level diagram of the audio line input section.

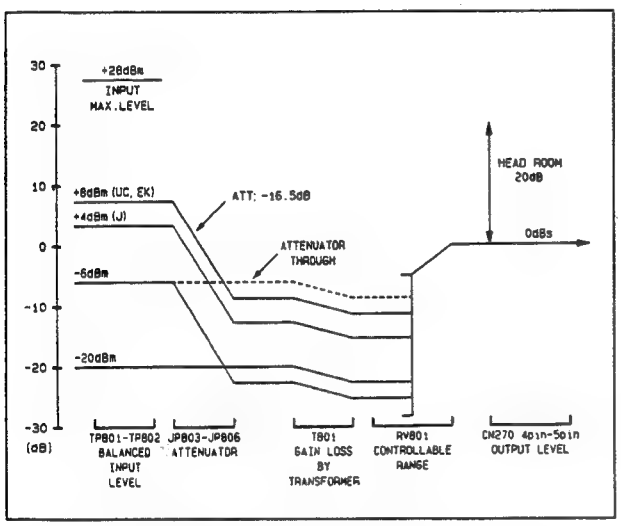



**Fig. 3-4-2. Level Diagram of Audio Line Input Section (IV-21 Board)**

**2. Digital Audio Input/Output Circuits (IV-21 board)**

**(1) Digital audio input circuit**

Two digital audio signals based on the AES/EBU format are supplied to this circuit from the DIGITAL AUDIO INPUT-1 connector (XLR, 3 pins) and DIGITAL AUDIO INPUT-2 connector (DSUB, 15 pins) on the connector panel. The digital audio input signal is selected using AUDIO INPUT XLR/DSUB selector switch S2 on the AU-86 board when the machine is in the local mode and using the control panel of the DVR-1000 when it is in the remote mode. However, the actual selection of the signals is undertaken by this circuit.

Depending on the contents of the "AXD/SEL" signal which is supplied from the AU-86 board, this circuit selects one of the two digital audio signals using selector circuit IC901 and 904, and it outputs the selected signal to the AU-86 board.

Diodes for input protection are connected to the respective input circuit sections.

**(2) Digital audio output circuit**

The main digital audio signals "DA OUT #1—#4" and the advance audio signals "EADV #1—#4" are supplied to this circuit from the AN-01 board.

The main digital audio signal is output via inverter IC906 and line driver IC905 and 907 to the DIGITAL AUDIO OUTPUT-1 connector (XLR, 3 pins) and DIGITAL AUDIO OUTPUT-2 connector (DSUB, 15 pins) on the connector panel.

The advance audio signal passes through inverter IC906 and line driver IC909, and it is output from the ADVANCE AUDIO OUTPUT connector (DSUB, 15 pins) on the connector panel.

Diodes for output protection are connected to the respective output circuits.

## 4-3-5. AA-29 Board

The AA-29 board is composed of the following circuits.

- Analog line audio A/D converter
- Analog line audio D/A converter
- Audio monitor output signal selector

The signals supplied to the ANALOG AUDIO INPUT CH-1, 2, 3 and 4 connectors on the connector panel are input to the A/D converter on the AA-29 board through the IV-14 or IV-20 board. The digital signals obtained by the A/D conversion are output to the PG-13 board.

The digital audio data from the PG-13 board are supplied to the D/A converter on the AA-29 board. The analog signals produced after D/A conversion are output through the AT-45 board to the ANALOG AUDIO OUTPUT CH-1, 2, 3 and 4 connectors on the connector panel.

In the monitor output selector, signals for the monitor left (L-CH) and right (R-CH) channels are selected for each channel from among the audio line input or output signals. The selected signals are supplied via the AT-45 board to the DVR-1000.

The timing signals used during A/D conversion and D/A conversion as well as the control signals for monitor signal selection are all supplied from the PG-13 board.

The audio signal CH-1, CH-2, CH-3 and CH-4 circuit configuration is identical for each channel and so the description below is confined to CH-1.

### 1. A/D Converter Block (AA-29 board)

The A/D converter block is composed of the following circuits.

(1) Input amplifier
(2) Gain control circuit
(3) Pre-emphasis circuit
(4) Low-pass filter
(5) DC offset compensation circuit
(6) Sample and hold circuit
(7) A/D converter
(8) Constant current circuit
(9) Digital auto zero compensation circuit
(10) Conversion clock generator

The analog signal processing blocks extends from the input amplifier section to the output stage of the low-pass filter section. The subsequent circuits are peripheral circuits required to operate the integrating type of A/D converter. This converter is a 16-bit linear quantizing type, and the sampling frequency is 48.0 kHz for both 525/60 systems and 625/50 systems.

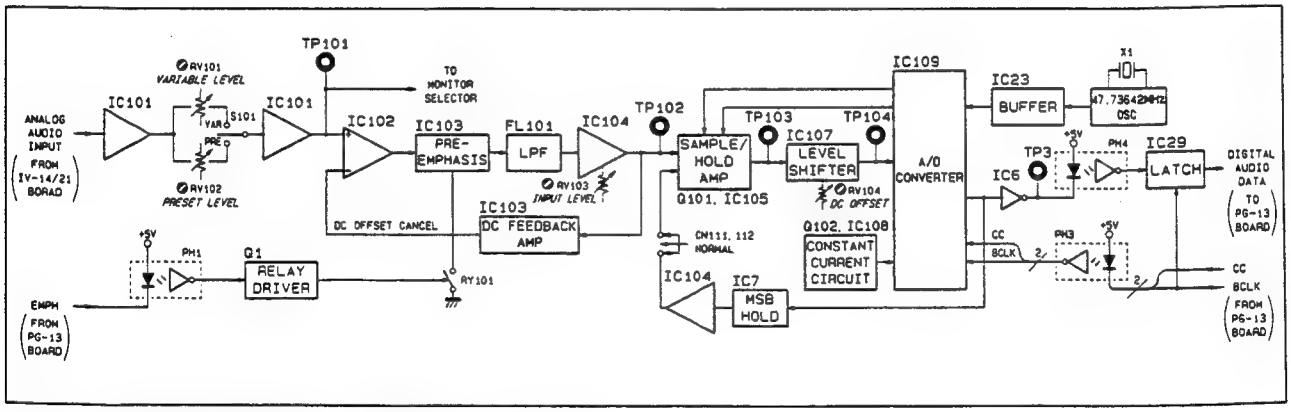



**Fig. 3-5-1. Block Diagram of A/D Converter (AA-29 Board)**

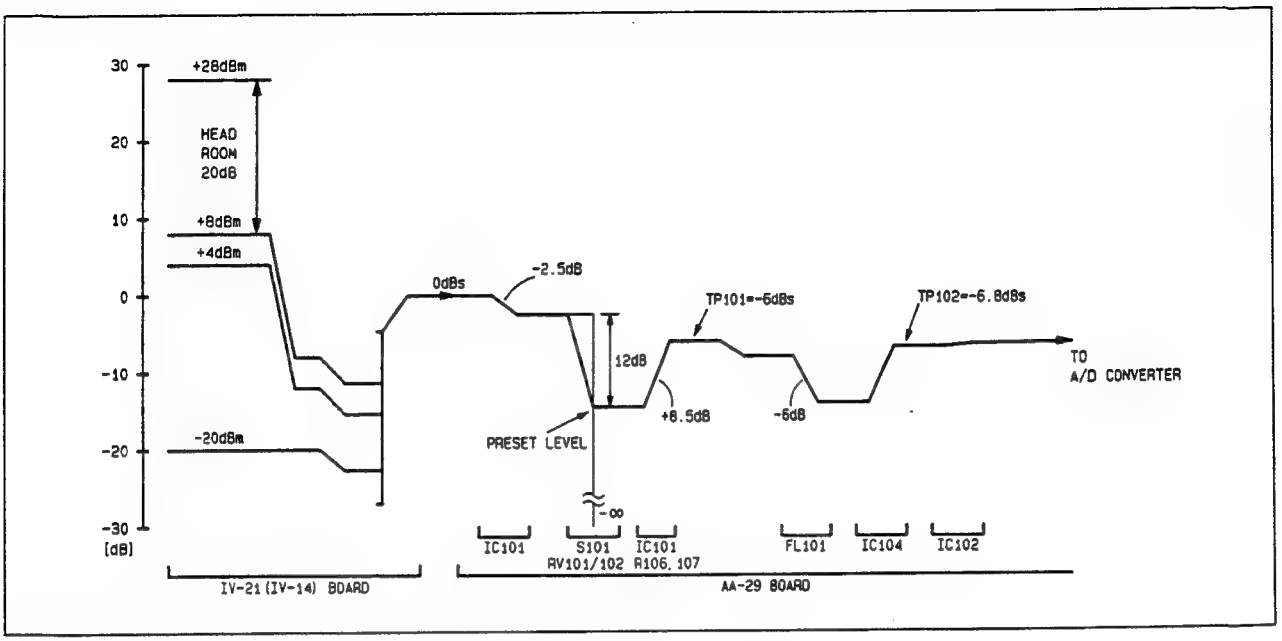



**Fig. 3-5-2. Line Audio Input Section Level Chart (AA-29 Board)**

**(1) Input amplifier (AA-29 board)**

After they have been supplied to this board in a balanced type from the IV-14 or IV-20 board, the CH-1 analog audio signals are converted into an unbalanced type by the differential input amplifier which is composed of IC101 and R111-R114. The reference level for the signals supplied to this circuit is 0 dBs. The amplifier gain is −2.5 dB.

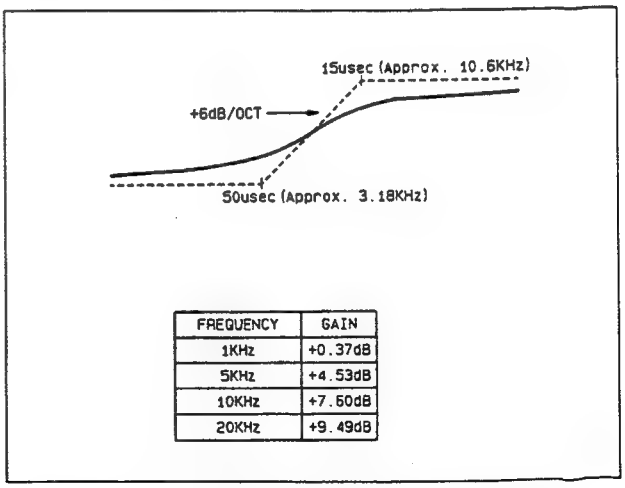
**(2) Gain controller (AA-29 board)**

The line input signals which are output from input amplifier IC101 are supplied to this circuit where their level is adjusted. When switch S101 on the front of the board for setting the input level is at the "VAR" position, it is possible to use level control RV101 to vary the input signal level across a range from +12 dB to −∞ with respect to the preset level. RV102 functions as the control for setting the preset level.

After its level has been set, the input signal passes through the buffer amplifier composed of IC101, R106 and R107 and it is output to the next stage pre-emphasis circuit. The gain of the buffer amplifier is +8.5 dB, and the reference level at TP101 is −6 dBs.

**(3) Pre-emphasis circuit (AA-29 board)**

This is a time constant circuit which reduces the amount of high-frequency noise, and it adds the characteristics shown in Fig. 3-5-3 to the audio signals while they are being recorded. The time constant circuit itself is provided at the non-inverting input side of non-inverting amplifier IC103, and the ON/OFF mode of this circuit is selected by relay RY101 in accordance with the "EMPH 1" signal supplied from the PG-13 board. During playback, the reverse characteristics are added to the signals converted into analog signals and their frequency response is made flat.




| FREQUENCY | GAIN |
|---|---|
| 1KHz | +0.37dB |
| 5KHz | +4.53dB |
| 10KHz | +7.60dB |
| 20KHz | +9.49dB |

**Fig. 3-5-3. Pre-emphasis Characteristics (AA-29 Board)**

**(4) Low-pass filter (AA-29 board)**

Prior to A/D conversion it is necessary to limit the frequency range of the original signals to less than one-half of the sampling frequency (fs). The sampling frequency of this unit is 48 kHz, and this means that the original signals must be attenuated at 24 kHz.

FL101 is an 11-stage active filter. Based on the 1 kHz frequency level, its attenuation characteristics are −0.3 dB ±0.3 dB at 20 kHz, under −80 dB at 25 kHz and under −90 dB between 60 kHz and 100 kHz. Since the FL101 output is in the high-impedance state, the output is received by buffer amplifier IC104 and its level is adjusted at the same time by RV103 provided with the amplifier so as to match the level with that of the next stage A/D converter.

The TP102 level is approximately −6.8 dBs at the reference level.

**(5) DC offset compensation circuit (AA-29 board)**

In order to maintain the zero level of the analog signals before they are supplied to the A/D converter, the DC components of the signals are eliminated by the DC servo circuit shown in Fig. 3-5-4.

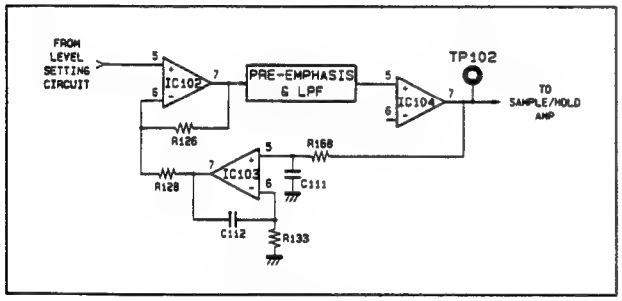



**Fig. 3-5-4. DC Offset Compensation Circuit (AA-29 Board)**

The DC components of the output of IC104 pin 7 are fed back to the non-inverting input pin of IC102 via integrating amplifier IC103, thereby canceling out the DC offset. When it comes to the AC components, this circuit functions as a non-inverting amplifier which is composed of IC102, R126 and R128. The gain of this amplifier is +0.8 dB.

**(6) Sample and hold circuit and level shifter (AA-29 board)**

During A/D conversion, it is necessary for the analog voltage applying at the sampling time to be held. In order to achieve this, the sample and hold circuit store a charge which is proportionate to the input voltage in holding capacitor C126. Since an integrating type of A/D converter is used on this board, this charge is released at a constant rate after sampling. Fig. 3-5-5 is a block diagram of these circuits.

Sample and hold pulse "SH2" is supplied from A/D converter IC109 to FET switch Q101. When the "SH2" pulse level is high, the sampling mode is established; when it is low, the hold mode is established.

In the sampling mode, Q101 is driven into conduction, and C126 is charged by the time constant determined by the ON resistance of Q101 and by R167 and C126. IC105 is a buffer for maintaining the charging current. When the input voltage is set to VIN, the resistance of R135 is equivalent to that of R146 and so the TP103 voltage is −VIN.

In the hold mode, Q101 is set OFF and the C126 charge is released at a constant rate.

As described in the next section, the A/D converter determines the selection of the two types of current source and the timing of the conversion completion by means of a comparison between the integrating voltage and reference voltage ($V_H$, $V_L$). This means that the integrating voltage in this vicinity expands by about 16 dB with the inverting amplifier which is composed of IC107, R155 and R156. D102 is a limiter for the unnecessary positive output voltage. Finally, the DC bias is varied by RV104 and the expanded part is selected.

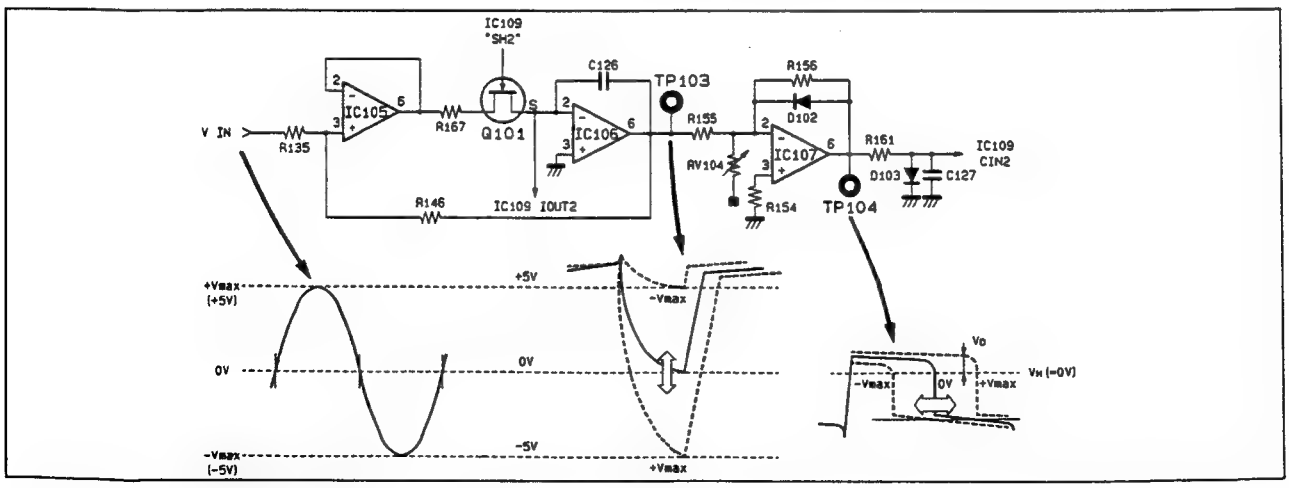



**Fig. 3-5-5. Sample & Hold Circuit and Level Shifter (AA-29 Board)**

**(7) A/D converter (AA-29 board)**

The 16-bit serial output type of CX20018, manufactured by SONY, is used for A/D converter IC109. This is a cascaded integrating type of A/D converter. When the charge corresponding to the analog level is to be released by the constant current source, the converter divides this discharge time into two halves, releasing the charge quickly during the first half of the time and then slowing down the discharge during the second half, and it assigns and outputs the count results of the respective periods to the high-order and low-order bits.

Fig. 3-5-6 is a block diagram of the A/D converter and its peripheral circuits while Fig. 3-5-7 is a timing chart.

There are two modes, the sample mode and the hold mode, which apply for the actual conversion. When conversion command "CC" is high, the sample mode is selected; when it is low, the hold mode is selected.

In the sample mode, Q101 is driven into conduction, SW-A and SW-B are set off and a charge corresponding to the input signal level is stored in C126 (see previous section). When "CC" is set low and the hold mode is established, Q101 is set off, SW-A is set on and SW-B is set off, and the high-order (MSB) counter starts counting. Simultaneously, holding capacitor C126 starts discharging at a constant current ($I_H$) and the TP103 voltage rises. IC107 is responsible for the inverted amplification and level shifting of the integrated output and also for the limiting of the forward direction output by means of D102.

When the TP104 voltage reaches the reference voltage $V_H$ of the high-order counter, the high-order (MSB) comparator is activated, SW-A goes off and SW-B is set on, and at the same time as the high-order counter stops, the low-order (LSB) counter starts counting and the discharge is continued at a constant current ($I_L$). The ratio ($I_H/I_L$) between $I_H$ and $I_L$ is set to 128 which means that the gradient of the integrated output voltage is 1/128.

When the TP104 voltage reaches the reference voltage $V_L$ of the low-order counter, the low-order (LSB) comparator is activated, all the counts are stopped and the series of conversion operations is completed. It is possible to obtain the A/D conversion data by connecting in series the 9-bit high-order counter and 7-bit low-order counter. After the A/D conversion, the parallel data are converted into serial data, synchronized with the "BCLK" bit clock pulse and then output.

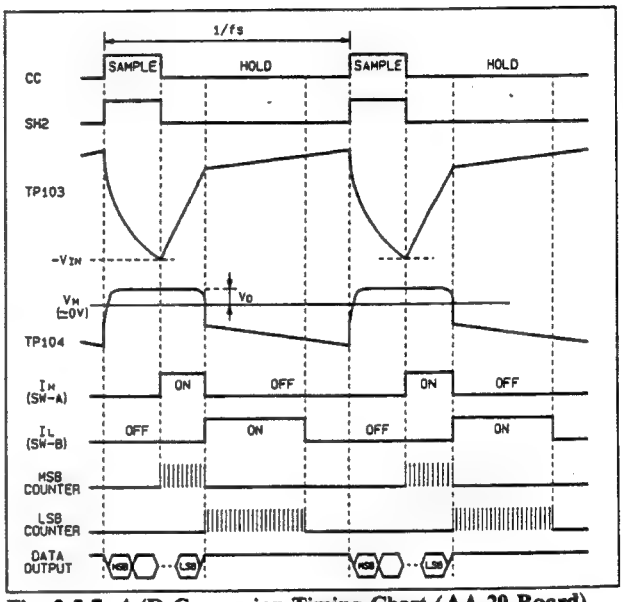



**Fig. 3-5-7. A/D Conversion Timing Chart (AA-29 Board)**

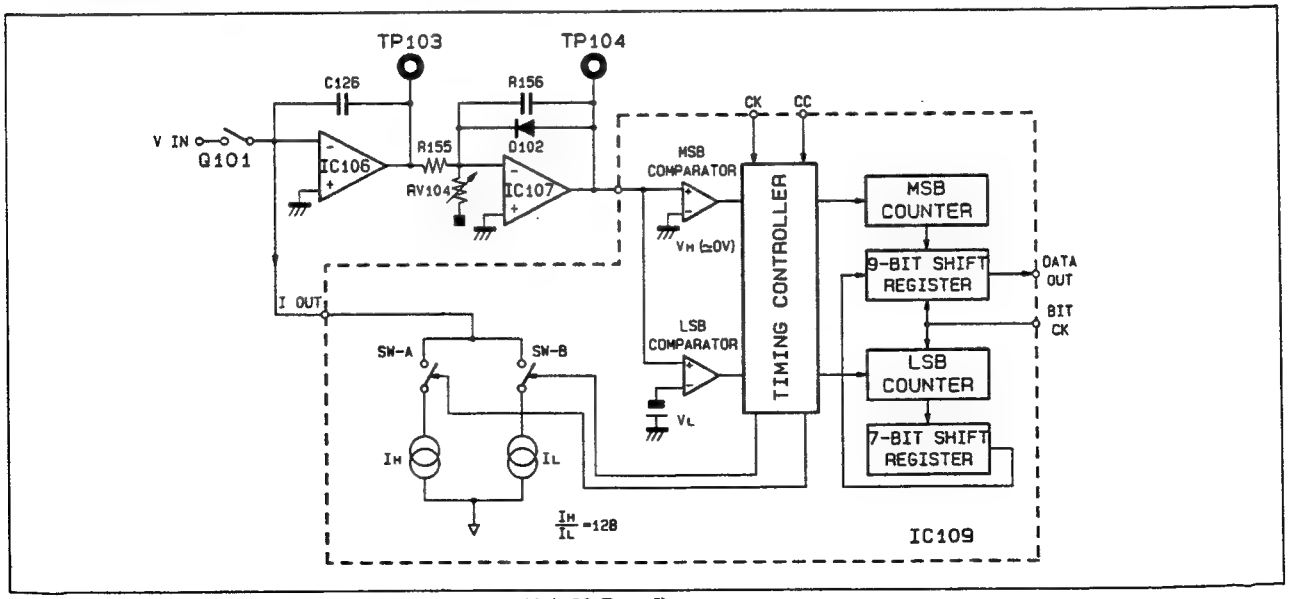



**Fig. 3-5-6. A/D Converter and Peripheral Circuits (AA-29 Board)**

**(8) Constant current circuit (AA-29 board)**

The A/D converter functions to create internally the $I_H$ and $I_L$ current sources with a current ratio of 1:128. The "$I_{SET}$" current, which serves as the reference for these current sources, is supplied from the external constant current circuit.

IC108 is a zener diode which is provided with a heater and, based on the constant voltage which is output from this diode, the "$I_{SET}$" reference current is supplied to the A/D converter through the current mirror which is composed of Q102, R160 and R162.

**(9) Auto zero compensation circuit (AA-29 board)**

The operational zero point of the A/D converter must be adjusted so that the output data is zero under a no-signal condition. Zero point adjustment is done by varying the DC bias with RV104. Furthermore, in order to deal with the offset which is generated by the amplifier system and with the fluctuations in the DC level caused by temperature characteristics during operation and in order to enhance the precision, the MSB of the output data is fed back to the analog system to safeguard against the generation of offset in the output data. The auto zero compensation circuit is composed of latch IC7 which detects the MSB of the output data of the A/D converter and amplifier IC104 which integrates this MSB and feeds it back to the sample and hold circuit. These components shift the analog level in the negative direction when the output data deviate toward the positive direction and, conversely, these shift it in the positive direction when the data deviate toward the negative direction, and they function to make the output zero under no-signal conditions.

Under no-signal input conditions, the output of the A/D converter is repeatedly set high and low at short intervals because of the effects of noise and the feedback loop. The time constant (approximately 7 sec) of the feedback loop is sufficiently longer than the input signals and the amount of feedback is low so that the signal components are not affected, leaving zero compensation valid for only the DC offset of a minimal amount. This is why the zero point that functions as the operating point must be adjusted accurately. In actual fact, it can be adjusted accurately by disconnecting jumper plug CN111, opening the feedback loop, adjusting the output to zero using RV104 and then re-connecting CN111 to restore the loop.

**(10) Master clock circuit (AA-29 board)**

A clock pulse with a frequency of 47.73642 MHz is supplied to the counter inside the A/D converter. The oscillator circuit is composed of IC23 and X1, and the oscillation output is supplied in ECL differential format to the various channels.

**(11) Output data (AA-29 board)**

The output sign format is the twos complement binary code. After being output from pin 27 of A/D converter IC109, the serial data are supplied to IC29 through photocoupler PH4 and after they have been latched by the "BCLK" clock pulse, they are output to the PG-13 board. Photocouplers PH1 to PH5 are used as the digital interface between the exterior part of the board and the A/D conversion system which encompasses the audio data, "EMPH 1/2/3/4," "CC" and "BCLK," and these contribute to safeguarding against noise interference.

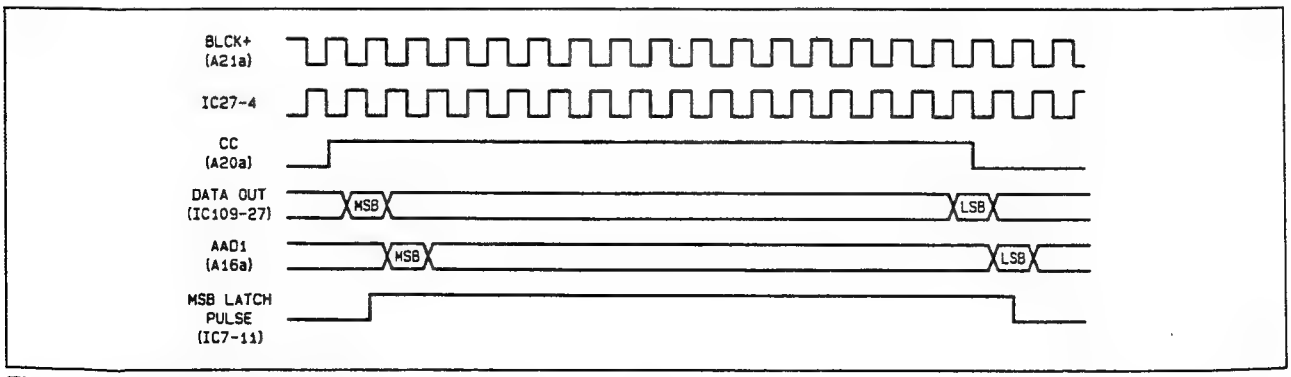



**Fig. 3-5-8. Data Output Timing (AA-29 Board)**

## 2. D/A Converter Block (AA-29 board)

The D/A converter block is composed of the following circuits.

(1) Serial-parallel converter
(2) D/A converter
(3) Sample and hold circuit
(4) Low-pass filter
(5) De-emphasis circuit
(6) Frequency response compensation circuit
(7) Output level control circuit
(8) Output amplifier

The data rate of the digital audio signals at the playback side is 48K samples/sec. Since these data are input to this board through the two-times oversampling filter on the PG-13 board, the data rate applying during D/A conversion is 96K samples/sec.

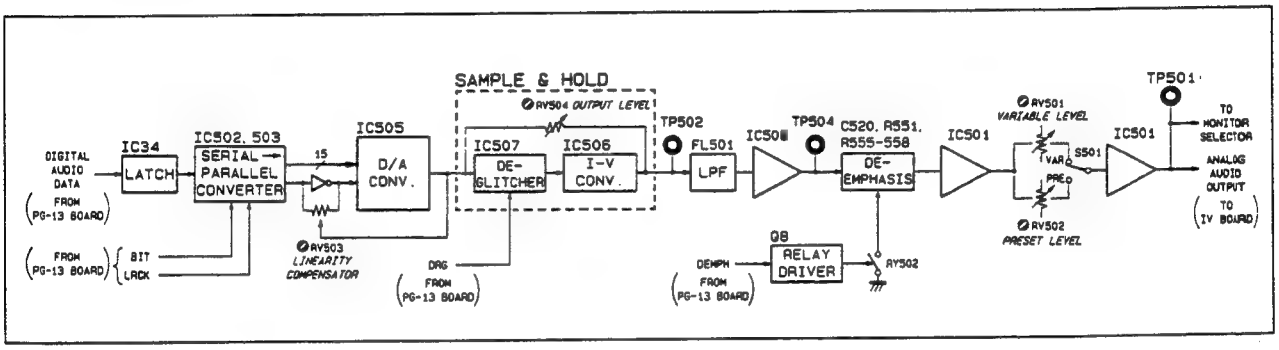



**Fig. 3-5-9. D/A Converter and Peripheral Circuits (AA-29 Board)**

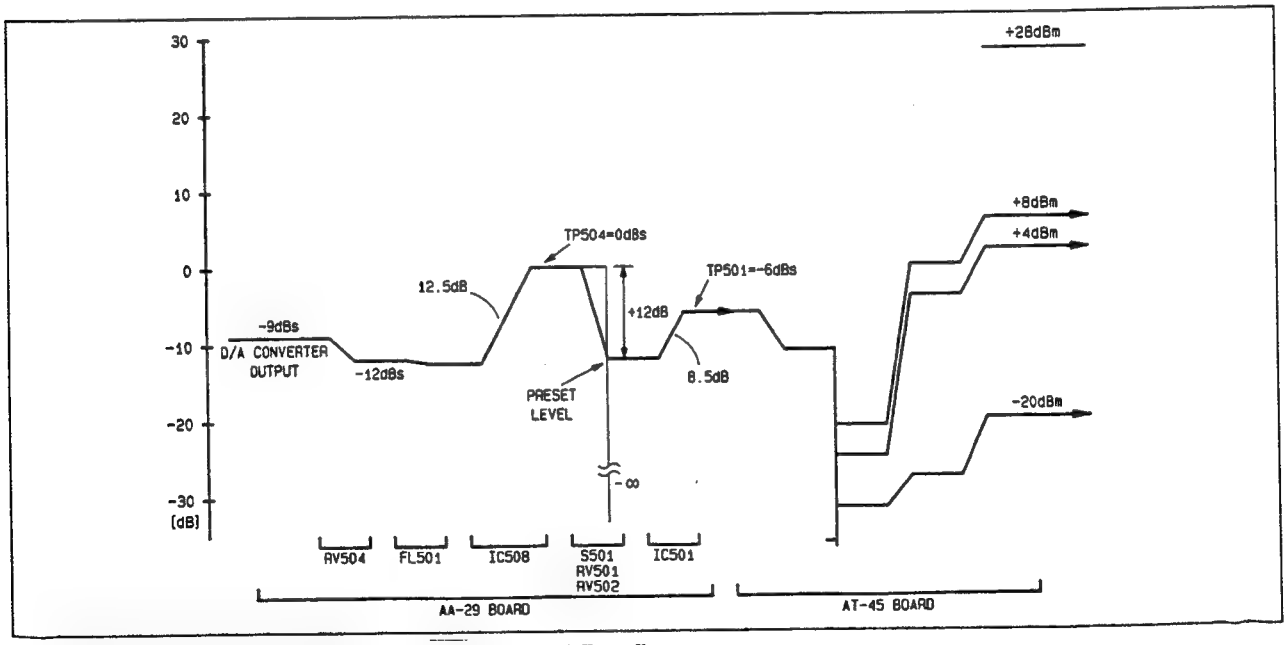



**Fig. 3-5-10. D/A Converter Section Level Chart (AA-29 Board)**

**(1) Input data and serial-parallel converter (AA-29 board)**

After they are output from the PG-13 board, the digital audio data for CH-1 enter this board, they are latched by IC34, converted into 16-bit parallel data by IC502/503, and are then supplied to D/A converter IC505. As shown in Fig. 3-5-12, the input serial data are supplied in synchronization with the data clock pulse "BIT", and the data latching during parallel conversion is undertaken at the rise of the "LRCK" pulse.

**(2) D/A converter (AA-29 board)**

A 16-bit parallel input type of D/A converter is used for D/A converter IC505. On an AA-29 board with the board number 1-620-925-11, the PCM53-I current output type (made by Burr-Brown) is used and on an AA-29 board with the board number 1-620-925-12, the PCM53-V voltage output type (made by Burr-Brown) is used. Fig. 3-5-11 shows the internal configuration of the D/A converter. (The internal circuitry has been created with reference to the handbook issued by the IC manufacturer.)

The segment method is employed for the actual D/A conversion, and a current source parallel system is combined with the resistance ladder network to divide the full scale into 8 segments for the 3 most significant bits while the resistance ladder is incorporated for the 13 least significant bits, and a current equivalent to the 13 bits is generated. By means of the segment decoder, the 3 most significant bits control the ON/OFF status of the current source for the number (0 through 7) corresponding to the 3-bit data. The current which has been set ON is added to form the high-order current $I_U$. A current of 0.25 mA is supplied from the various current sources and the high-order current $I_U$ changes across a range from 0 mA to 1.75 mA in accordance with the data.

The same current source as that for the 3 most significant bits is used for the 9 middle bits (bits 4 through 12), and a current flows corresponding to the weight of each bit by means of the resistance ladder. As regards the 4 least significant bits, the emitter resistance of the current source is first increased in accordance with the bits and the current is limited, after which it passes through the resistance ladder.

The low-order current $I_L$ equivalent to the 13 bits which passes through the resistance ladder changes by 30 nA for each step, it varies in a maximum of "$2^{13}$-1 steps", and it is added to the high-order current $I_U$. This means that the range of the output current with respect to the 16-bit data input is from 0 mA to 1.99997 mA. In actual fact, $I_{OFFSET}$, which is equivalent to 1 mA, is subtracted from this range, with the result that the current output $I_{OUT}$ ranges from −1 to 0.99997 mA.

The above description refers to the operation of the current output type of D/A converter. When the voltage output type of D/A converter is used, the current output $I_{OUT}$ mentioned above is I/V converted to produce a ±10 V output voltage $V_{OUT}$.

RV503 is the control which serves to compensate for zero crossover distortion. Based on the MSB of the input data of the D/A converter, this control compensates the distortion by varying the amount of current which flows to the output pin of the D/A converter.

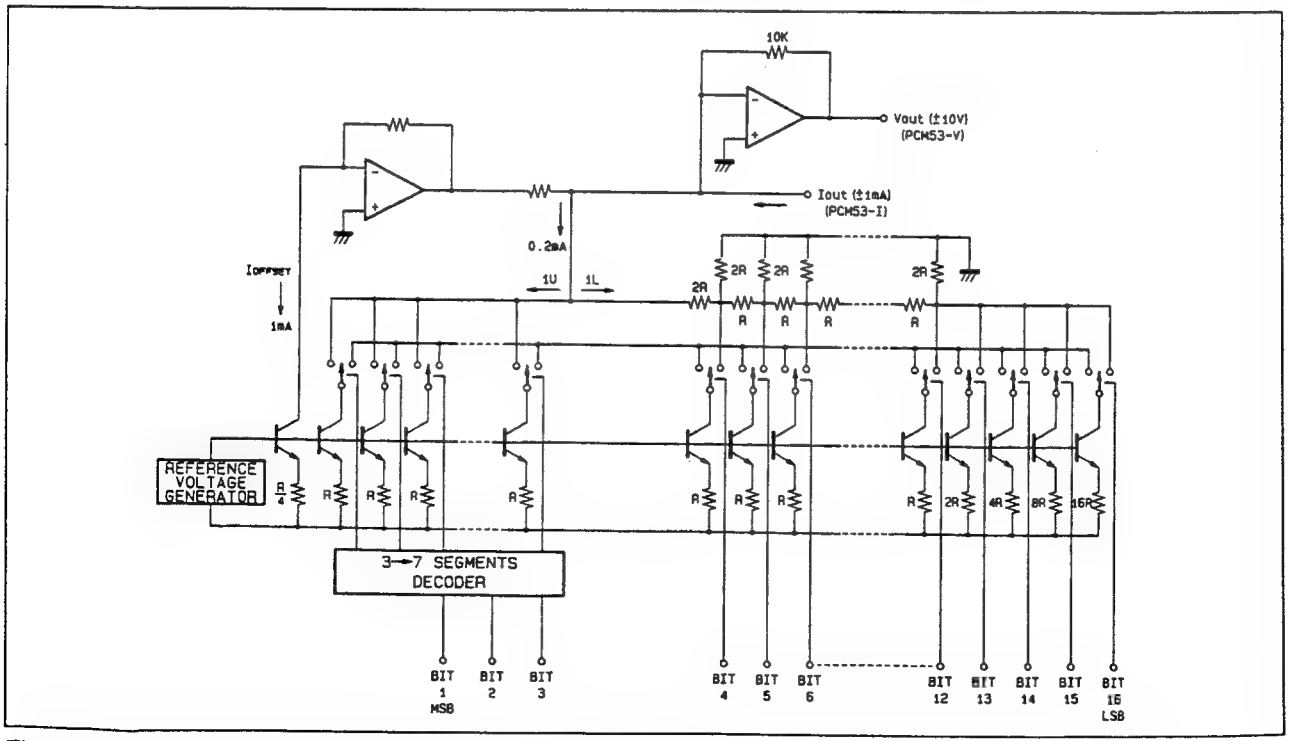



**Fig. 3-5-11. Basic Configuration of D/A Converter (PCM53/AA-29 Board)**

**(3) Sample and hold circuit (AA-29 board)**

This circuit is composed of IC507, IC506 and peripheral circuits, and it provides deglitching during D/A conversion and I/V conversion.

When the sample and hold pulse "DGR" supplied from the PG-13 board is high, the sample mode is established; when it is low, the hold mode is established.

In the sample mode, analog switcher IC507 is set on, the D/A converter output and the integrating amplifier IC506 input are connected, and integrating capacitor C524 is charged in accordance with the output voltage. In the hold mode, analog switcher IC507 is set off and the output voltage of the D/A converter is held. In this way, sampling is conducted after the output current of the D/A converter has stabilized and by holding the value at the change point of the output, the occurrence of glitches is avoided.

The output voltage of TP502 is determined by the output current of the D/A converter, R544 and control RV504 which adjusts the output level. The output level of TP502 is approximately −12 dB at the reference level.

**(4) Low-pass filter (AA-29 board)**

Low-pass filter FL501 is a 9-stage active filter with a flat response up to 20 kHz. It has attenuation characteristics of approximately −20 dB at 40 kHz, approximately −60 dB at 60 kHz and more than −77 dB at frequencies of 68.2 kHz and above. Since the two-times oversampling digital filter is positioned before the low-pass filter on the PG-13 board, the lower limit frequency of the 2fs loopback components is 76 kHz (48 kHz × 2 −20 kHz). IC508 in the next stage functions to buffer the output of the low-pass filter and to amplify it by approximately 12.5 dB.

**(5) De-emphasis circuit (AA-29 board)**

As a counter to the pre-emphasis provided at the A/D conversion side, de-emphasis is provided at the D/A conversion side with characteristics which are the reverse of those for the pre-emphasis indicated in Fig. 3-5-3, and the frequency response is made flat. This response is determined by R551, R555-R558 and C520. The de-emphasis ON/OFF control signal "DEMPH11" is supplied from the PG-13 board to drive relay RY502 through Q8. When the "DEMPH11" signal level is low, the de-emphasis function is activated.

The output level is always attenuated by 6 dB by means of the resistance divider which is composed of R555-R558.

**(6) Frequency response compensation circuit (AA-29 board)**

The amplitude characteristics in the high-frequency range in the vicinity of 20 kHz drop by approximately 1 to 1.5 dB because of the aperture affect. This is compensated for by IC508, R559, R561 and C521.

**(7) Output level control circuit (AA-29 board)**

After it is output from pin 7 of IC508, the audio signal is supplied to the differential amplifier which is composed of IC501 and R510-R513. The output of this amplifier is supplied to the output level control circuit and, depending on the setting of output level selector switch S501 on the front of the board, the output level is set.

When S501 is set to the "VAR" position, it is possible to adjust the level using RV501. In fact, the output level can be varied vis-a-vis the preset level across a range extending from +12 dB to −∞. RV502 is the control for setting the preset level.

**(8) Output amplifier (AA-29 board)**

Once its output level has been set, the signal is supplied to the buffer amplifier which is composed of IC501, R503 and R504, where it is amplified by approximately 8.5 dB and then output.

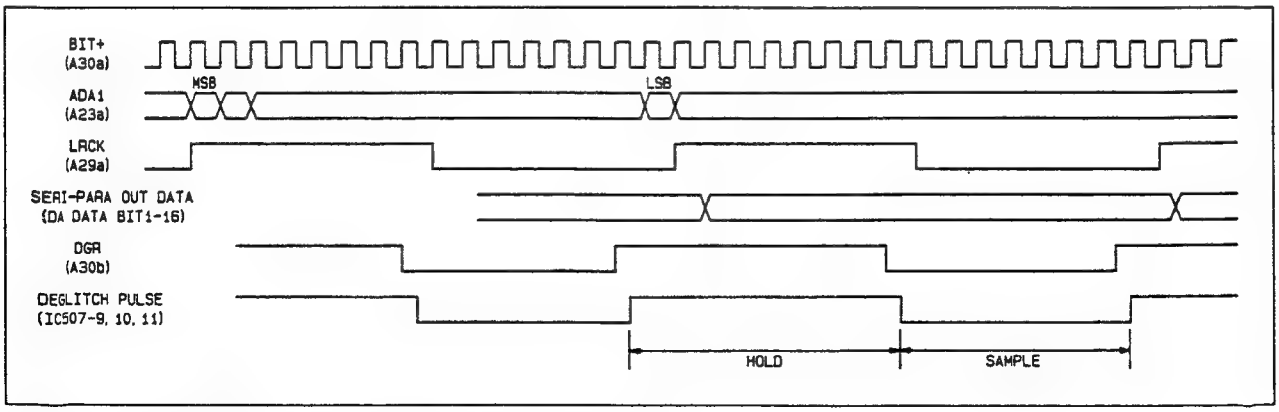



**Fig. 3-5-12 Input Data and Control Signal Timing (AA-29 Board)**

### 3. Audio Monitor Output Signal Selector Circuit (AA-29 board)

The line analog audio input signal from the A/D conversion section and the line audio output signal from the D/A conversion section are supplied to this circuit which selects the signal that is output for audio monitoring.
There is a monitor output for both the left and right channels and the output signal can be selected individually for each channel.
The selected signals are analog signals whose input/output levels have been respectively adjusted in the A/D conversion and D/A conversion sections.
The difference in level between the signals of the each channels is adjusted by RV1 through RV8, and the signals are then supplied to the next stage selector circuits IC3 and IC4. The 3-bit control signal "ALCNT 0-2" (or "ARCNT 0-2") from the PG-13 board is supplied to the selector circuit and, depending on its contents, one of the signals is selected. The selected signal is amplified by 6 dB by the buffer amplifier which is composed of IC5, R11 and R12 (IC5, R17 and R18). It is then supplied to the DVR-1000 through the AT-45 board.
The TP1 level is −10 dBs at the reference level.

## 4-3-6. PG-13 Board

The PG-13 board is composed of the following circuits.

- A/D conversion control circuit
- AES/EBU encoder
- Peak level hold circuit
- Digital mixer circuit
- Two-times oversampling digital filter

### 1. A/D Conversion Control Circuit (PG-13 board)

This circuit is designed to create the "BLCK" (64×48 kHz frequency) pulse and the "CC" pulse (48 kHz frequency, approx. 25% duty cycle) from the FAS256 (256×48 kHz frequency) and FAS (48 kHz frequency) clock pulses which are supplied from the TG-28 board. These pulses are used for controlling the A/D conversion, and they are supplied to the AA-29 board. Fig. 3-6-2 is the timing chart for these control pulses and the input data of the PG-13 board.



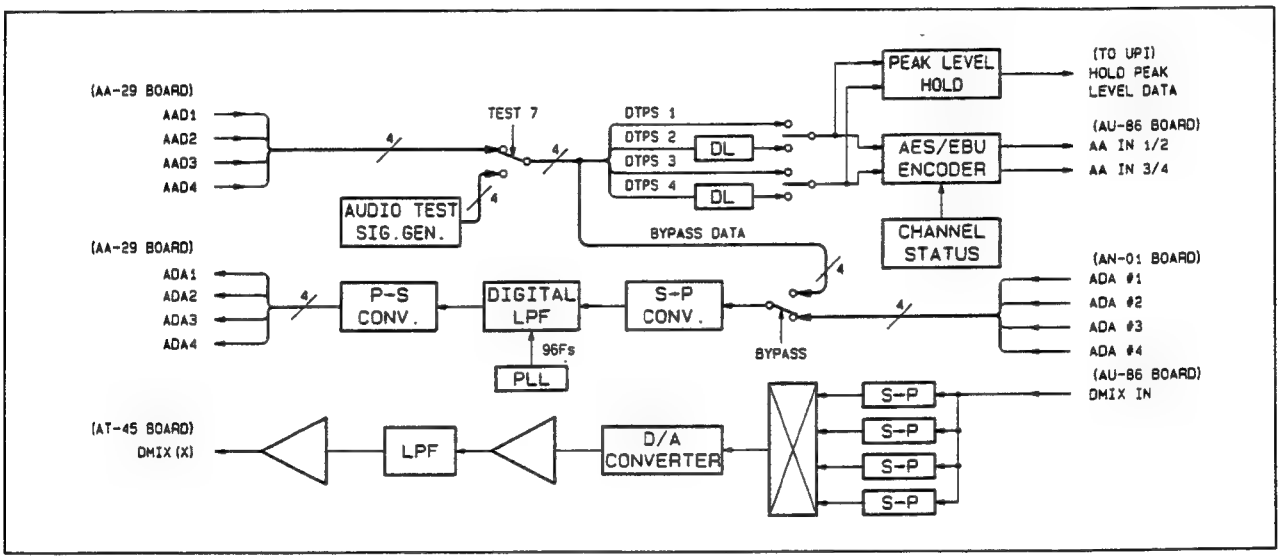



**Fig. 3-6-1. Function Diagram of PG-13 Board**

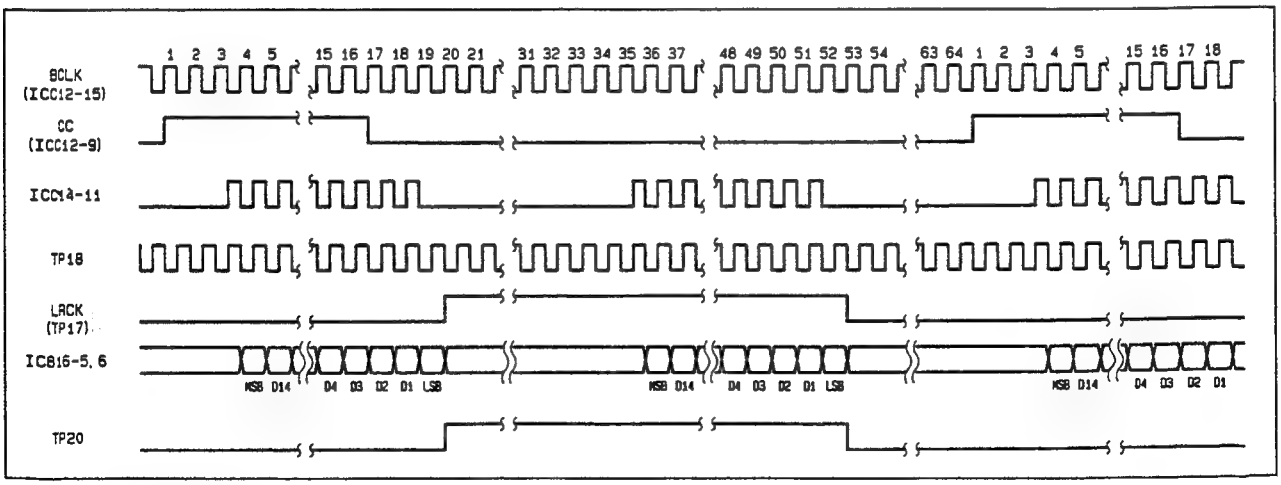



**Fig. 3-6-2. Timing Chart of A/D Conversion Control Pulses (PG-13 Board)**

## 2. AES/EBU Encoder (PG-13 board)

The digital serial data (AAD1-AAD4) provided by quantization on the AA-29 board, are supplied to the PG-13 board in sequence from MSB to LSB (MSB first sequence) at the 64fs clock rate.

In order to turn the audio data which are input at the identical timing into the AES/EBU format data, the CH-2 and CH-4 data are delayed at delay circuit ICC14 by 32 clocks, the CH-1/2 and CH-3/4 data are then time division multiplexed at the next stage multiplexer ICC13, and the resulting data are supplied to AES/EBU encoder ICB13 and B14.

The C bit (channel status bit) data and U bit (user bit) data are also inserted by the AES/EBU encoder, and these data are written at the timing described below.

The mode is established when pin "A1" (pin 17) of ICB14/B13 is set high by the pin 10 output of ICB11. The data are written at the timing of the rise of ICB13/14 pin "CS" (pin 19). A pulse indicating the start of the C bit is input to pin "BLKSYNC" (pin 6) of ICB14/14, and the C bit data and U bit data are written in sequence at the timing of the pin "CS" (pin 19) rise. The C bit data and U bit data are differentiated by the status of pin "A0" (pin 18): when this pin level is low, the C bit data are written and when it is high, the U bit data are written. The chip select signal which is input to pin "CS" (pin 19) writes the C bit data and U bit data equivalent to 4 samples into ICB13 and B14, and this is done once every 4 samples.

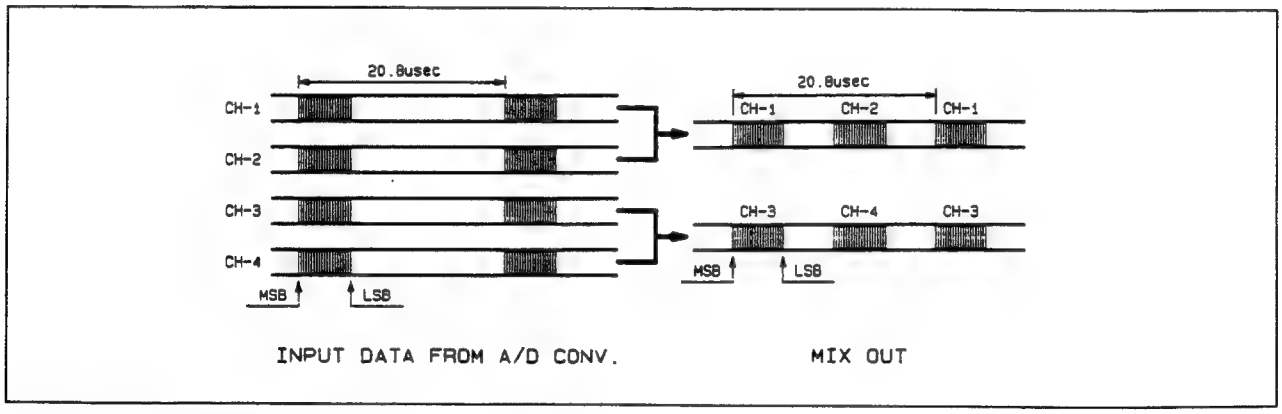



**Fig. 3-6-3. Delay Circuit (PG-13 Board)**

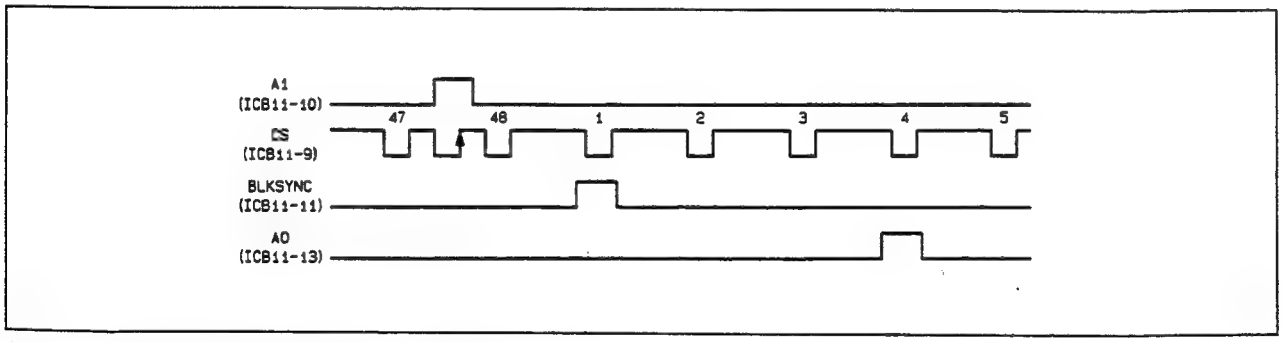



**Fig. 3-6-4. Channel Status Data Write Timing (PG-13 Board)**

### 3. Peak Level Hold Circuit (PG-13 board)

The CH-1/2 data mixed by ICC13 are converted by ICA2 and A3 into parallel data by time division while the CH-3/4 data are converted by ICA4 and A5. The converted parallel data are a twos complement and so they are converted into absolute value data by ICB2, B3, C2 and C3 in the sequence of CH-1, 2, 3 and 4. The converted absolute value data and the peak level data stored in ICB5 and C5 are compared by ICB4 and C4, and the higher of the two data is selected by ICA6-ICA9. The selected data is stored in ICB5 and C5 and used for comparison with the next data.

The above procedure is repeated so that the peak level data of CH-1, 2, 3 and 4 are respectively stored in ICB6/B8, ICB9/C6, ICB7/C8 and ICC7/C9. The stored peak level data are transferred to UPI ICB18 once per frame by pressing INPUT CHECK button on the control panel of the DVR-1000. The 16-bit parallel data are separated into the most significant (high-order) and least significant (low-order) byte, and fetched in the sequence of the CH-1 low-order, CH-1 high-order, CH-2 low-order, CH-2 high-order byte through the CH-4 high-order byte.

### 4. Digital Mixer Circuit (PG-13 board)

The serial data of the 4 channels are input from the AU-86 board to this board at the 256fs clock rate. The input data are converted into parallel data channel by channel by means of ICD7/D3, ICD8/D4, ICD9/D5 and IC10/D6. The parallel data are latched by ICE7/E3, ICE8/E4, ICE9/E5 and ICE10/E6, and they are added in accordance with the principle of time division. Depending on the number of channels whose data are to be mixed, the active time for output enable "OE" of each latch is selected. In other words, based on the selection of only one channel, the "OE" of each channel will be one-fourth when the data of all 4 channels are mixed, one-third when the data of 3 channels are mixed and one-half when the data of 2 channels are mixed. The data which have been added by time division are D/A converted by ICF5, converted into analog signals through the 20 kHz low-pass filter and output to the AT-45 board as the "D MIX" signals. The "D MIX" output level is adjusted using RV2 so that it is equivalent to −10 dBs at the reference level.



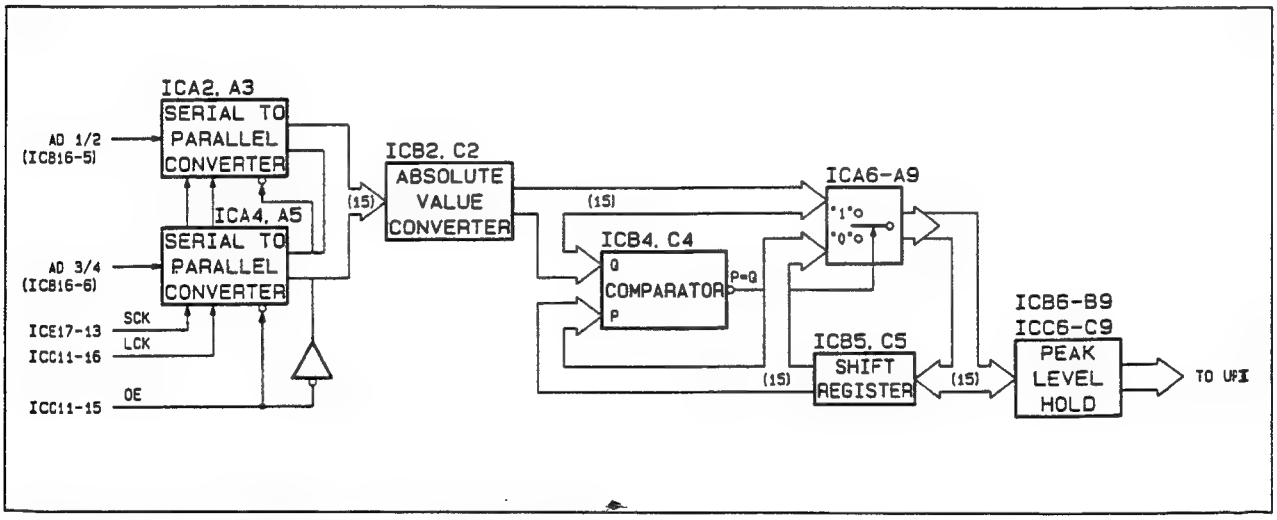



**Fig. 3-6-5. Peak Level Hold Circuit (PG-13 Board)**

**5. Data Latch (PG-13 board)**

The serial audio data from the AN-01 board and also the BYPASS-7 data from the AES/EBU encoder on the PG-13 board are supplied to this circuit. The input signal is selected by ICJ19.

The serial data of each channel, which have been input from the AN-01 board, are respectively converted into parallel data by ICG7/F7, ICG12/F12, ICJ7/H7 and ICJ12/H12.

Similarly, the serial data sent from the AES/EBU encoder on this board are respectively converted into parallel data by ICF8/G8, ICF13/G13, ICH8/J8 and ICH13/J13. The serial data from the AN-01 board are input in sequence from LSB to MSB (LSB first sequence). Conversely, the serial data applying in the BYPASS-7 mode are input in sequence from MSB to LSB (MSB first sequence).

After parallel conversion, the data pass through digital filter ICF9/F14/H9/H14 and are supplied to the serial converter circuits in the next stage. The serial converter circuits of the channels are composed of ICG11/F11, ICG16/F16, ICF11/H11 and ICJ16/H16, and the input data are converted into serial data by the MSB first sequence.

Fig. 3-6-6 shows the timing applying when the serial data input from the AN-01 board are converted into parallel data and also the timing relationship between the data and the "BIT," "LRCK" and "DGR" pulses which are output to the D/A converter circuit.

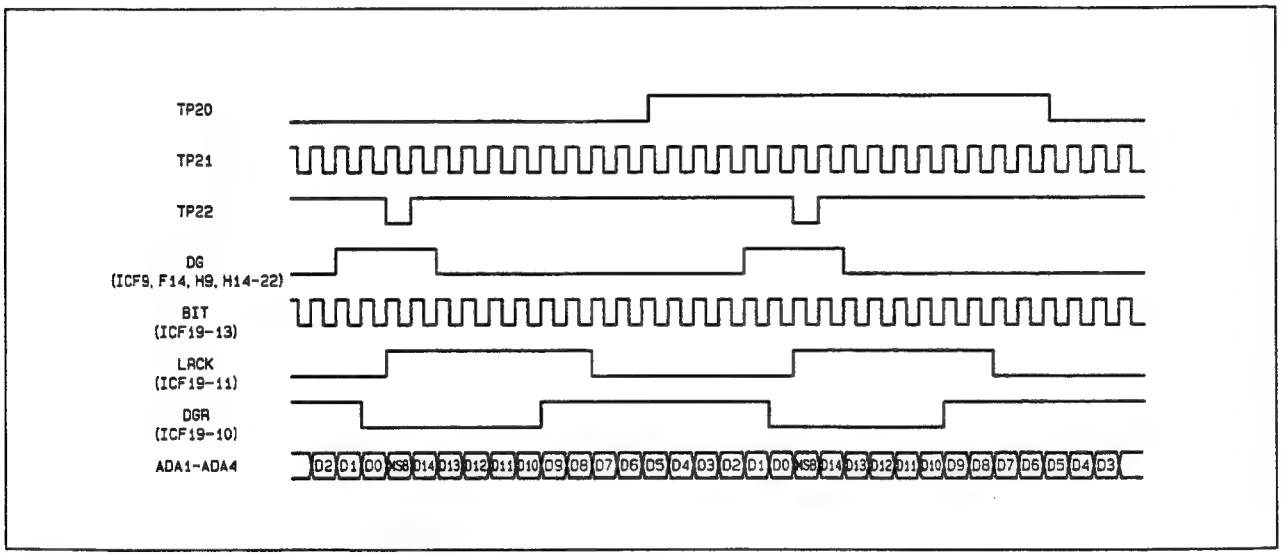



**Fig. 3-6-6. D/A Converter Control Signal Timing (PG-13 Board)**

### 6. Digital Filter (PG-13 board)

The digital filters are composed of ICF9 (for CH-1), ICF14 (for CH-2), ICH9 (for CH-3) and ICH14 (for CH-4). Each of the channels has the same circuit configuration and so the description is confined to only channel-1.

ICF9 is a 16-bit parallel input/output type of digital filter. It is configured as a 121-stage linear phase FIR filter with an 18-bit filter factor, and it serves to provide two-times oversampling.

The "fs" sampling clock pulse is input to pin "CKSY" (pin 19) of ICF9 while the "96fs" clock pulses generated by PLL circuit ICH17/H18/J17/J18 are respectively input to pin "CK0" (pin 20). Starting at the timing produced when fs is low, the 16-bit input data are synchronized with the falling edge of the 47th CK0 clock pulse and fetched to the latch inside ICF9.

The input data format is a twos complement but since digital filter ICF9 is based on offset binary input specifications, the polarity of the most significant bit is reversed for the processing.

The relationship between the input data and output data is such that the input data of 31 samples before (31 × 2T) the output timing and the arithmetically computed results of the sum and product of the 30 samples both before and after (making a total of 60 samples) inclusive of these data are output alternately.

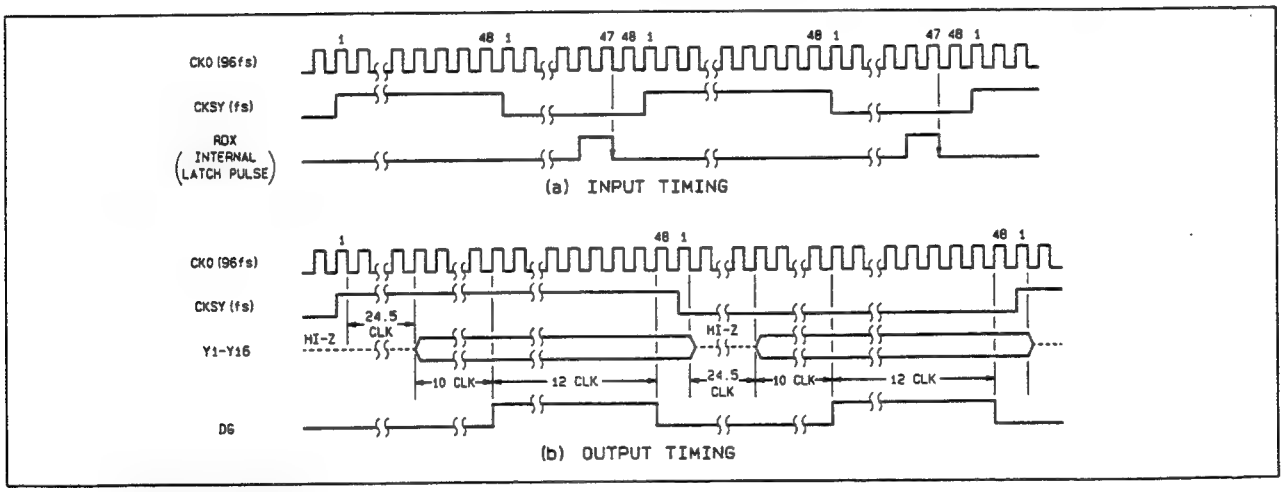



**Fig. 3-6-7. Digital Filter Timing (PG-13 Board)**

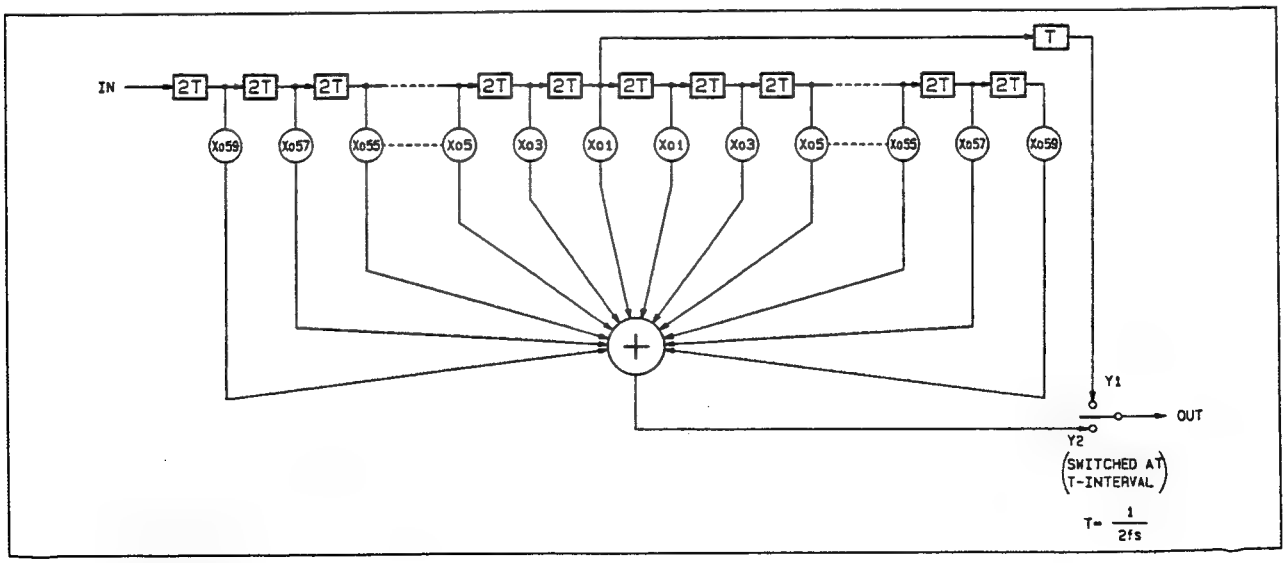



**Fig. 3-6-8. Digital Filter Configuration (PG-13 Board)**

## 4-3-7. AU-86 Board

The AU-86 board may have the board number suffix of "−11," "−12" or "−13." In each case, the configuration of the circuitry is virtually identical although the reference numbers of some parts differ between boards with the "−11/12" suffix and boards with the "−13" suffix. In order to avoid confusion, the following description applies to a board with the "−11" suffix.

The AU-86 board is the board to which the digital audio signals are supplied and it is composed of the following circuit blocks.

- Input signal selector
- AES/EBU decoder
- Asynchronous input detector
- Clock exchanger
- Delay compensation circuit in A/D conversion stage
- ADVANCE head playback signal input processor
- Recording signal selector
- Recording level control circuit
- Format circuit for bypass signals to AN-01 board

The circuits for recording channels CH1 through CH4 are configured in the same way and CH1 is used as an example in the following description.

### 1. Input Signal Selector (ICA24, A25/AU-86)

The following two types of digital audio signals conforming to the AES/EBU format are supplied to the AU-86 board. Fig. 3-7-2 shows the input data format. Reference should be made to Section 4-1. for details on the AES/EBU format.

The method in which the input signal is selected differs according to whether the DVPC-1000 is operating in the remote mode or local mode. When it is in the remote mode, the input signals are selected by the controls of the DVR-1000 control panel. In this case, it is possible to designate independent sources for recording channels CH1/2 and CH3/4. When the DVPC-1000 is in the local mode, the input signals are selected by DIG/ANA selector switch S3 on the AU-86 board. In this case, recording channels CH1 through CH4 are selected simultaneously. Furthermore, the AU-86 board is provided with an audio test signal generator. When TEST SIGNAL ENABLE switch S4-1 is set to the ON position in the test mode (when TEST switch S3/IF-139 is ON), the signals which are selected by test signal selector switch S1 can be used as the input signals. In cases like this, channels CH1 through CH4 are all switched at the same time to the test signal.

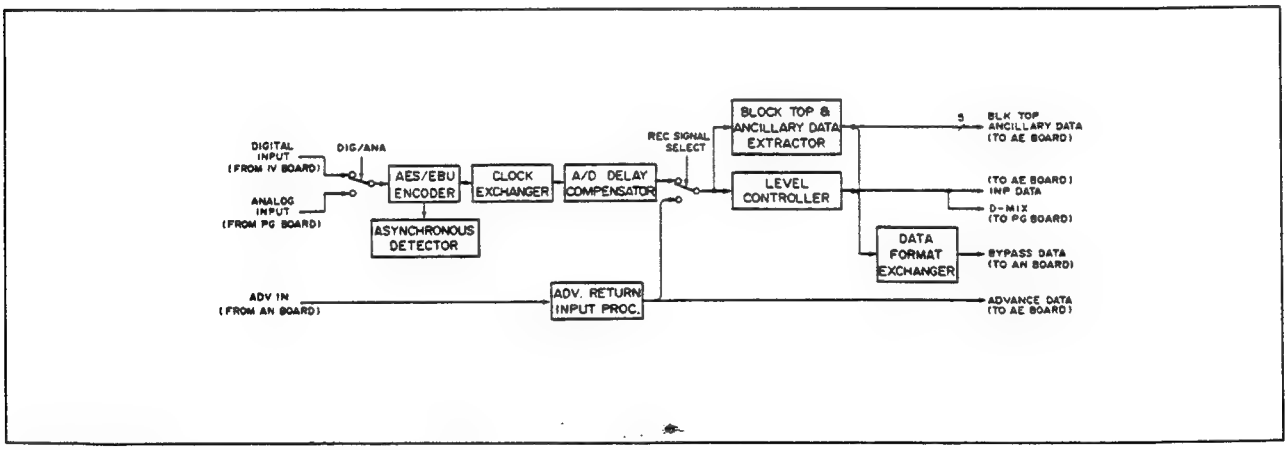



**Fig. 3-7-1. Function Diagram (AU-86 Board)**

**(1) "AA IN 1/2," "AA IN 3/4"**

These are the analog input audio signals which have been A/D converted on the AA-29 board and encoded in the AES/EBU format on the PG-13 board.

The audio channel CH1 and CH2 signals are multiplexed with the subframes A and B of "AA IN 1/2" respectively and supplied to the input signal selector whereas the CH3 and CH4 signals are multiplexed with the subframes A and B of "AA IN 3/4" respectively and supplied to the same circuit.

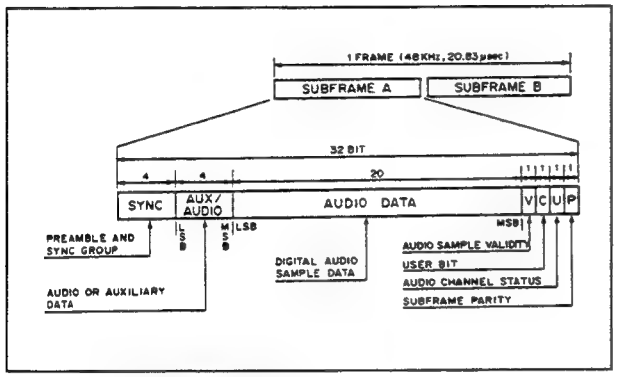



**Fig. 3-7-2. Input Data Format (AU-86 Board) (AES/EBU Format)**

**(2) "DA IN #1," "DA IN #2," "DA IN #3," "DA IN #4"**

After having been input to the DIGITAL AUDIO INPUT-1 or DIGITAL AUDIO INPUT-2 connector on the connector panel, the AES/EBU format digital audio signals are supplied to the input signal selector through the IV board.

The digital audio signal input connector is selected by AUDIO INPUT XLR/DSUB selector switch S2 when the DVPC-1000 is in the local mode and by the controls on the DVR-1000 control panel when the DVPC-1000 is in the remote mode. However, the actual input signal is selected on the IV board in accordance with the "AXD SEL" signal which is output from the UPI on the AU-86 board.

When the input digital audio signals are in the 2-channel mode or stereo mode, subframe A of input signal "DA IN #1" is recorded onto recording channel CH1 and subframe B is recorded onto CH2. Similarly, subframe A of input signal "DA IN #3" is recorded onto CH3 and subframe B onto CH4 while signals supplied to "DA IN #2" and "DA IN #4" are not recorded. When the input signal is in the 1-channel mode (monophonic mode or PRIMARY/SECONDARY mode), the input channel itself serves as the recording channel and subframes A of the channels are recorded onto the same recording channel. Subframes B are not recorded.

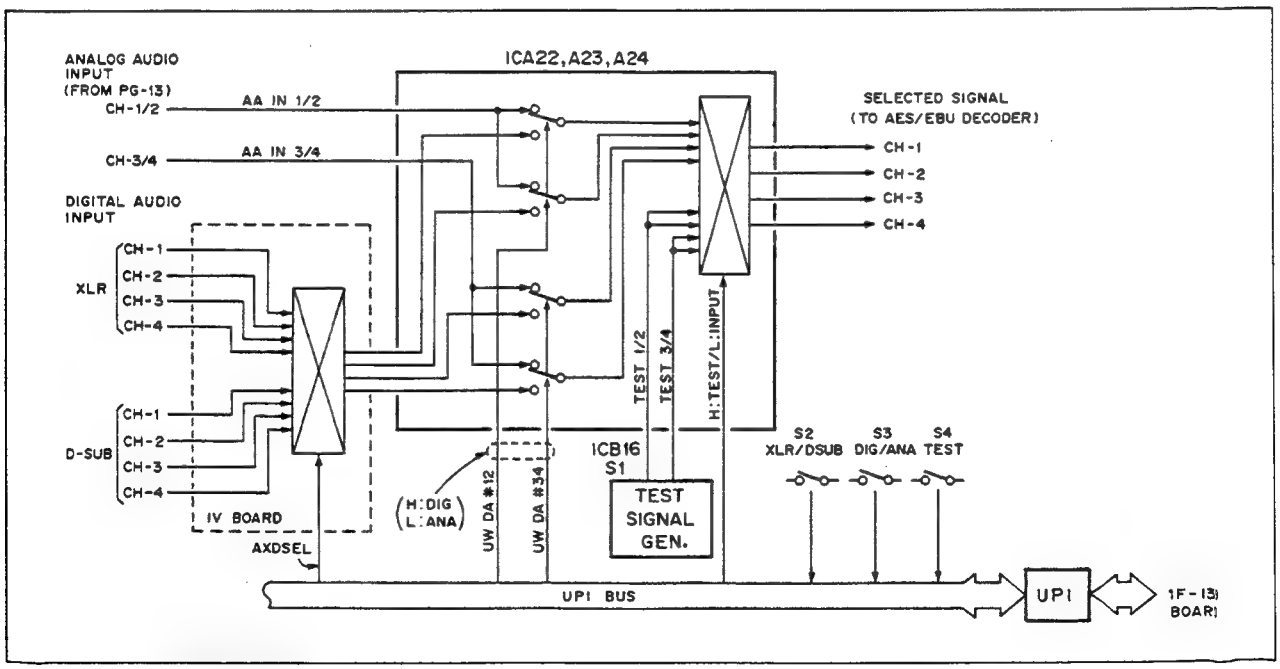



**Fig. 3-7-3. Input Signal Selector (AU-86 Board)**

## 2. AES/EBU Decoder (AU-86 board)

This circuit block is composed of a PLL section and decoder section.

### (1) PLL section

Under the AES/EBU format, biphase mark coding is used for the audio data section although it is not used for the preamble section only. This irregularity is utilized to extract the clock pulses (2 × 48 kHz) in subframe units by means of monostable multivibrator IC1 and to use this as the reference signal during phase comparison. Voltage-controlled oscillator ICA1 generates a signal with a frequency of 12.288 MHz (256 × 48 kHz). This signal is divided down by 128 in counter IC2 and the phase of this signal is compared with the phase of the reference signal by ICA2.

### (2) Decoder section

The decoding of the AES/EBU format is done by ICA3 (CX23025). In this section, the biphase mark coding is decoded and the block top signal "BLK ID" is detected. After having been decoded and demodulated into the non-return-to-zero (NRZ) code, the serial data are output as the "FEED" signal from pin 11 of ICA3. At the same time, the LRCK, WCK and BCK clock signals as well as the block top "BLK ID" signal are output from ICA3.

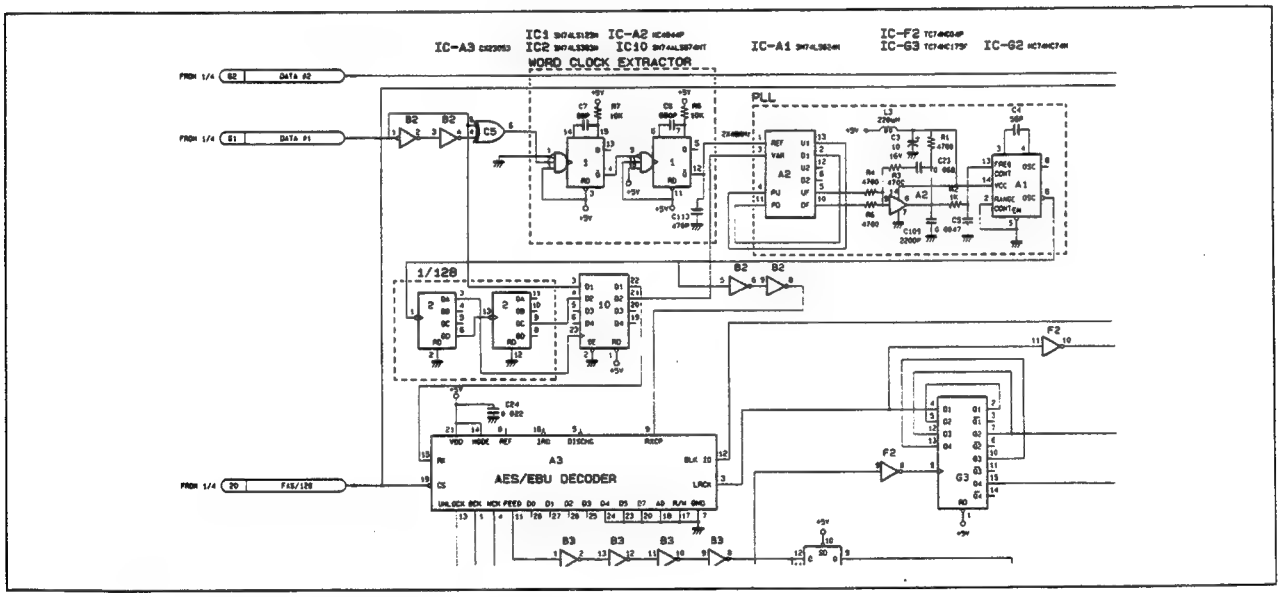



**Fig. 3-7-4. PLL Circuit/AES/EBU Decoder (AU-86 Board)**

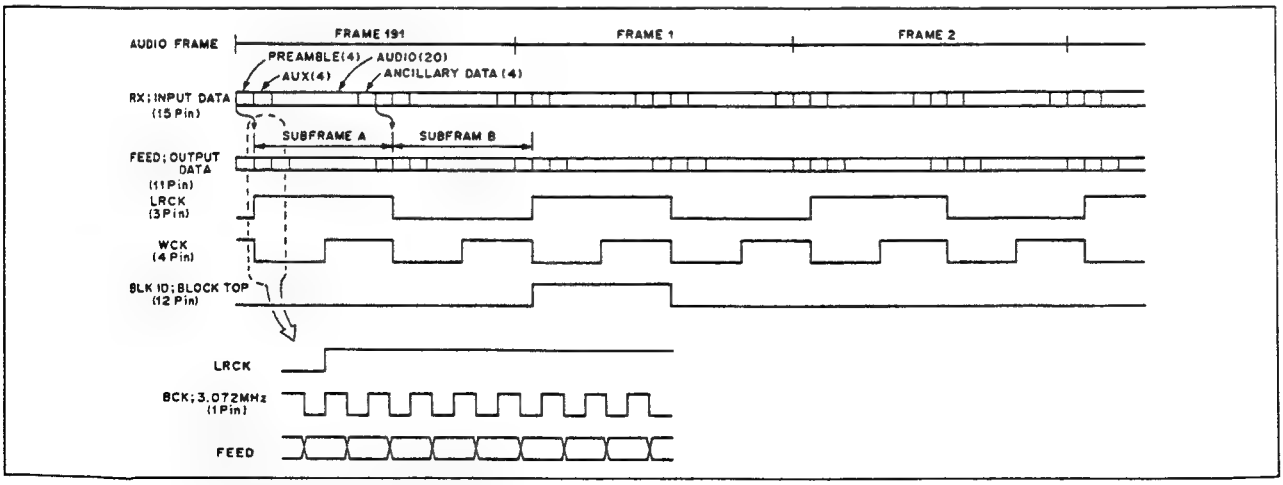



**Fig. 3-7-5. AES/EBU Decoder Input/Output Timing Chart (AU-86 Board)**

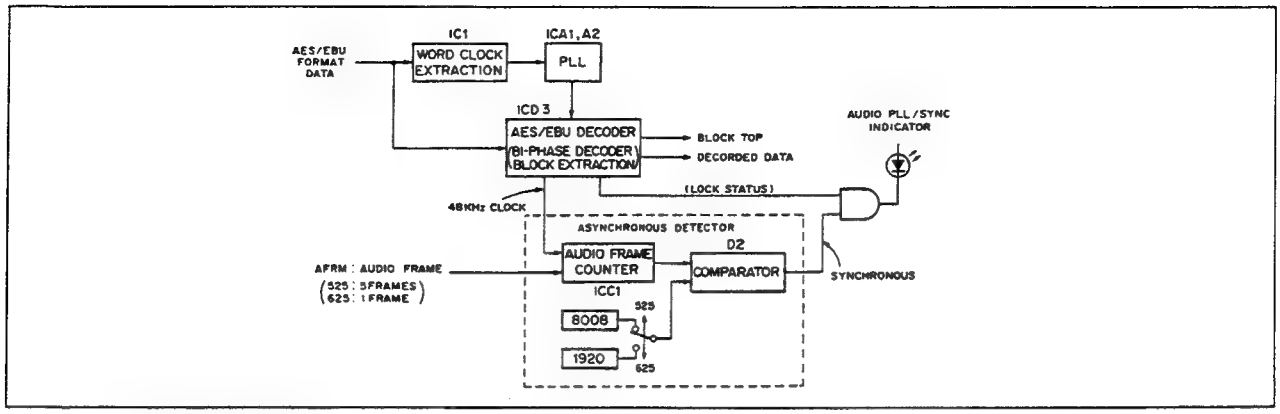



**Fig. 3-7-6. Asynchronous Detector (CH1/AU-86 Board)**

### 3. Asynchronous Input Signal Detector (AU-86 board)

This circuit uses the sample number of the input signal to detect whether the input signal is synchronized with the reference signal of the VTR. Channels 1 through 4 feature the same circuit configuration and so the description below is confined to channel-1.

When the input signal is synchronized with the VTR reference signal, audio data of 8008 samples are supplied between 5 frames with a 525/60 system and audio data of 1920 samples are supplied between 1 frame with a 625/50 system. ICC1 functions to count the sample number between the audio frames and ICD2 detects the synchronization. In actual fact, the values of the least significant 4 bits are compared and the synchronization is detected.

When the PLL circuit in the AES/EBU decoder section is locked and the input signal is synchronized with the VTR reference signal, the green LED (D9) lights.

### 4. Clock Exchanger (AU-86 board)

The output signal of the AES/EBU decoder is synchronized again with the internally generated 48 kHz frequency and, at the same time, jitter is absorbed. When the input signal is not synchronized with the VTR reference signal, the samples are removed or repeated until the prescribed sample number is reached, and with all subsequent processing the input signals are all treated as synchronized. Also, in this circuit the block top information (block top = high) is inserted into the audio signals.

In actual fact, the clock signals for succession are generated by PLD (programmable logic device) ICH3 and the data are synchronized by serial-parallel-serial conversion.

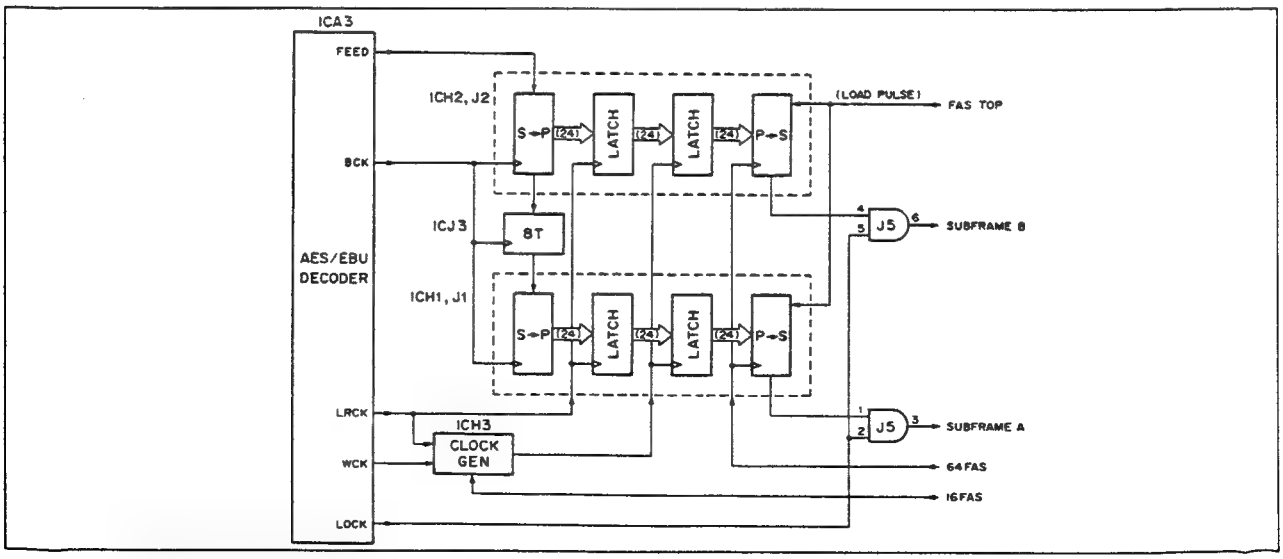



**Fig. 3-7-7. Clock Exchanger (CH-1/AU-86 Board)**

### 5. Delay Compensation Circuit in A/D Conversion Stage (AU-86 board)

When a digital input signal has been selected, a signal with zero delay is supplied to the AU-86 board but when an analog input signal has been selected, a delay equivalent to approximately 5 samples is produced from the time the signal is supplied to the DVPC-1000 and until it is input to this board. This delay is produced by the delay arising from A/D conversion and the operation of the filter. The delay compensation circuit delays the signal by 5 samples when the digital input signal is selected, and it converts the signals supplied in the 4-channel parallel signal format into a 4-channel multiplexed serial format, and outputs them.

Selection between the analog input and digital input signals is conducted independently for channels 1/2 and for channels 3/4, and so two memories in series are used for the processing. In actual fact, the delay equivalent to 5 samples is produced by the pre-stage memory ICC14 and the delayed signal and zero delay signal (input signal) are simultaneously written into post-stage memory ICF13 and F14. The read out signal from this post-stage memory is output with the signals having zero delay when analog signal input mode is selected and with the signals which have been delayed by 5 samples when digital signal input mode is selected. Input to this circuit is activated by a 64×48 kHz (3.072 MHz) frequency and in the stages following the output section a 256×48 kHz (12.288 MHz) frequency is used.

The input mode is selected in the input section of this circuit. In the 2-channel mode (or stereo mode), the subframe A signal from the channel-1 connector is selected for channel-1 and the subframe B signal from the channel-1 connector is selected for channel-2. In the 1-channel mode (monophonic or PRIMARY/SECONDARY mode), the subframe A signal from the channel-1 connector is selected for channel-1 and the subframe A signal from the channel-2 connector is selected for channel-2. The same applies to channel-3 and channel-4. With an analog signal input, channels-1/2 and channels-3/4 are multiplexed, the signals are supplied to this board, and the same process of selection as for the 2-channel mode is then undertaken automatically.

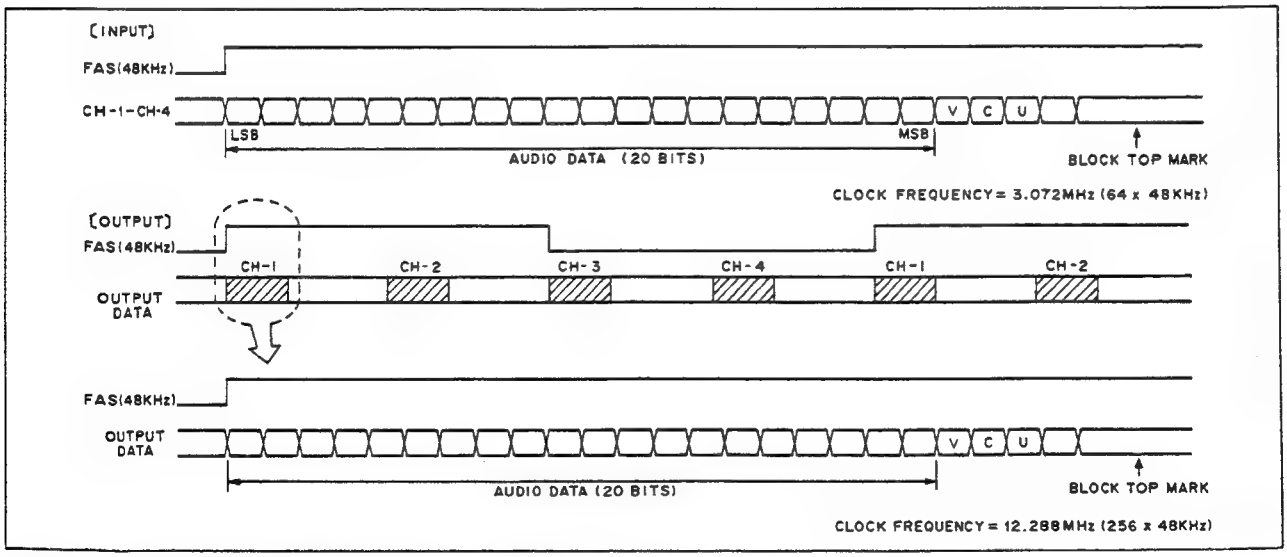



**Fig. 3-7-8. Input/Output Timing for Delay Compensation Circuit (AU-86 Board)**

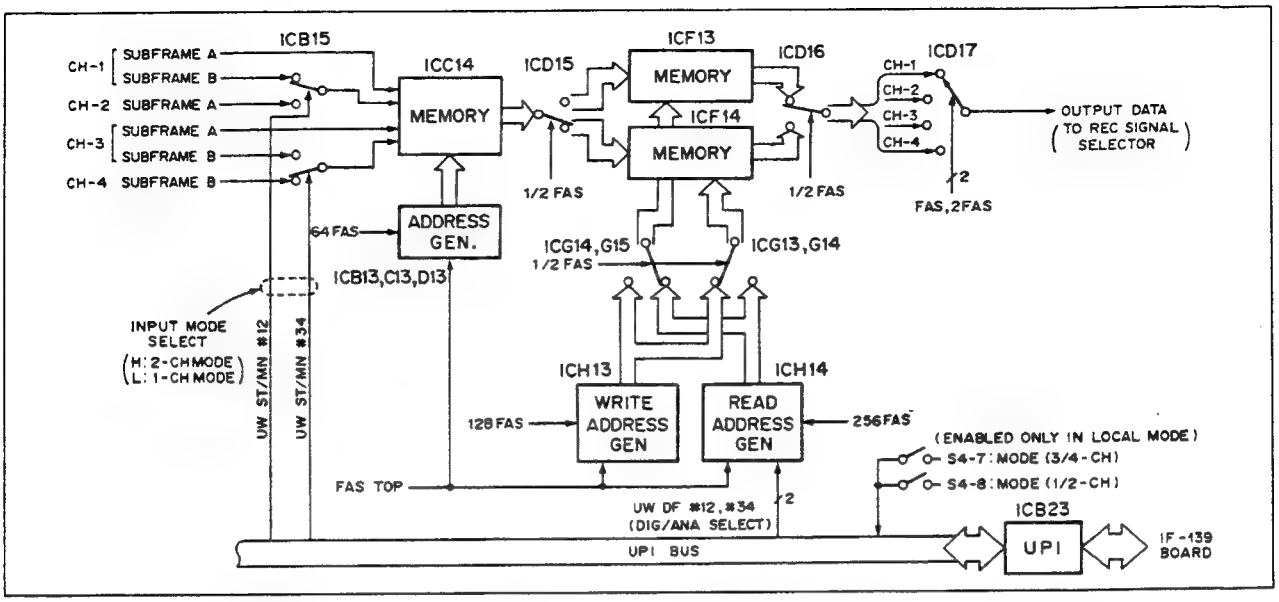



**Fig. 3-7-9. Delay Compensation Circuit in A/D Conversion Stage (AU-86 Board)**

### 6. ADVANCE Head Playback Signal Input Processor (AU-86 board)

The playback data from the ADVANCE head are required when cross-fade during editing or dubbing between channels (when, for instance, recording the playback data of channel-1 onto channel-2). The ADVANCE head playback data from the AN-01 board are supplied to the AU-86 board as 4-channel multiplexed serial data. The ADVANCE head playback data supplied to the AU-86 board are fetched to memory ICE18 and F18.

Two sets of the signals selected as the edit source and the signals used with cross-fade are output from this circuit at the timing shown in Fig. 3-7-10.

### 7. Recording Signal Selector (AU-86 board)

In accordance with the control signal from UPI (ICB23), this circuit functions to select the signals to be recorded. In the REC mode, the output from the delay compensation circuit (see Section 5.) in the A/D conversion stage is always selected. In an editing mode (such as EDIT), depending on the selection of the edit source from the control panel, the output from the delay compensation circuit in the A/D conversion stage and the ADVANCE head playback signal are selected channel by channel and output to the level control circuit in the next stage.

The V (validity bit), U (user bit) and C (channel status bit) informations and the block top information are extracted from the selected signal and sent to the AE-06 board. During spot erasing, the validity bit is output as zero.

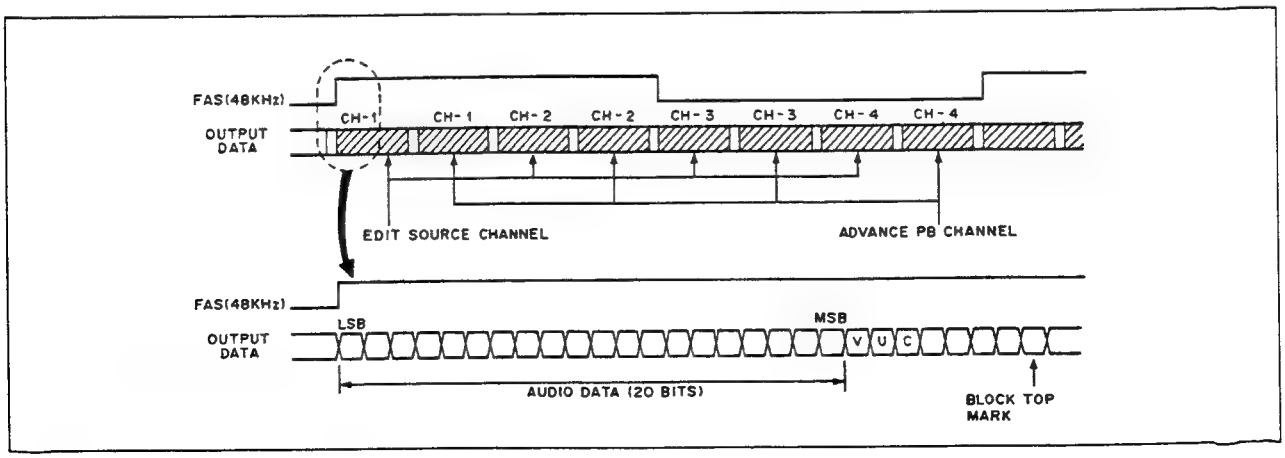



**Fig. 3-7-10. Output Timing for ADVANCE Head Playback Signal Processor (AU-86 Board)**

### 8. Level Control Circuit (AU-86 board)

This circuit controls the level during recording. When input to the multiplier, the sign bit (MSB) of the input data is held by ICK14 and then input to the circuit itself. A 16-bit coefficient is given from UPI (ICB23) to multiplier ICJ17 and J18 and, with $8000_H$ as 0 dB, the level can be controlled from $-\infty$ to +6 dB.

If the AU-86 board has the "−13" board number suffix, the level control can be changed to a broader range extending from $-\infty$ to +12 dB by shorting jumper plug CN3. The level control data (arithmetic coefficient) are given to the arithmetic unit from the DVR-1000 through the IF-139 board and UPI. However, UPI communication is once per frame and so the gain will change suddenly and irritating noise will be heard if the coefficient is supplied directly from the UPI to the arithmetic unit. On an AU-86 board which has the "−13" board number suffix, therefore, a PROM for controlling the coefficient is installed between the UPI and arithmetic unit. The PROM works by limiting the change to only one level per sample.

An overflow of the multiplier is identified by using ICJ23 to detect the change in the sign bit of the multiplier output. When the overflow is positive (+), "$7FFF_H$" is output; when it is negative (−), "$8000_H$" is output. The data are output from this circuit by means of serial-parallel-serial conversion at a timing which is delayed by one-fourth of 48 kHz behind the input to the level control circuit.

After the ADVANCE head playback signals are delayed by one-eighth of 48 kHz in this circuit, the sign bit (MSB) is held and then output.

### 9. Bypass Signal Format Circuit (AU-86 board)

In this circuit, the multiplexed 4-channel serial audio data as well as the validity bit, user bit, channel status bit and block top data are fetched to memory ICG25, converted into the AN-01 board input signal format and output.

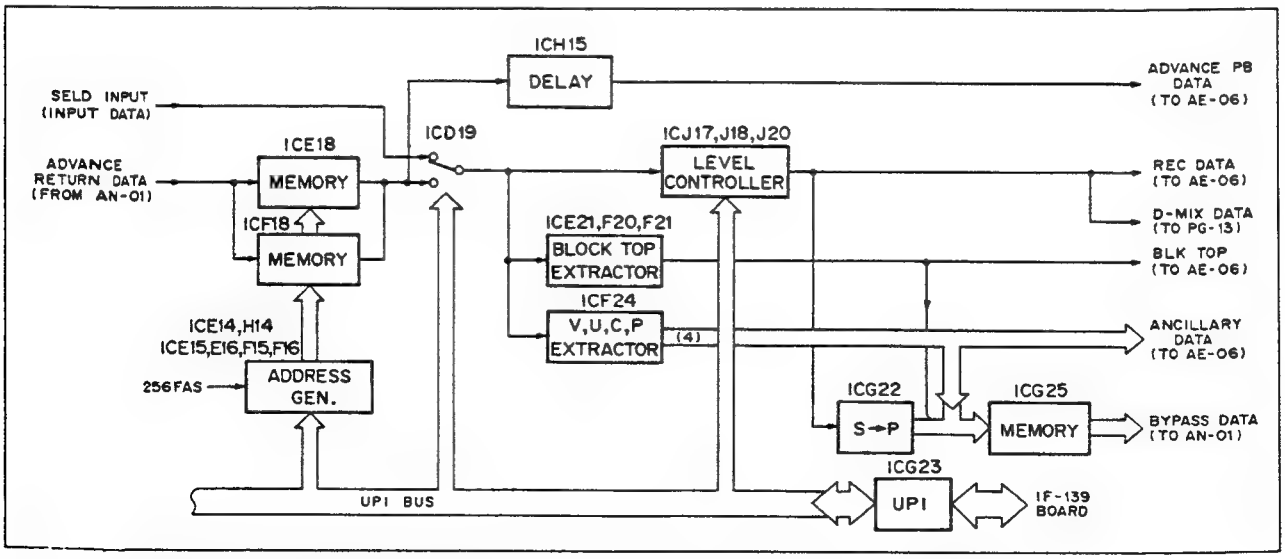



**Fig. 3-7-11. ADVANCE Head Playback Signal Input Processor/Level Control Circuit (AU-86 Board)**

## 4-3-8. AE-06 Board

The AE-06 board is a processing board on the digital audio data recording system and it is composed of the following circuits.

- Cross fader and coefficient generator
- Peak level hold circuit
- Audio data word mode setting circuit
- Audio data sequence re-arranging circuit
- Channel status processor
- Addition data generator
- User data processor
- Audio outer encoder

The input audio data and ADVANCE head playback data are supplied from the AU-86 board to the cross fader circuit on the AE-06 board. This circuit multiplies the coefficient corresponding to the VTR mode to the respective signals and generates the recording audio data. In the peak level hold circuit section the maximum value of the recording audio data is detected and output frame by frame to the IF-139 board via the UPI.

The channel status data and AES/EBU block top data from the AU-86 board are supplied to the addition data generator. The user data from the IF-139 board are supplied to the user data processor. In the audio outer encoder the audio data, addition data and user data are fetched to the memories, the data readout from the memories is controlled and the audio outer code block is generated. At the same time, the outer check word based on the Reed Solomon code is added and output to the IE-17 board.



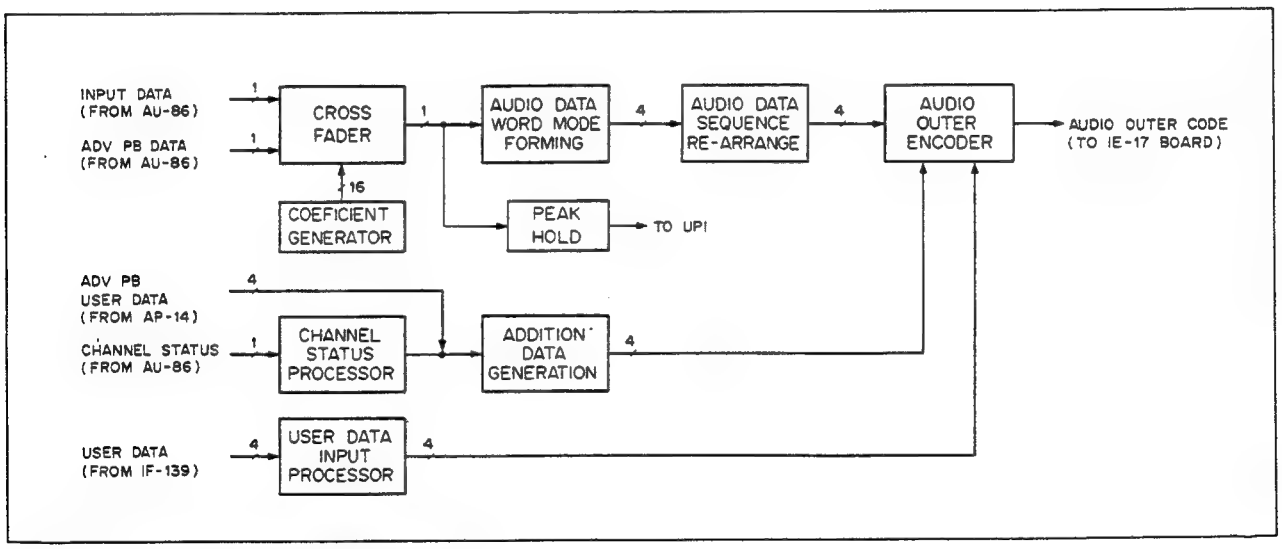



**Fig. 3-8-1. Function Diagram (AE-06 Board)**

### 1. Cross Fader (AE-06 board)

Coefficients "X" and "1-X" are multiplied respectively to the input audio data and ADVANCE head playback data supplied from the AU-86 board, and the results are added and then output. The actual calculation is conducted by 1-bit × 8-bit multipliers ICG29 and G30 (G31, G32) and by adder ICH31. Two multipliers are used for each data for the 16-bit multiplication. In addition, they process the 4-channel multiplexed data.

In the REC mode and EE mode, coefficient "X" at the input audio data side is fixed at 1 (8000H) whereas coefficient "1-X" at the advance playback data side is fixed at 0 (0000H), and these are output to the audio outer encoder without changing the input audio data. In the PLAY mode, the procedure is reversed: they are output straight through the advance playback data side.

In the edit mode and spot erase mode, cross-fade is applied at the IN and OUT points of each mode, and during the edit and spot erase periods the input audio data are output directly. (However, during spot erase mode all the bits in these data are set to "0.")

If "sound-mute-sound" (muting of editing periods) has been designated while conducting a preview operation in an edit mode and if the spot erase mode has been established, the recording data will be muted (all bits are set to "0") by the "MUTE IN/MUTE ADV" control signal sent from the UPI (ICA17).

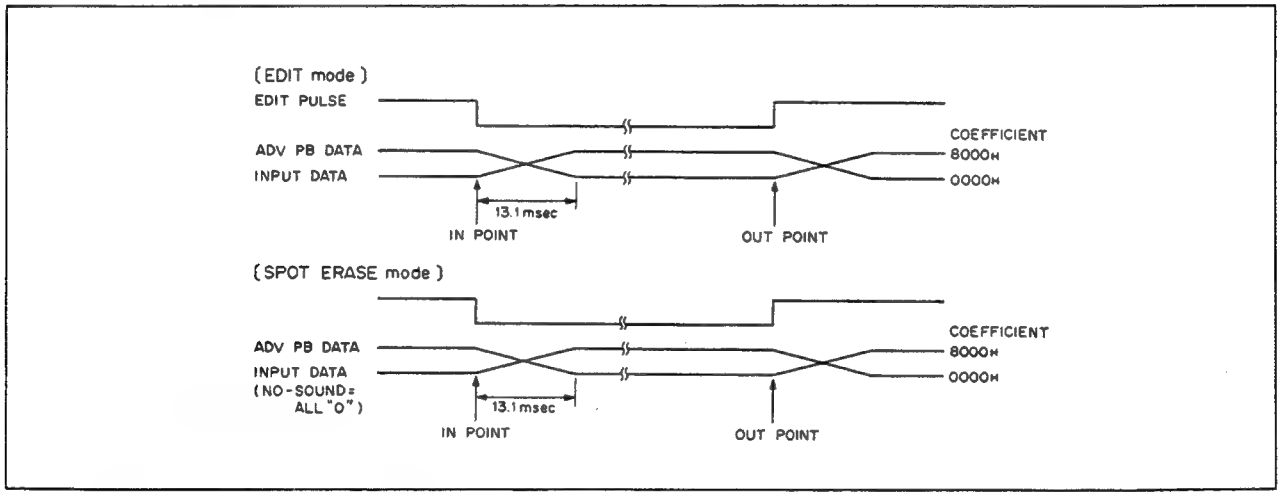



**Fig. 3-8-2. Cross Fading (AE-06 Board)**

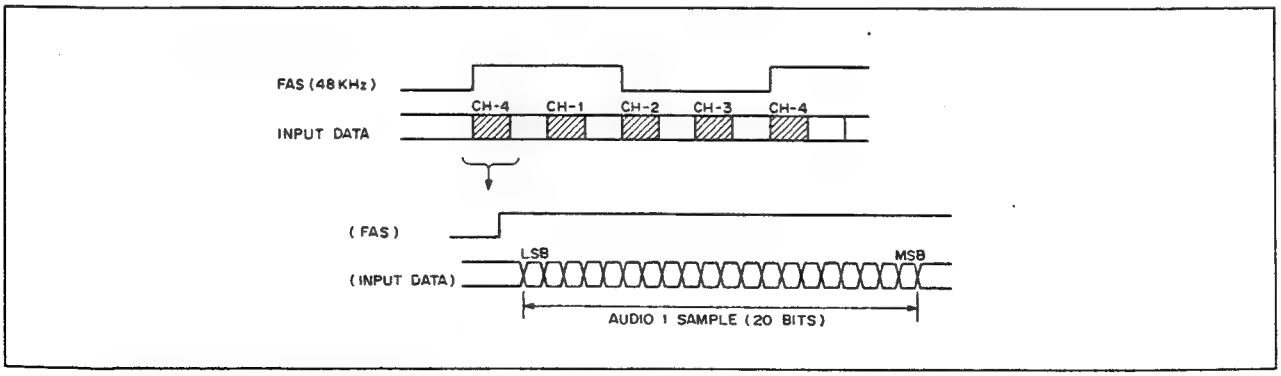



**Fig. 3-8-3. Data Input Timing (AE-06 Board)**

(The figure shows the timing as it relates to the input audio data although the ADVANCE head playback data are also supplied at the same timing.)

## 2. Coefficient Generator (AE-06 board)

This is the circuit which generates the "X" and "1-X" coefficients which are used with cross-fade.
The coefficient target value and the amount of change (fading gradient) per sample are fetched from UPI ICA17 to memory ICE10, they are compared with the coefficient currently generated, the coefficient is changed into sample units by the gradient applied until the target value is reached, and the coefficient is generated.
Arithmetic processing is conducted with 4 bits and, in accordance with the control exercised by ROM ICE13, F14 and PLD (programmable logic device) ICE14, the following process is repeated: the target value, amount of change (fading gradient) and current coefficient are fetched to memory ICE10, output in sequence, calculated and the results are fetched again.
At present, the target value is fixed at "8000H," and the amount of change is fixed at "034H" in both the edit mode and spot erase mode.
The coefficient generator is activated by a clock signal with a frequency of 256×48 kHz, and the calculation of the coefficient is completed within a time period of approximately 1/4×48 kHz. Consequently, the coefficient calculation is conducted as shown in Fig. 3-8-4.

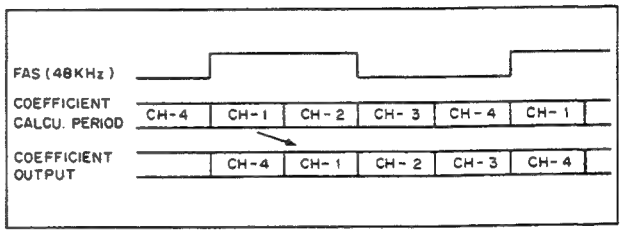



**Fig. 3-8-4. Timing of Coefficient Calculation (AE-06 Board)**

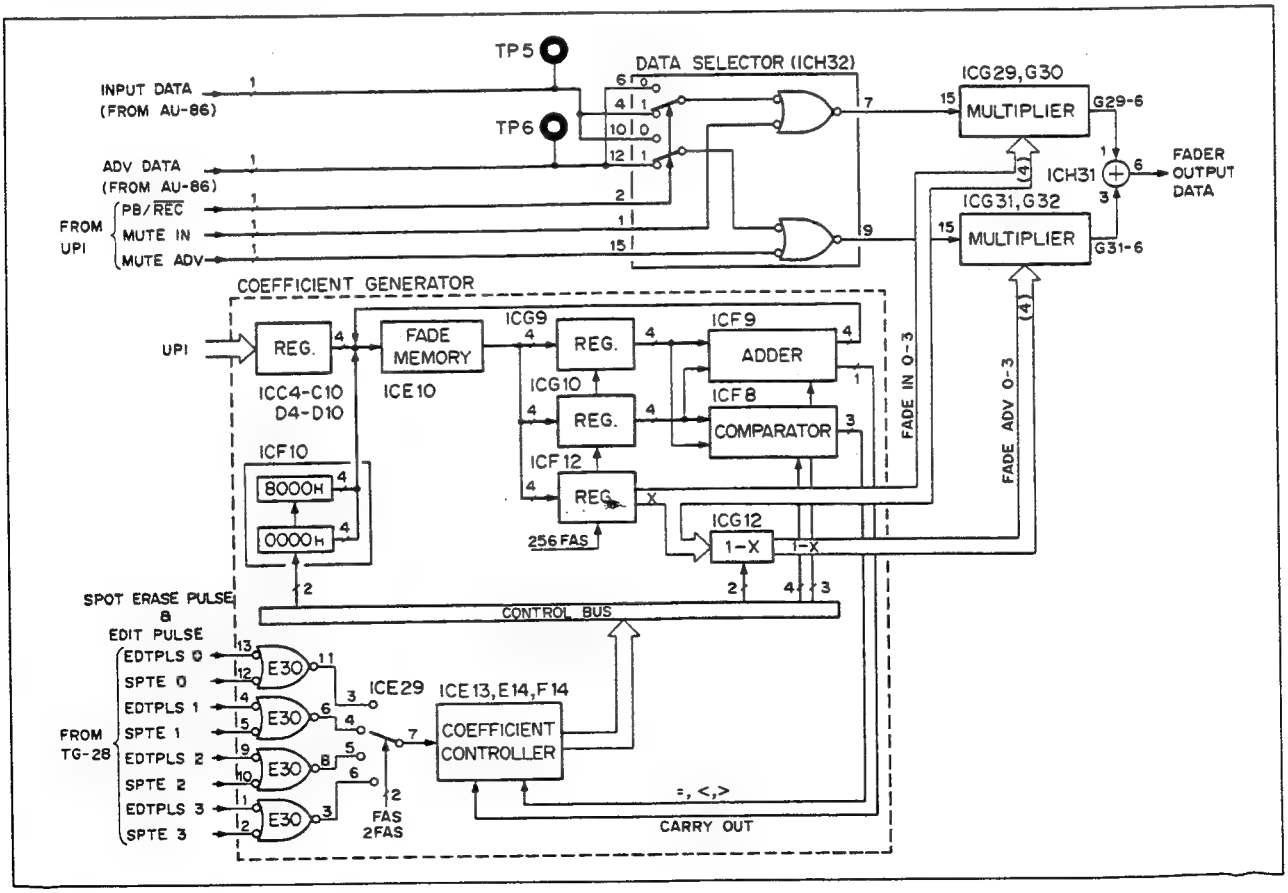



**Fig. 3-8-5. Cross Fader and Coefficient Generator (AE-06 Board)**

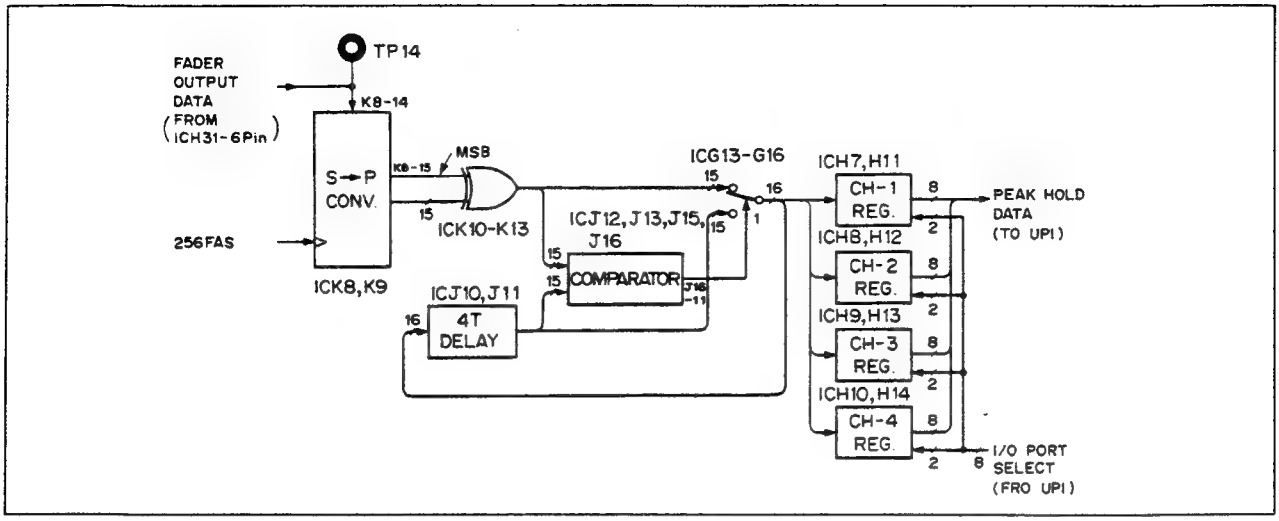



**Fig. 3-8-6. Peak Level Hold Circuit (AE-06 Board)**

### 3. Peak Level Hold Circuit (AE-06 board)

After they have been output from the cross fader, the serial data are converted into 16-bit parallel data by serial-parallel converter ICK8 and K9, and they are supplied to the peak level hold circuit.

These data are a 2's complement binary code and are converted into an absolute expression by exclusive OR gate ICK10-K13. Channel by channel, comparator ICJ12, J13, J15 and J16 compare the data which have been converted into the absolute expression and the current maximum value and the larger of the two values is fetched to register ICH7-H14. UPI ICA17 reads out the maximum value once per frame and sends it as the peak value to the DVR-1000 via the IF-139 board. Immediately after they have been fetched to the register, the data are held in register ICJ10 and J11 as the current maximum value and then used for the next comparison.

### 4. Audio Data Word Mode Setting Circuit (AE-06 board)

Under the CCIR-657 recommendation (D-1 format), the regulation stipulates that the one audio data sample (20 bits) can be selected from among the 8 modes listed in Table 3-8-1. In this circuit, the 20-bit serial audio data which have been output from the cross fader are converted into 4-bit parallel data, and the least significant 4 bits of the 20-bit audio data to be recorded are generated from among a total of 8 bits composed of the least significant 4 bits of the audio data and the 4-bit ancillary data (V, U, C, R ancillary data bits). The 3-bit data "LNGH" indicating the word mode applied channel by channel from UPI ICA17 is time division multiplexed by multiplexer ICJ30 and ICJ31. The recording audio data are delayed by 112 clocks by the 64×48 kHz (3.072 MHz) clock signal at ICK30, and the data of channels-1 through 4 which have been sampled at the same timing during the 48 kHz period are output.

| MODE | LNGH | | | AUDIO LENGTH | ANCILLARY BITS | | | |
|---|---|---|---|---|---|---|---|---|
| | 3 | 2 | 1 | | C | U | V | R |
| 0 | 0 | 0 | 0 | 16 BITS | X | X | X | X |
| 1 | 0 | 0 | 1 | 17 BITS | X | X | X | – |
| 2 | 0 | 1 | 0 | 18 BITS | X | – | X | – |
| 3 | 0 | 1 | 1 | 18 BITS | X | X | – | – |
| 4 | 1 | 0 | 0 | 19 BITS | X | – | – | – |
| 5 | 1 | 0 | 1 | 19 BITS | – | – | X | – |
| 6 | 1 | 1 | 0 | 19 BITS | – | X | – | – |
| 7 | 1 | 1 | 1 | 20 BITS | – | – | – | – |

CHANNEL STATUS
USER DATA
VALIDITY BIT
RESERVED

**Table 3-8-1. Audio Data Word Mode Setting (AE-06 Board)**

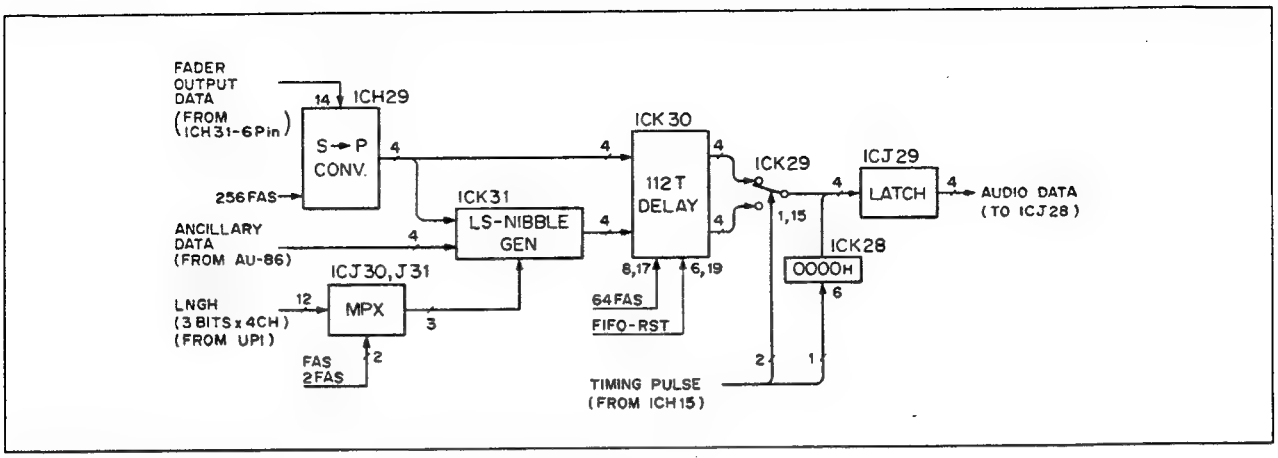



**Fig. 3-8-7. Audio Data Word Mode Setting Circuit (AE-06 Board)**

### 5. Audio Data Sequence Re-arranging Circuit (AE-06 board)

This circuit serves to convert the audio data, which have been input continuously in terms of time, into the audio outer code sequence and output them.

The continuously supplied audio data are written into memory ICJ28 in audio segment units. In contrast, the output data feature a rate of 4 outer code blocks per 48 kHz period. This means that readout is approximately 1.9 msec shorter than writing. Hence, the start of readout is delayed by approximately 2.2 msec from the start of writing. During readout, the channels are switched with each outer code block for readout in the following sequence: "CH-1 (EVEN) – CH-2 ... CH-4 (E) – CH-1 (ODD) ... CH-4 (O) – CH-1 (E) ...". Under the D-1 format, the audio data are separated into the odd and even samples and code blocks are configured. Consequently, 2 code blocks/channel apply per segment and the audio data in one code block comprise 161 or 160 samples.

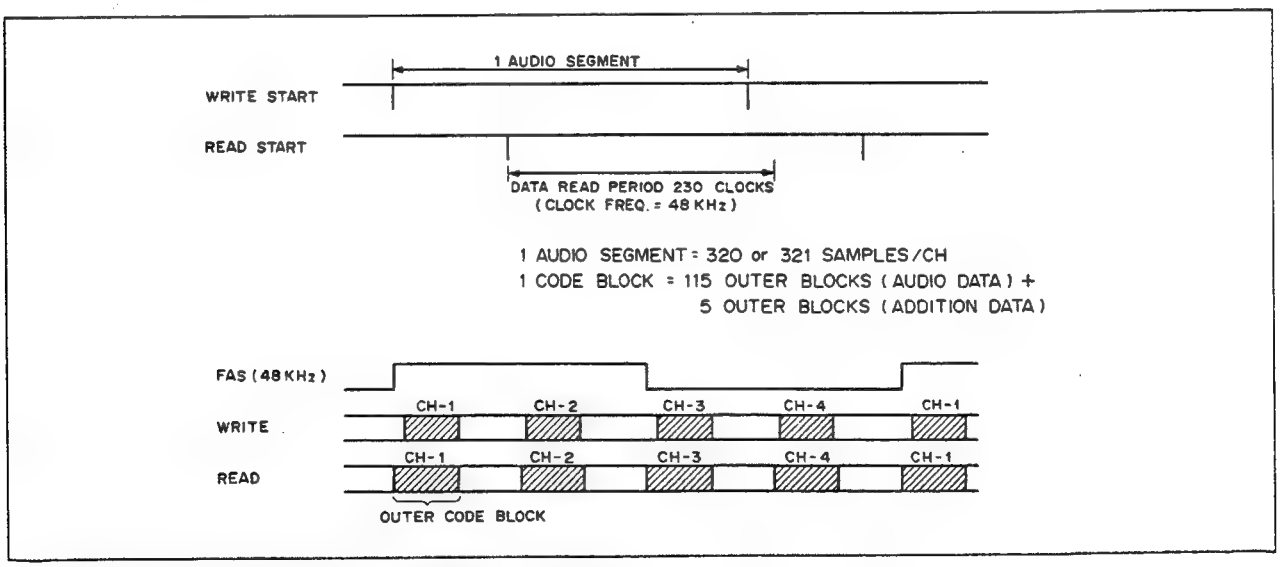



**Fig. 3-8-8. Audio Data Sequence Re-arranging (AE-06 Board)**

### 6. Channel Status Processor (AE-06 block)

In order to record the pre-emphasis information (PREF) and channel use information (CHAN) and in order to display the pro/consumer use information and audio/non-audio information as warnings, these informations are extracted from among the channel status data in this circuit block.

Channel status data "ANCI2" supplied from the AU-86 board is written into memory ICJ3 in AES/EBU clock units. The data in one AES/EBU block are read out from this memory segment by segment, and byte-0 and byte-1 of the channel status data are extracted. Simultaneously, the flag (bit-4/byte-22) indicating the reliability of byte-0 and byte-1 is also extracted, the cyclic redundancy check character (CRCC) is calculated and when the readout of the AES/EBU block data has been completed, the CRCC detection result is fetched as error information. Only when no error is indicated for both the flag (bit-4/byte-22) and CRCC, the byte-0/byte-1 data are written into memory ICJ2 for the addition data. If an error has been detected for either the flag or CRCC, the writing of data is prohibited. When errors are continuously generated in 8 AES/EBU blocks, byte-0 and byte-1 are written into the memory and the warning information which indicates that an error has arisen in the channel status data is output to UPI ICA17.

### 7. Addition Data Generator (AE-06 board)

This circuit generates the addition data (BCNT, ELAP, LNGH, SEQN, S.MARK0, S.MARK1) in the audio product block. The addition data indicate the information described below.

PREF: Pre-emphasis information in channel status data

CHAN: Channel use information in channel status data

BCNT: This denotes valid audio sample number in code block.

ELAP: This marker applies when different data are recorded over the original data and copy data so that cross-fade is conducted at the IN and OUT editing points. With this machine, moreover, an ADVANCE head is used for the cross-fade and so the marker (ELAP) is not used.

LNGH: This data prescribes the audio data word mode.

SEQN: This indicates the segment number. Numbers 0 through 14 are repeated.

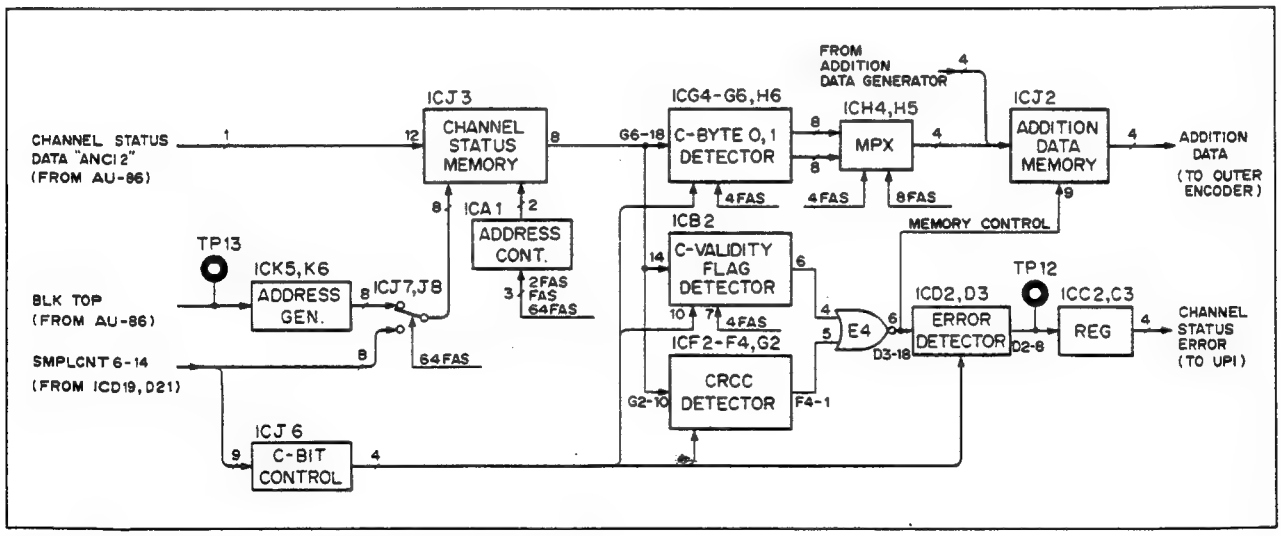



**Fig. 3-8-9. Channel Status Processor Circuit (AE-06 Board)**

S.MARK0: This indicates in the code block the position of the top data in the AES/EBU block that appears first.

S.MARK1: This indicates in the code block the position of the top data in the AES/EBU block that appears last.

Note: If the top data of the AES/EBU block do not exist in the code block, "AA$_H$" is inserted into S.MARK0/S.MARK1.

"LNGH" is provided from UPI ICA17 and "SEQN" is set by counter ICE26 which uses the segment pulse as the clock input. "BCNT" is set to "160" or "161" depending on the segment number, and "ELAP" is always fixed at "0." S.MARK0 and S.MARK1 are provided by latching the output of counter ICD19 and D21, which counts the sample number in the segments, by the top data of the AES/EBU block and by decoding this signal.

The above-mentioned addition data are written into addition data memory ICJ2 with each audio segment at the timing applying immediately after segment pulse "ASEG" has been output. In a mode such as audio editing or spot erasing in which the user data are not rewritten, these user data must be played back by the ADVANCE head and recorded again at the same position. As a result, the ADVANCE playback user data are fetched from the AP-14 board to the AE-06 board and these data are written after "PREF" and "CHAN" have been written into addition data memory ICJ2.



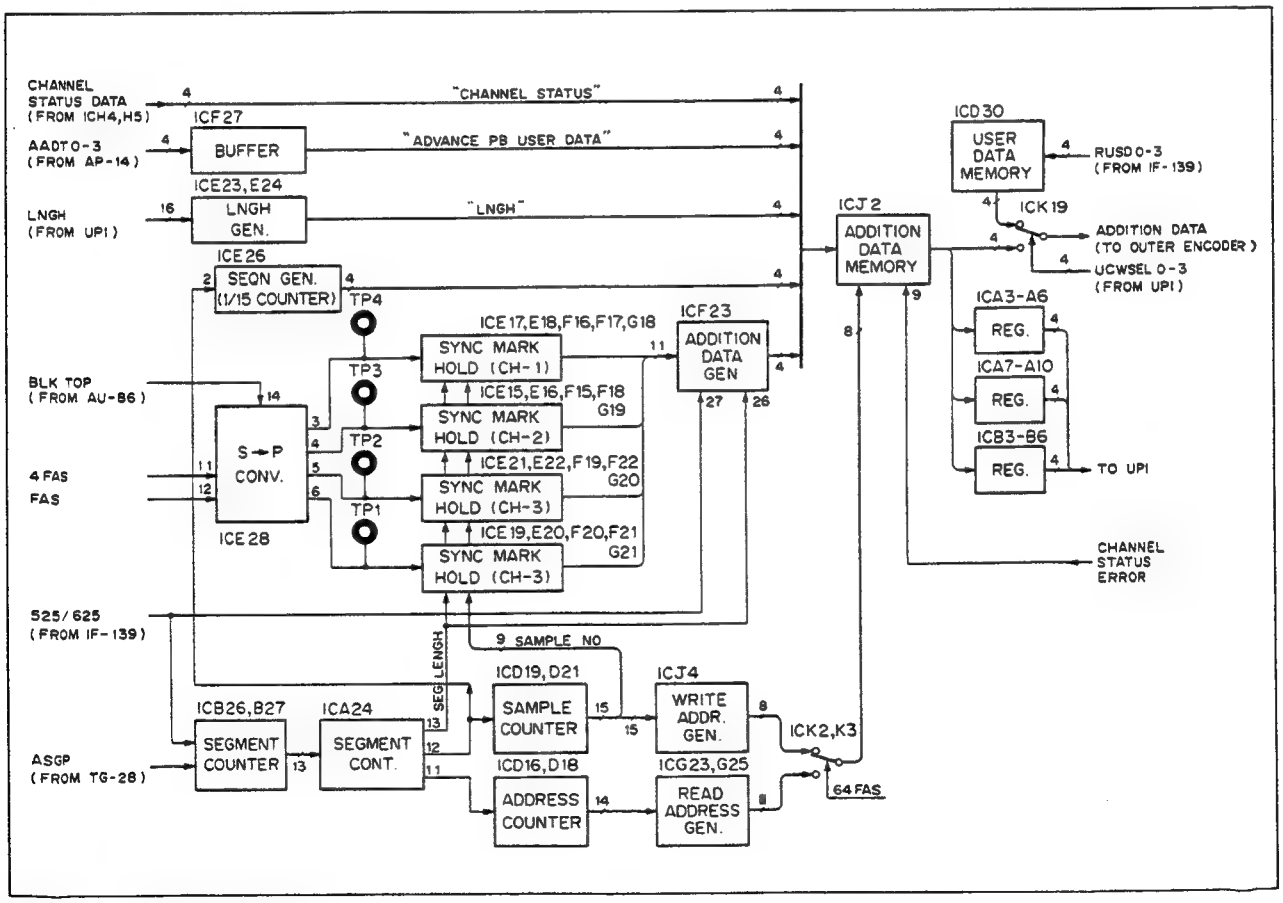



**Fig. 3-8-10. Addition Data Generator Circuit (AE-06 Board)**

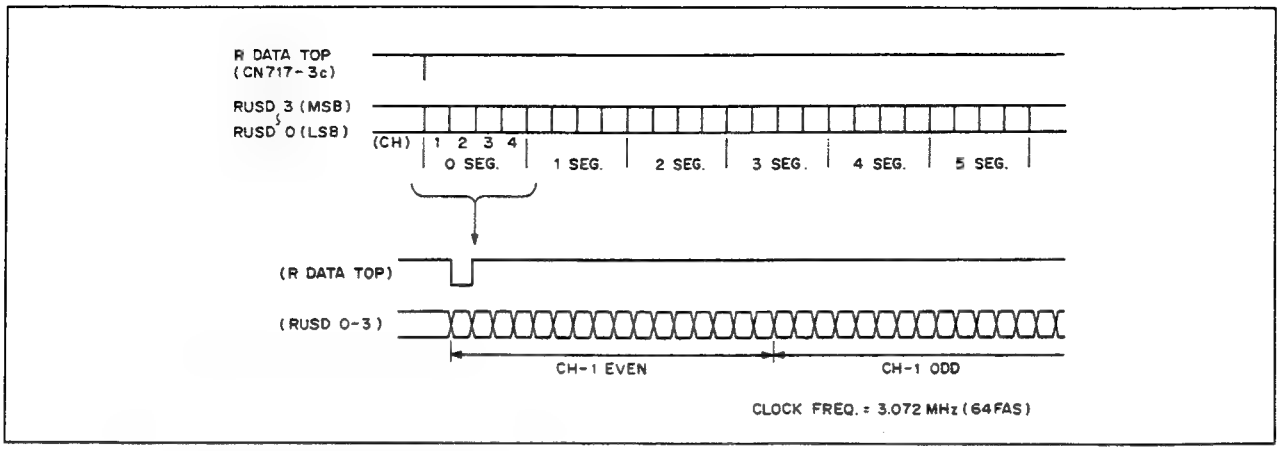



**Fig. 3-8-11. User Data Input Timing (AE-06 Board)**

### 8. User Data Input Processor (AE-06 board)

User data "RUSD3-RUSD0," which are equivalent to one frame and which have been supplied from the IF-139 board, are written via ICD31 and D32 into user data memory ICD30. The user data written in ICD30 are read out in sequence at the prescribed timing in accordance with the segment numbers and they are input into outer encoder ICH20 and H21.

### 9. Audio Outer Encoder (AE-06 board)

As shown in Fig. 3-8-12, the audio product block is composed of the audio data, addition data and user data. On the AE-06 board, data readout from audio data memory IC28, addition data memory ICJ2 and user data memory ICD30 is controlled by ROM ICG23, G25, J20 and J22, and the data are supplied to the encoder in sequence from the outer code block at the left side of Fig. 3-8-12. The data of 8 code blocks (4 channels × 2 blocks) are input in the following sequence: CH1 (EVEN) → CH2 (E) ... CH4 (E) → CH1 (ODD) → CH2 (O) ... CH4 (O) → CH1 (E) → ...

In the case of audio editing or spot erasing, the advance playback user data written into the addition data memory are input into the encoder.

The audio outer code is a (10, 7) Reed Solomon code with 1 word equivalent to 4 bits. The Galois field generating polynominal and code generating polynominal are given below.

Galois field generating polynominal GF (16):

$$P(X) = X^4 + X^1 + X^0$$

Code generating polynominal ($\alpha = 2_H$):

$$G(X) = (X + \alpha^0)(X + \alpha^1)(X + \alpha^2)$$
$$= X^3 + \alpha^{10}X^2 + \alpha^{11}X + \alpha^3$$

The Reed Solomon code is generated by a divider composed of two PROMs, ICH20 and H21, and register ICH17.

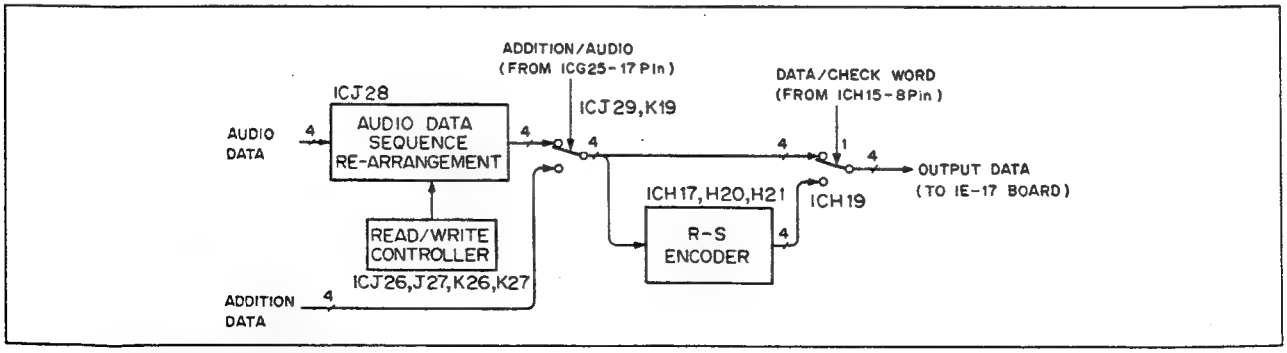



**Fig. 3-8-13. Audio Outer Encoder (AE-06 Board)**

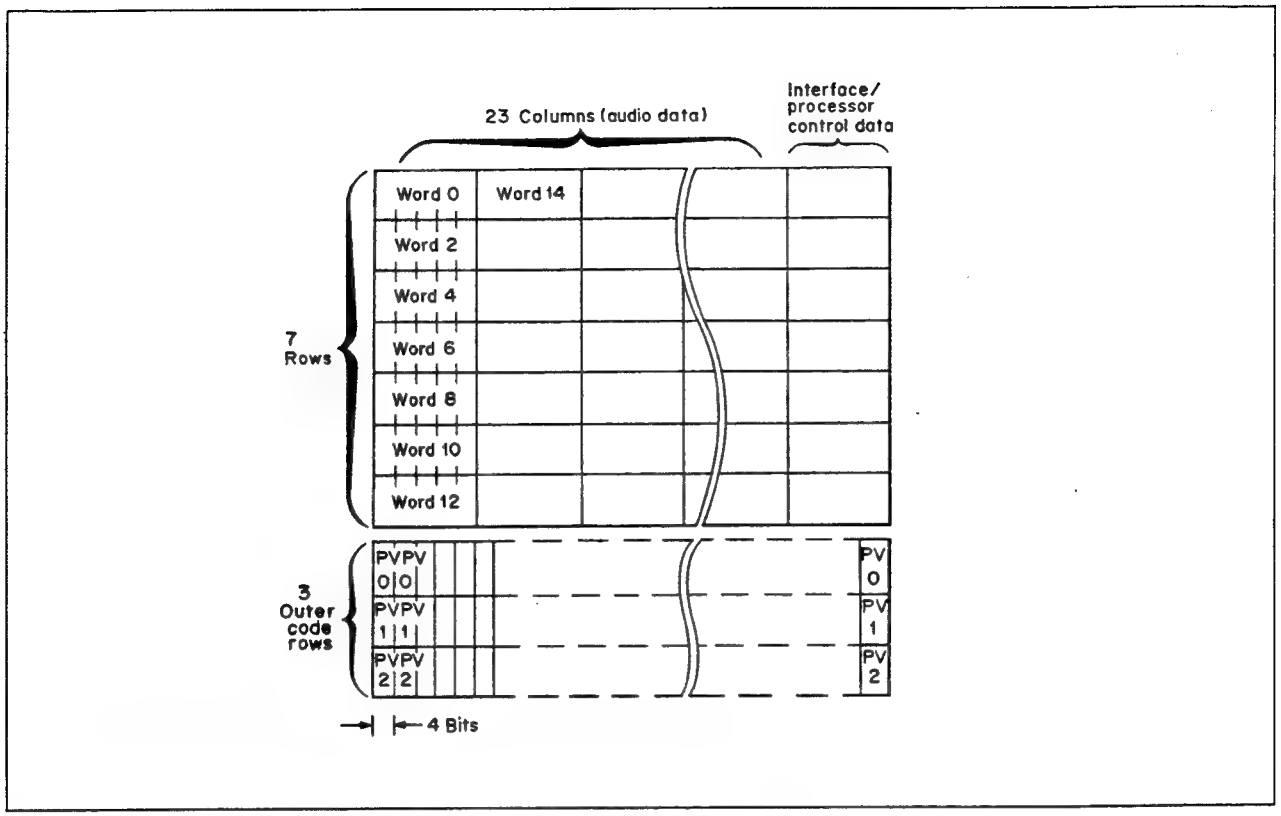



**Fig. 3-8-12. Audio Product Block Layout (Even samples/AE-06 Board)**

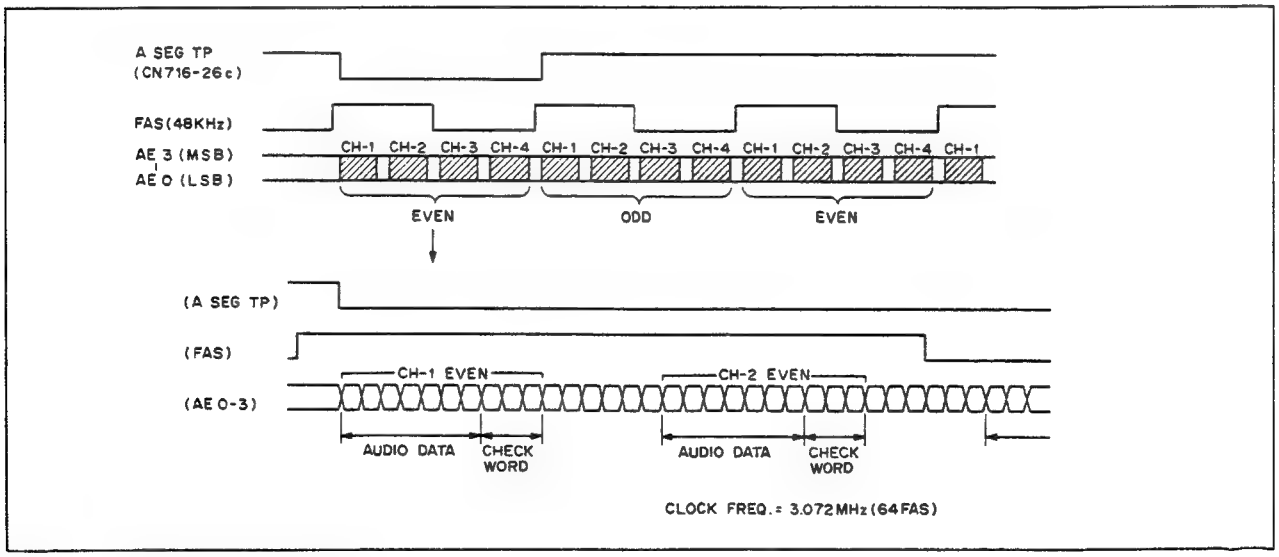



**Fig. 3-8-14. Audio Outer Encoder Output Timing (AE-06 Board)**

## 4-3-9. AP-14 Board

The AP-14 board processes the digital audio playback signals and it is composed of the following circuits.

- Addition data extractor
- Channel status data generator
- User data extractor
- Audio data time base converter
- Channel status data re-blocking

The ADVANCE head playback data and CONFI head playback data obtained by readout from the LIP-SYNC memory (frame memory) on the CI-01 board and by outer decoding are supplied to the AP-14 board alternately in outer code block units. On the AP-14 board, the CONFI and ADVANCE playback addition data are extracted from these input data, the audio data are controlled by the extracted data, and the data are returned to their original time sequence. In the case of a 525/60 system, "LEAP-FRAME" processing is also conducted on this board.

The user data in the code blocks are also extracted, and the user data in the CONFI head playback data are output externally through the IF-139 board. In addition, the user data in the ADVANCE head playback data are sent to the AE-06 board of the recording system and used when editing. Finally, the AP-14 board is also responsible for re-blocking the channel status data.

### 1. Addition Data Extractor (AP-14 board)

As shown in Fig. 3-8-12 (refer to the AE-06 board in Section 4-3-8), the audio product block is composed of the audio data, the addition data which controls the audio data, and the user data. For a detailed description of the addition data, refer to the AE-06 board in Section 4-3-8.

Before the audio data are processed, the 5 outer code blocks at the right end of the product block are supplied first in order to enable the addition data, which control these audio data, to be processed. The CONFI head playback data and ADVANCE head playback data are supplied alternately in outer code block units and for each head 5 outer code blocks each of these data are supplied from the product blocks.

(CH-1:EVEN → CH1:E → CH1:E → CH1:E → CH1:E) → (CH2:EVEN×5) → (CH3:EVEN×5) → (CH4:EVEN×5) → (CH1:ODD×5) → (CH2:ODD×5) → (CH3:ODD×5) → (CH4:ODD×5) → ...

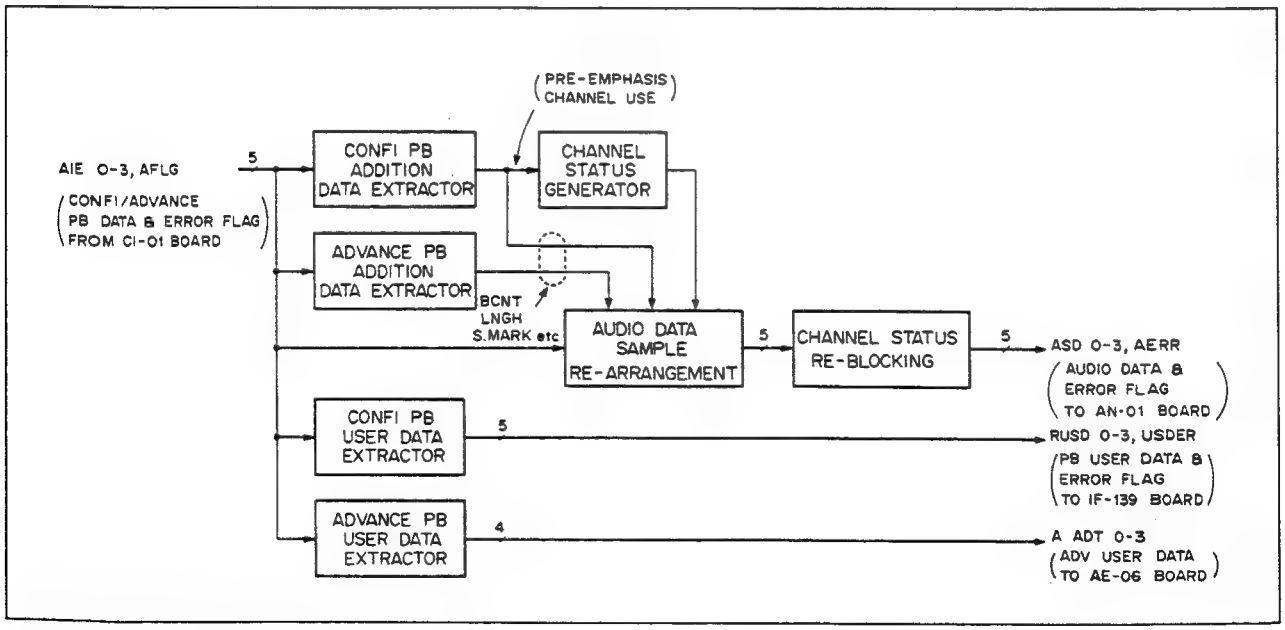



**Fig. 3-9-1. Function Diagram (AP-14 Board)**

The addition data supplied to the AP-14 board are written into memory ICG18 and K18 and the following processes are undertaken. However, "ELAP" and "SEQN" are not used with the DVPC-1000 and so they are not processed.

1. BCNT
   For each channel, this data detects the sample number in a segment from the odd sample block and even sample block "BCNT" and uses it for controlling the audio data memory.

2. CHAN
   This data is used to identify the channel use of the recorded data. It is fetched to the UPI and displayed on the control panel through the IF-139 board.

3. PREF
   This data is used to identify the pre-emphasis in the recorded data. It is fetched to the UPI and displayed on the control panel through the IF-139 board. At the same time, it is sent to the de-emphasis circuit on the AA-29 board through the UPI, IF-139 board and PG-13 board.

4. LNGH
   This data is used to identify the audio data word mode of the recorded data. It is fetched to the UPI and displayed on the control panel through the IF-139 board. Based on this data, the audio data 20 bits and ancillary data 4 bits are reconfigured on the AP-14 board.

5. SMARK0/SMARK1
   The SMARK0/SMARK1 data in the even sample block and odd sample block are decoded channel by channel, this value and the value of the sample counter in the segment are compared, the matching pulse is extracted and the AES/EBU block top is detected.

The above addition data are read out from memory ICG18 and K18 at the timing indicated in Fig. 3-9-3 for processing. The asynchronous audio status is detected from the second MSB of "BCNT." If asynchronous audio signals are input, AUDIO SYNC indicators D1 through D4 light up and at the same time warning information is output to the IF-139 board through the UPI.

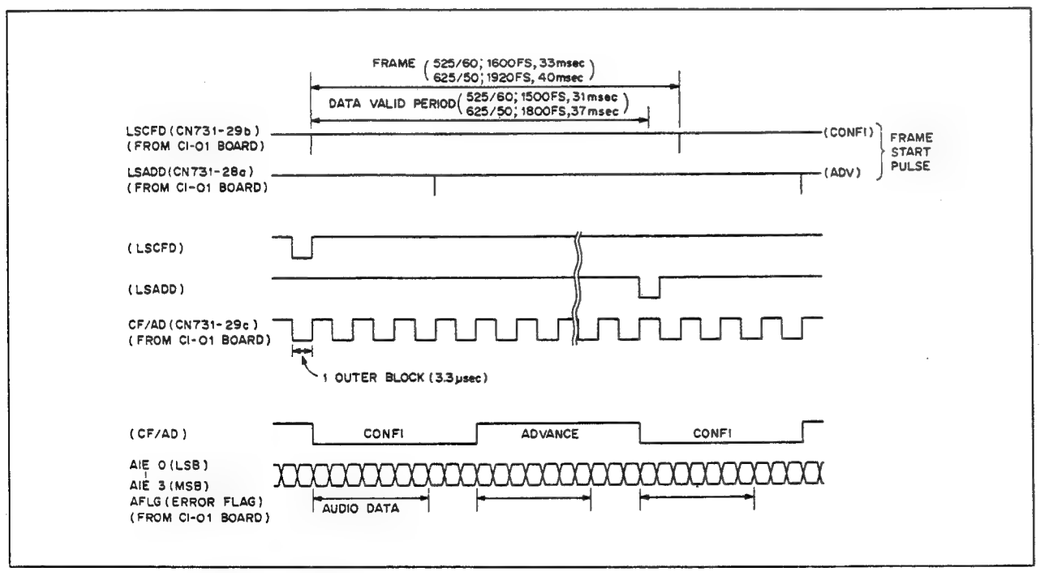



**Fig. 3-9-2. Data Input Timing (AP-14 Board)**

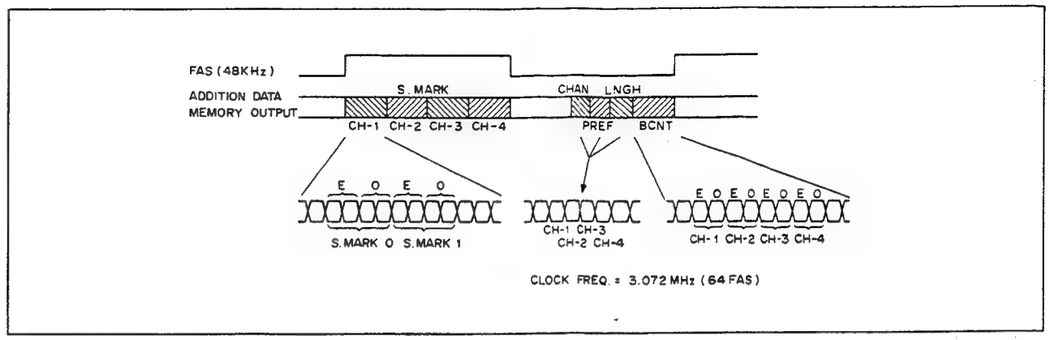



**Fig. 3-9-3. Addition Data Readout Timing (AP-14 Board)**

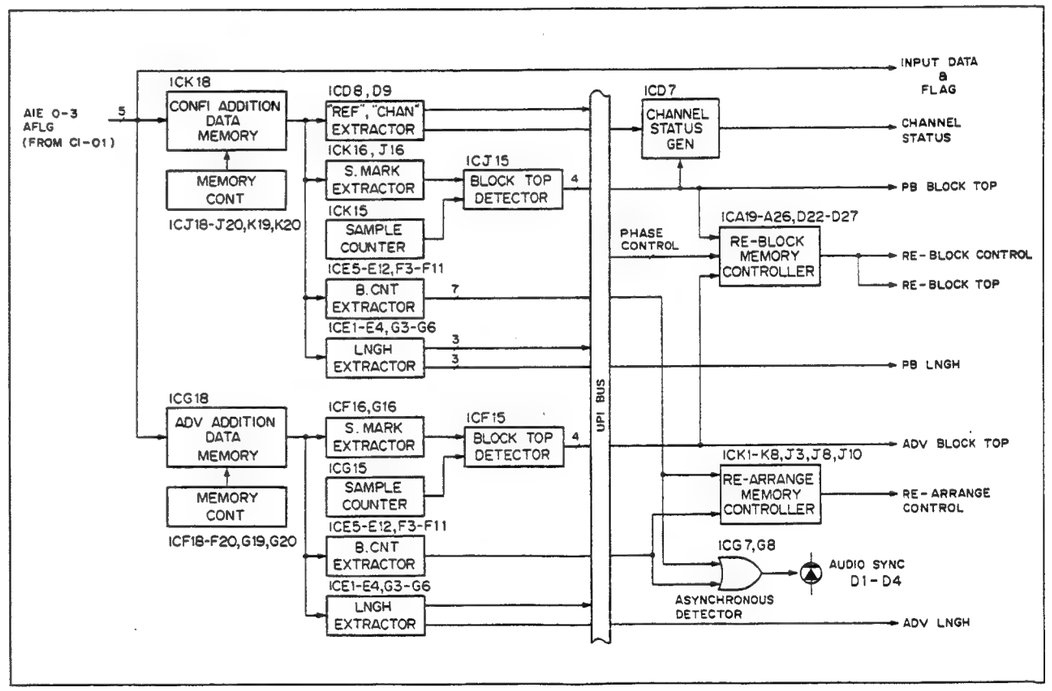



**Fig. 3-9-4. Addition Data Extractor Circuit (AP-14 Board)**

### 2. Channel Status Data Generator (AP-14 board)

When the channel status data have been recorded, the recording data are output in their original form. When the channel status data are not recorded (when "LNGH" is 19+V, 19+U or 20), the channel status data are prepared from addition data "PREF" and "CHAN", and they are output. The "PREF" data are inserted into channel status data bits 2, 3, 4/byte-0, and the "CHAN" data are inserted into bits 0, 1, 2, 3/byte-1. Furthermore, channel status data bit-0/byte-0 (PRO USE/CONSUMER USE) is set to "1", the other bits are all set to "0", and the CRCC is calculated, inserted into byte-23 and output. Along with the CONFI head output/ADVANCE head output, the channel status data are prepared from the addition data among the CONFI head playback data.
In the actual circuit, "CHAN" and "PREF" among the addition data are extracted by ICD8 and D9 and they are stored in register ICB2 through B5. At the same time, the CRCC is calculated by PROM ICD7 and stored in the registers ICC2 through C5. These data are loaded into parallel-serial converter ICA6-A13, B6-B13 and C6-C13 by the AES/EBU block top pulse which is detected from "SMARK0" and "SMARK1", and they are output as serial data.

### 3. User data extractor (AP-14 board)

The user data (UCW) in the audio product block are separated into the CONFI head playback data and ADVANCE head playback data, and they are written into memory ICG26 and J24.

1. CONFI head playback user data
The user data are written into memory ICJ24 in segment units but they are read out in frame units. Readout address counter ICK23 is cleared by the readout top pulse "RDATA TOP" which is supplied from the IF-139 board, and the data are read out in succession.

2. ADVANCE head playback user data
The user data which have been written into memory ICG26 are read out in segment units by the timing signal "AADTTP" which is supplied from the AE-06 board, and they are output to the AE-06 board. These data are used in the audio editing, spot erasing or other such mode in which the user data are not rewritten (in actual fact, the played back data are re-recorded at the original position).

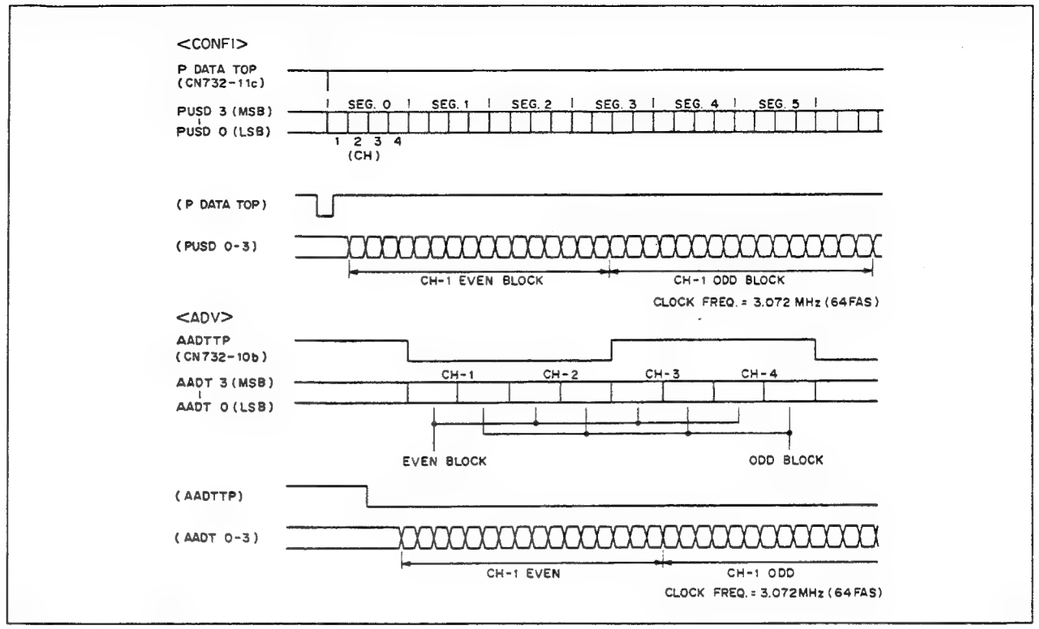



**Fig. 3-9-5. User Data Output Timing (AP-14 Board)**

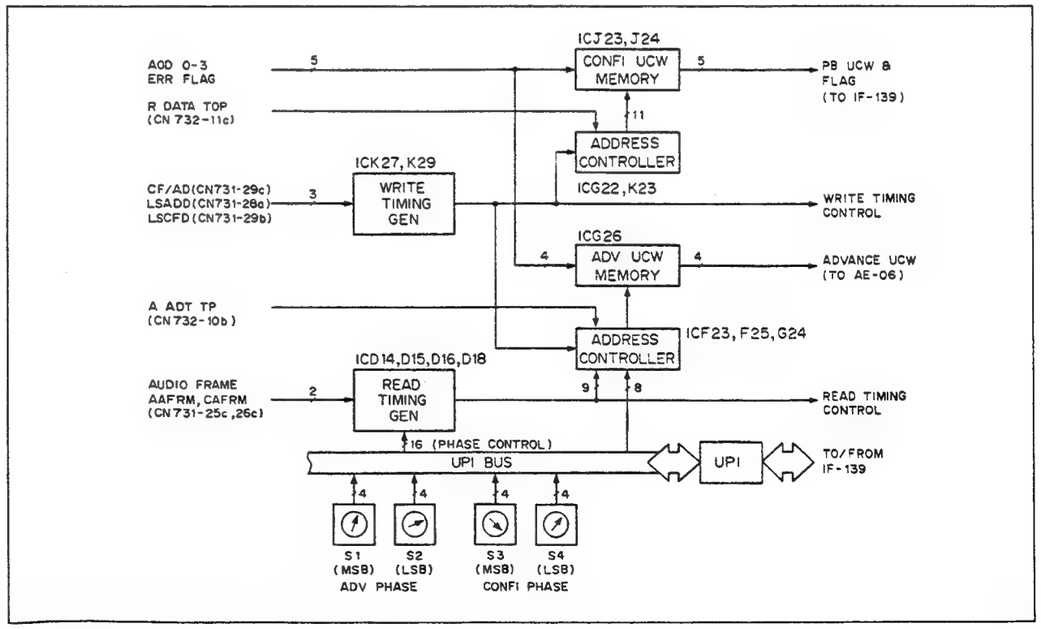



**Fig. 3-9-6. Timing Generator/User Data Generator (AP-14 Board)**

### 4. Audio Data Time Base Converter (AP-14 board)

As mentioned in "1. Addition Data Extractor", the CONFI head playback data and ADVANCE head playback data are supplied alternately in outer code block units to the AP-14 board. With each respective head, the data in 5 outer blocks are input from the product blocks in the sequence of CH1:EVEN → CH1:ODD ... → CH4:ODD. This is because the audio data of a sample (20 bits) is divided into 5 outer code blocks, and these 5 blocks are composed of data equivalent to 7 samples. After they have been supplied to the AP-14 board, the audio data are written into memory ICK12. As indicated in Fig. 3-9-7, the CONFI head playback data and ADVANCE head playback data are read out alternately from the memory in sample units.

In ICG12, the least significant 4 bits of the audio data 20 bits are converted in accordance with "LNGH" (audio data word mode) extracted from the addition data, and the audio data and ancillary data are prepared. "0" is inserted into any of the unrecorded bits among the "U" and "V" bits of the ancillary data and audio data and when the "C" bit is not recorded, the channel status data generated from the addition data is inserted.

Furthermore, this memory also exercises control so that even tapes with asynchronous audio signals recorded (such signals are not recorded with the DVR-1000/DVPC-1000) are played back at the 48 kHz frequency synchronized with the reference signal. In actual fact, the sample number applying during readout is kept constant regardless of the sample number applying when the data are written into the memory. In other words, when the sample number is low during data writing, the last sample is repeatedly read and when many samples have been written, the last samples are not read. The write sample number is obtained by decoding "BCNT" among the addition data. On the other hand, the read sample number is 320 samples/segment with a 625/50 system and 320 samples/segment or 321 samples/segment referenced to 5 frame pulses with a 525/60 system. Based on these two types of information, the read addresses in the memory are controlled.

In the case of synchronous audio signals, the write sample number and read sample number always tally, and "LEAP FRAME" processing for the 525/60 system is conducted by this circuit.

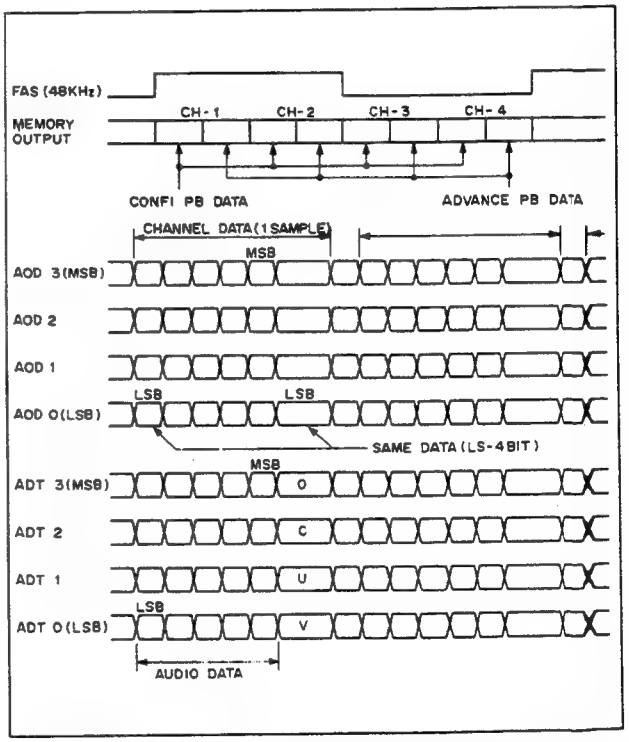



**Fig. 3-9-7. Audio Data Time Base Conversion (AP-14 Board)**

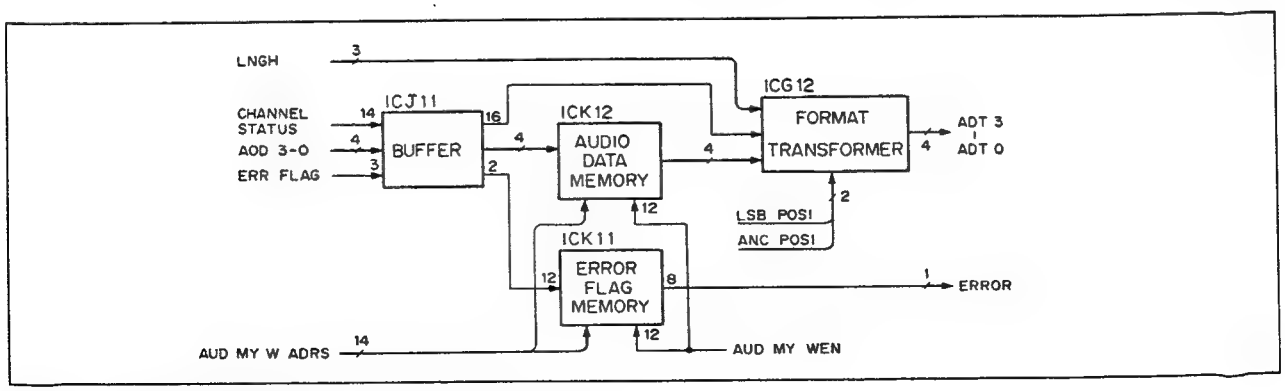



**Fig. 3-9-8. Audio Data Time Base Converter (AP-14 Board)**

### 5. Channel Status Data Re-blocking Circuit (AP-14 board)

As shown in Fig. 3-9-9, the block phase of the recorded audio data and the block phase of the input data always differ which means that when editing, switching or other such processing is conducted, discontinuity will arise in the AES/EBU block structure.

When this kind of discontinuity has arisen, a choice between two modes can be made for the DVPC-1000: in one the mode the channel status data are output in their original form and in the other mode (re-blocking) the discontinuous blocks are removed and the AES/EBU block continuity is preserved. The modes are selected using the controls on the control panel of the DVR-1000.

In the re-blocking mode, the circuit configuration is such that phase is defined by the "REF BLK" reference signal and the blocks are made continuous. At present, however, the reference signal is not supplied and so re-blocking is undertaken without defining the phase. In actual fact, a method is used by which the channel status data are written into memory ICC24 and only those individual blocks whose writing has been completed properly are read out.

A delay equivalent to 1 frame must be guaranteed at the VTR input/output for the audio data and so these data are output to the prescribed position regardless of re-blocking. This means that when re-blocking has been undertaken, the relationship existing between the audio data and channel status data at the time of their input is not maintained.

As a result of this, a time difference will arise if re-blocking is undertaken when the time code data among the channel status data or other such time data are used. When the data are output in the 2-channel mode (including the stereo mode), they are output with the block phase of subframe B aligned with the block phase of the data which are output to subframe A. However, when the data have not been recorded in the 2-channel mode, the block phases of subframes A and B will already be aligned and so the data are output without further processing.

The above processes concern the digital output data. Since, however, the ADVANCE head playback data which are supplied to the AU-86 board via the AN-01 board must be supplied without the played back data being processed, the information of the original phases which are unrelated to the re-blocking is required. This is why the channel status data and the block top information for digital output as well as the channel status data and the block top information supplied to the AU-86 board are output. This is shown in Fig. 3-9-11.

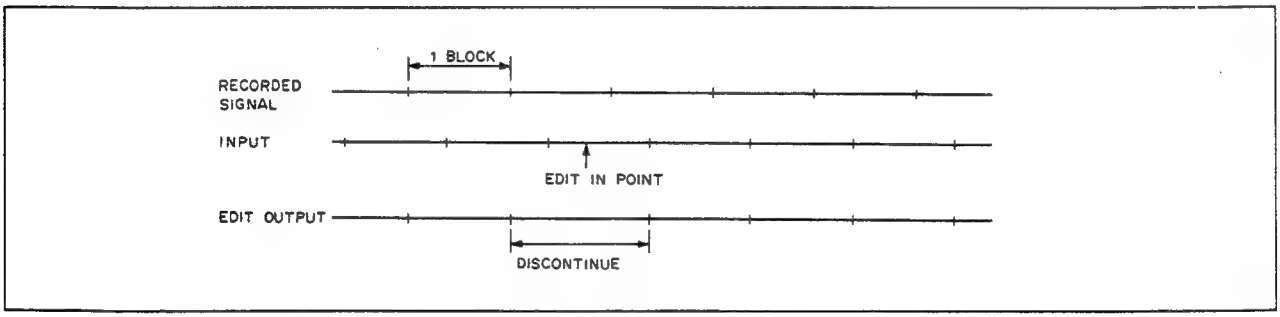



**Fig. 3-9-9. Discontinuity in AES/EBU Block Structure (AP-14 Board)**

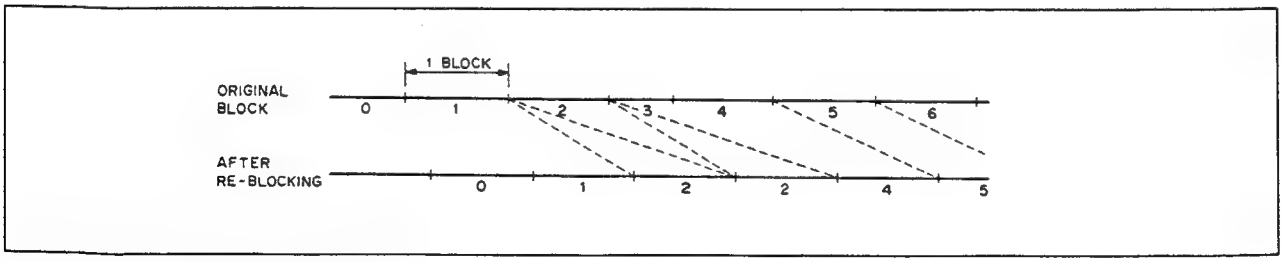



**Fig. 3-9-10. Re-blocking (AP-14 Board)**

When it comes to playback using the CONFI head, the return data which are supplied to the AU-86 board do not exist and only the one type of ancillary data are sent to the next slot of the audio 20 bits. Two types of ancillary data are sent for the ADVANCE head playback data.

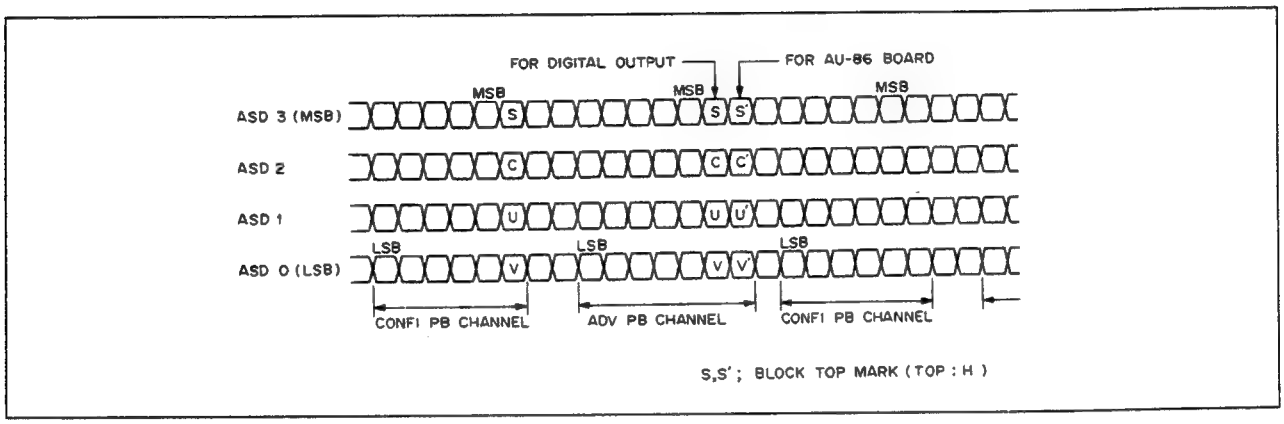



**Fig. 3-9-11. Output Data Format (AP-14 Board)**

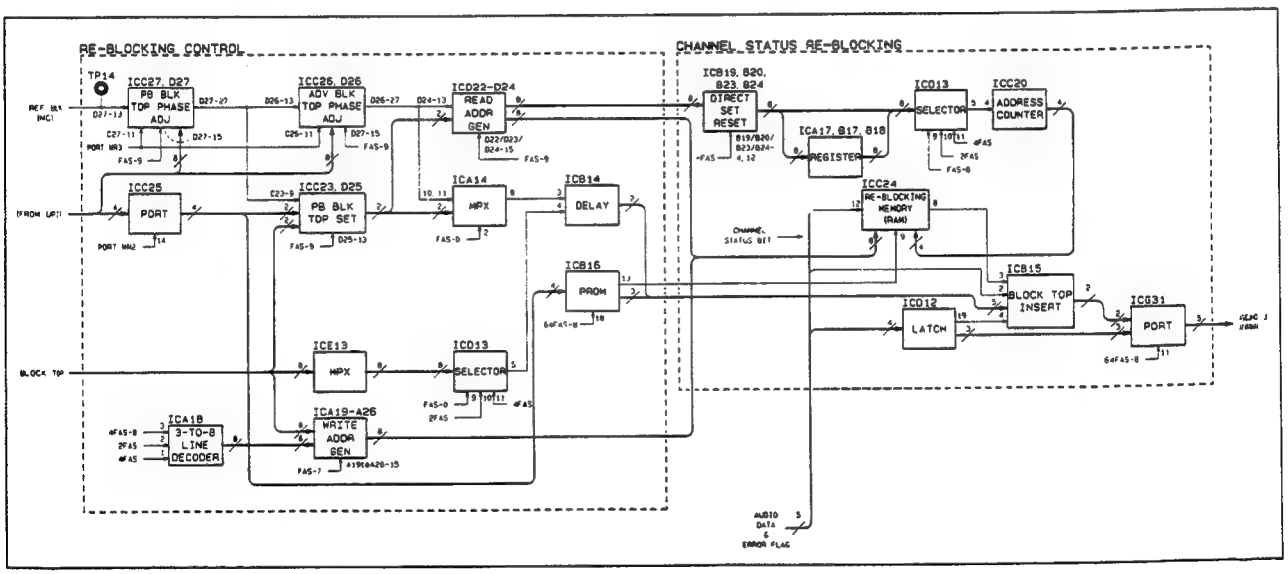



**Fig. 3-9-12. Channel Status Data Re-blocking Circuit (AP-14 Board)**

## 4-3-10. AN-01 Board

The AN-01 board is responsible for the final processing of the playback system digital audio signals, and it is composed of the following circuits.

- Audio error concealment circuit
- Muting circuit
- Advance return data output circuit
- Level controller
- Peak level detector
- Output channel selector
- Output mode setting circuit
- AES/EBU encoder

Audio data for a total of 8 channels composed of the CONFI head playback data CH-1/2/3/4 and the ADVANCE head playback data CH-1/2/3/4 are supplied to the AN-01 board from the AP-14 board. The test bypass data are also supplied from the AU-86 board.

On the AN-01 board, the audio data supplied in 4-bit parallel format are converted into serial data and the data for all 8 channels are processed by time division multiplexing. The data processing rate is 256fs (12.288 MHz). The processing after the output channel selector is done for each channel individually. The following audio signals are output from the AN-01 board.

The CONFI head playback audio data are output to the PG-13 board. This signal is D/A converted on the AA-29 board and output externally from the ANALOG AUDIO OUTPUT connector.

The CONFI head playback audio data which have been encoded in the AES/EBU format are output to the IV-14 (or IV-21) board. This signal is output externally via the DIGITAL AUDIO OUTPUT-1/2 connectors. Once the ADVANCE head playback audio data have been encoded in the AES/EBU format inside the AN-01 board and their delay has been adjusted, they are output externally through the ADVANCE AUDIO OUTPUT connector.

The AN-01 board may have the board number suffix of "−11" or "−12." For the two boards the configuration of the circuitry is partially different and the following description applies to a board with the "−11" suffix. The changes affecting the boards with the "−11" and "−12" suffixes are listed below. For details of the circuits in which these changes have been adopted, reference should be made to the description of the respective circuits.

- Change in audio error concealment method
- Change in the audio level control range
- Change in the audio level controller

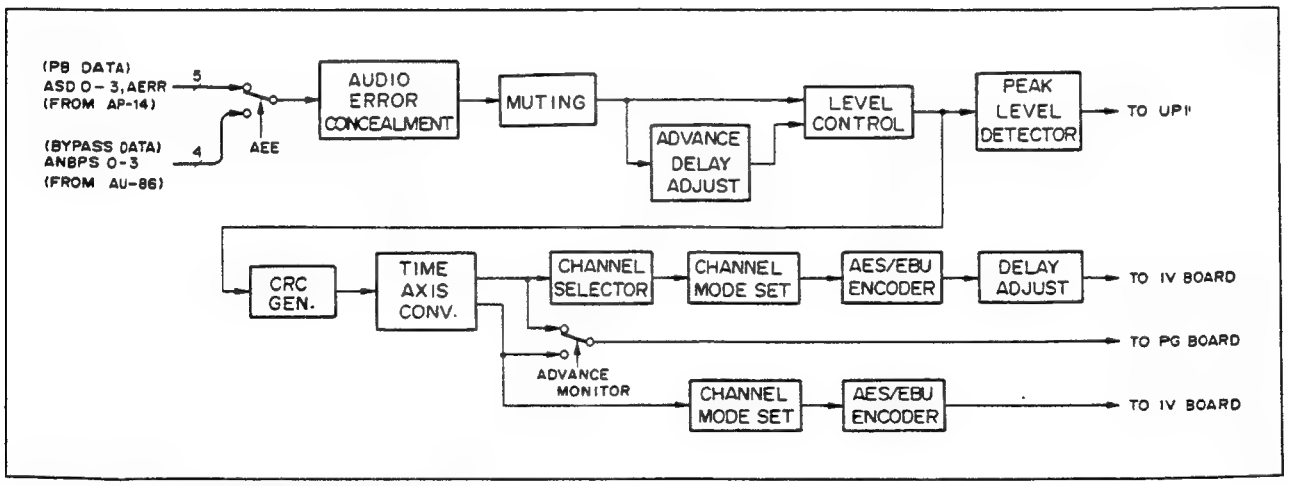



**Fig. 3-10-1. Function Diagram (AN-01 Board)**

### 1. Input Data Format and Serial-Parallel Converter (AN-01 board)

The "ASD0-ASD3" 4-bit audio data and the "AERR" error flag from the AP-14 board are supplied to the AN-01 board. The CONFI head playback data and ADVANCE head playback data are time-division-multiplexed, as shown in Fig. 3-10-2, and then input.
The "ANBPS0-ANBPS3" test bypass signals are supplied from the AU-86 board of the recording system.
The 4-bit parallel input audio data are converted into LSB first serial data by ICJ24.
T1, C1, U1 and V1 are supplied to the ancillary data in the CONFI head playback data section. Two types of ancillary data are supplied in the ADVANCE head playback data section: T1, C1, U1 and V1 are used for digital output, and T2, C2, U2 and V2 are used for advance return output.

### 2. Audio Concealment Circuit (AN-01 board)

Errors in the audio data are corrected on the CI-01 board. For data whose errors cannot be corrected, the "AERR" error flag is raised and supplied to the AN-01 board.
Based on the error flag, the concealment circuit provides interpolation for the error data. If there is no error in the samples before or after the error data, these are used for interpolation. If interpolation is not possible because of errors present in the such data, pre-hold applies and the error-free data of the previous one or more samples are output in their original form. If the pre-hold state continues, the audio data are muted.

**(1) Error flag selection**
The "AERR" error flag is raised for data whose errors cannot be corrected on the CI-01 board. When the "V" (validity) flag has been raised in the input data, it means that these data have been flagged as "error data." Two different types of error flag are used in this circuit to assign two different concealment modes:

- E + V mode
  Concealment of samples flagged by "AERR" or "V"
- E mode
  Concealment of samples flagged by "AERR" only

A control on the DVR-1000 control panel determines which of these modes is to be used. The mode information "CFLG SL0/1" is supplied via the UPI of the AN-01 board to pins 12 (MD0) and 19 (MD1) of error flag selector ICH23.



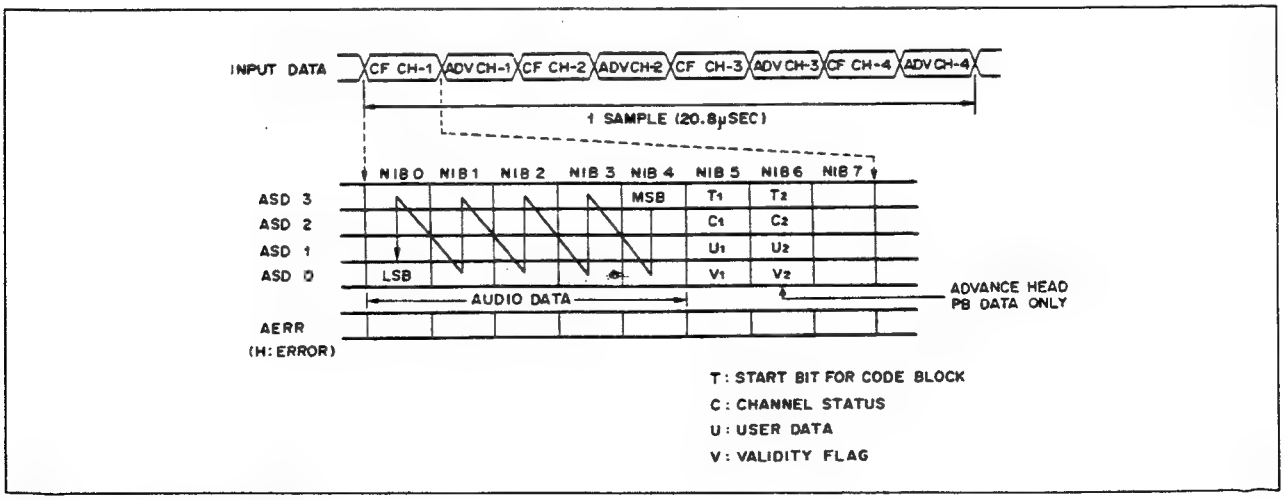



**Fig. 3-10-2. Input Data Format (AN-01 Board)**

**(2) Circuit configuration**

A block diagram of the concealment circuit is shown in Fig. 3-10-3.

The data required to generate the interpolation data are provided in delay circuit ICJ22.

The interpolation data generator is composed of adder ICH18 and F17, multiplier ICG14, G16 and H17, and their peripheral circuits, and it generates the interpolation data from the data of the 3 samples before and after the error data. Error flag judgement circuit ICH13-H15 and J13-J16 detect whether interpolation is possible or not, and its information is supplied to the interpolation data generator.

The output data of the concealment circuit are held in hold data register ICJ18 and when interpolation is not possible, these data are selected by output data selector ICF16 and output.

The through data (input data), interpolation data and hold data are supplied to output data selector ICF16 and the output data are selected in accordance with the 3-bit data supplied from the error flag judgement circuit. At the same time, the "U," "C" and "T" data among the input data are added to the prescribed time slot, and the "V" flag is set to "1" (error data) for the interpolated or held data and output.

The above description applies to AN-01 boards provided with the "−11" board number suffix. Whereas on this board the interpolation data are generated from the data of 3 samples before and after the error data, the board with the "−12" suffix features simple average interpolation which uses 1 sample before and after. As a result, the error flag judgement circuit has also been simplified. The other circuits have virtually identical configurations.

**3. Muting Circuit (AN-01 board)**

This muting circuit employs digital data. It is activated when the DVPC-1000 has been set to any one of the 4 modes listed below and when error data have occurred continuously for 16 or more samples.

The muting is released once there are 256 samples of continuous error-free data. Fade IN and fade OUT during muting ON/OFF are both performed at the time which corresponds to 128 samples.

(1) When the PLL circuit on the TG-28 is unlocked

(2) When the muting command has been output from the IF-139 board (for instance, during DVR-1000 mode switching or shuttle playback)

(3) When the muting is forcibly selected at the control panel

(4) When error data (pre-hold) are continuous

Fig. 3-10-4 is a block diagram of the muting circuit. "CEAL FLG" in the diagram is the flag indicating the hold status which is output from the audio concealment circuit in the previous stage. "MUTE OFF" is the flag for releasing forced muting which is only valid in the test mode. "MUTE FS" is the forced muting flag which is input channel by channel from the control panel. "MT CMD" and MUTE" are the forced mute flags provided by the IF-139 board and TG-28 board respectively. A sequence of priority governs these muting flags.

The number of continuously occurring error data is counted by INVALID data counter ICB22, B23 and B24. When error data equivalent to 16 samples have been generated continuously, the mute start pulse (low: MUTE ON) is output from

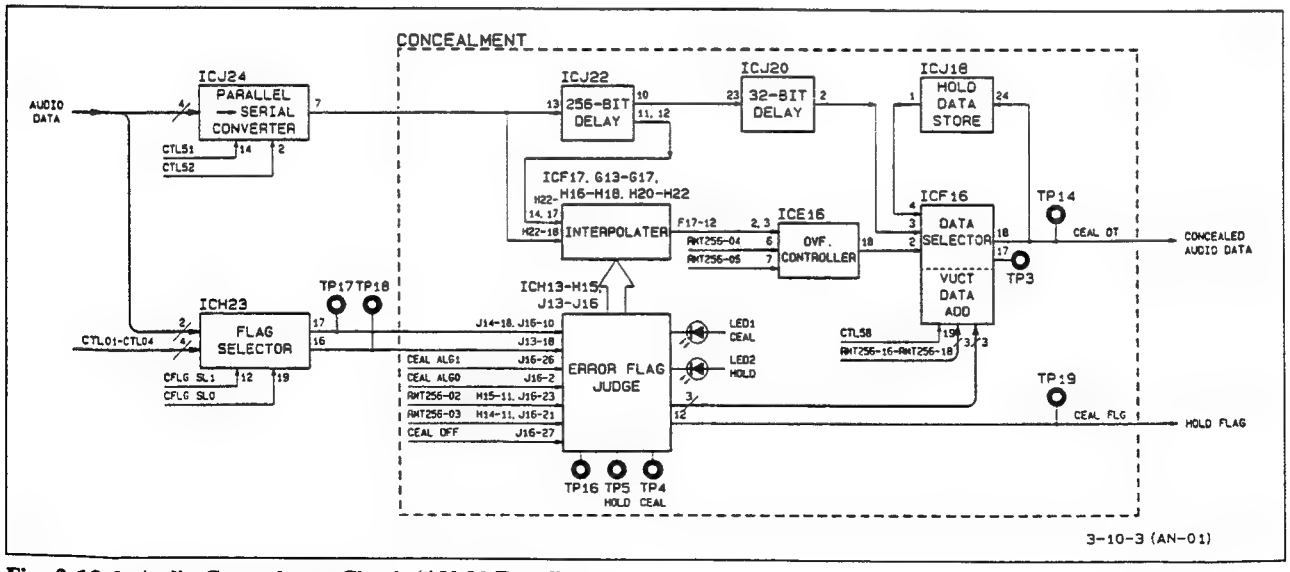



**Fig. 3-10-3. Audio Concealment Circuit (AN-01 Board)**

ICB24 pin 9. Flip-flop ICC20 and C21 indicating the muting status is set by this mute start pulse. The error-free data are counted by VALID data counter ICC22, C23, C24 and D25 and when such data equivalent to 256 samples occur continuously, the mute release pulse is output from ICD25 pin 8 to reset flip-flop ICC20 and C21 which indicates the muting status. Based on the muting period signal output from ICC20 and C21, muting slope counter ICB19, B20 and B21 is activated and it generates the slope for fade IN/OUT during muting. Coefficient generator ROM ICB17 generates the coefficient for providing the actual fade IN/OUT slope, and this coefficient is supplied to multiplier ICC17.

On an AN-01 board with a "−12" board number suffix, PROM ICB17 for generating the coefficient is removed, and the multiplier is provided with the slope counter output as the multiplication coefficient.

MUTE TIME counter ICC19, C20 and C21 is installed in order to secure the minimum muting time so that the muting will not be released immediately after operation has entered the muting mode. S2 serves to set the minimum muting time and at present it has been set to "7." The minimum muting time in this case is approximately 683 msec.

After the audio data leave the multiplier, the "V," "U," "C" and "T" bits are added to the prescribed slots and output by ICB16 and C16.

Finally, delay circuit ICC14 and C15 serve to delay the audio data output from the concealment circuit by 192 samples, after which the data enter this circuit.



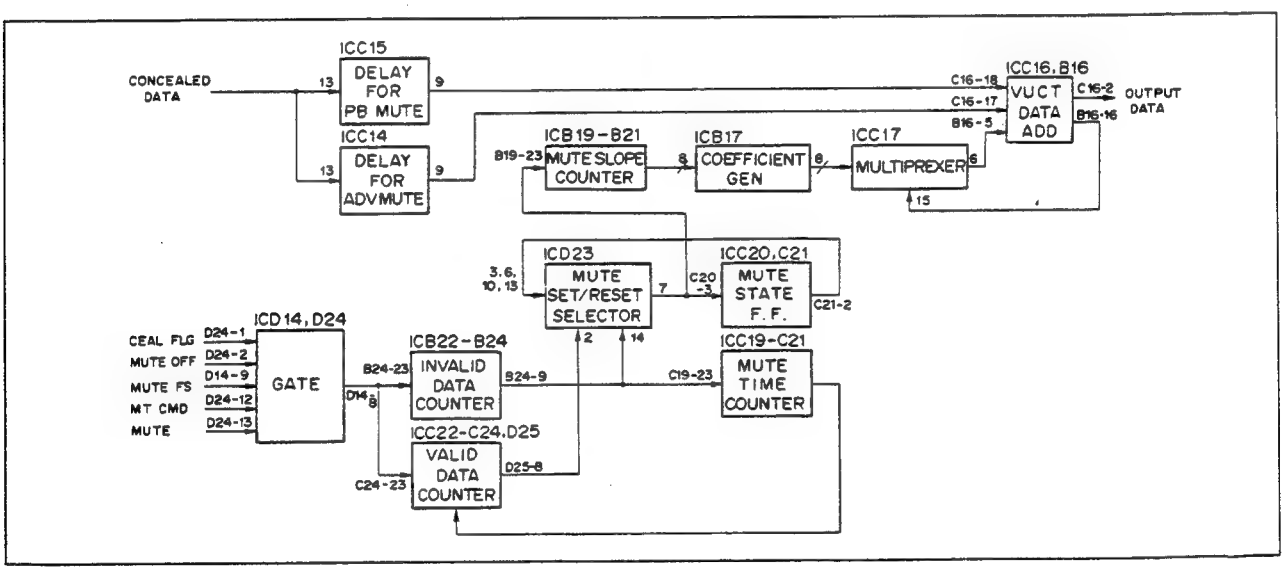



**Fig. 3-10-4. Muting Circuit (AN-01 Board)**

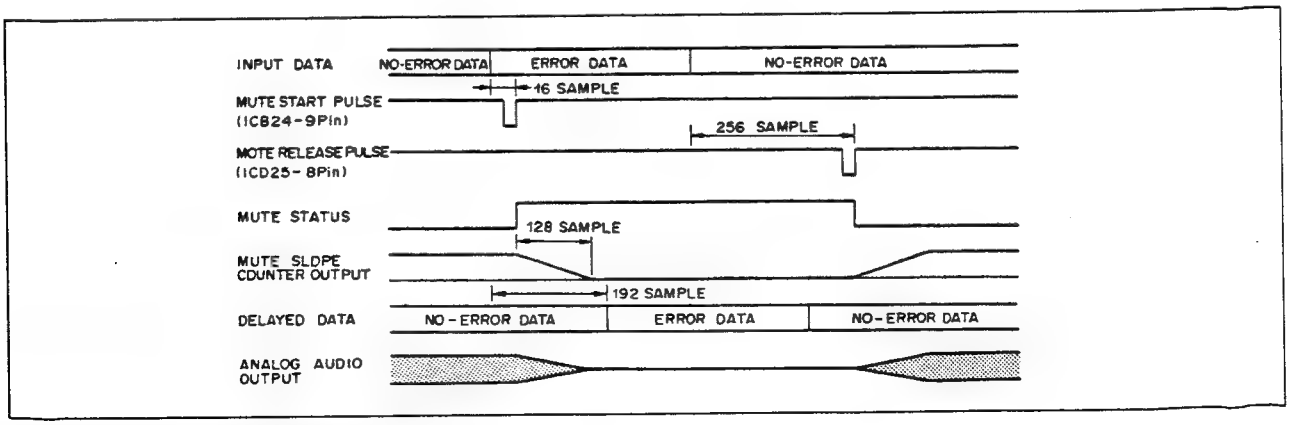



**Fig. 3-10-5. Muting Circuit Timing Chart (AN-01 Board)**

### 4. Advance Return Data Output Circuit (AN-01 board)

After concealment, the ADVANCE head playback data are fed back to the AU-86 board of the recording system along a separate path from the main signal line. These data are known as the advance return data, and they are used for sound-on-sound and other editing operations between the audio channels. The advance return data output circuit serves to provide delay adjustment so that the advance return data phase will match the phase in the recording system and data formatting. The delay circuit is composed of memory ICH4 and counter ICJ4. The amount of delay can be set in 1-sample units by S8 and S9 and at present both S8 and S9 are set to "F." The amount of delay applying with this setting is 256 samples. ICG8, G11 and J17 provide very fine phase alignment within a sample and align the phases of the "V," "U," "C" and "T" bits.

### 5. Advance Data Delay Circuit (AN-01 board)

When the ADVANCE AUDIO OUTPUT connector output is input again for editing after it has been processed by an external unit such as a digital mixer which is attended by a delay, the advance data phase must be controlled in accordance with the external delay. This circuit is designed to set this delay.
The delay circuit is composed of memory ICH2 and counter ICJ2. The delay amount is set by a control on the DVR-1000 control panel and the relevant information is supplied to this circuit via the UPI. When the DVPC-1000 is in the local mode, the delay is set by S6 and S7. When both S7 and S6 are set to "$C7_H$," the advance delay is equivalent to a sample number of 0.

### 6. Level Controller (AN-01 board)

In the level controller, the 20-bit audio data output from the muting circuit are multiplied by the 16-bit multiplication coefficient supplied from the UPI, and their output level is varied across a range from +6 dB to −∞. The most significant 20 bits are taken out as the output data and the lower bits are discarded. Separate multipliers are used for the CONFI head playback data and ADVANCE head playback data and each provides processing for 4 channels by means of time division. Multiplication is done by providing the 2's complement code audio data with the straight binary code coefficient. The multiplication coefficient supplied from the UPI passes through ICG7, it is converted into parallel data by shift register ICH8 and J8, and then supplied to the multipliers. This data is fetched to the UPI via ICH7 and J21, and the UPI controls the coefficient data so that the output level will change smoothly.
Before entering the multipliers, the sign bit (MSB) of the audio data is held by ICG8 and input. ICG9 and G10 detect changes in the sign bit after multiplication and they provide overflow/underflow processing. They also add and output the "V," "U," "C" and "T" bits in the input data to the designated slots of the output data.
On an AN-01 board with a board number suffix of "−12," the variable level range can be selected to either +6 dB to −∞ or +12 dB to −∞ by means of jumper plug JP4. When JP4 is shorted, the range is set to +6 dB to −∞; when it is left open, it is set to +12 dB to −∞.

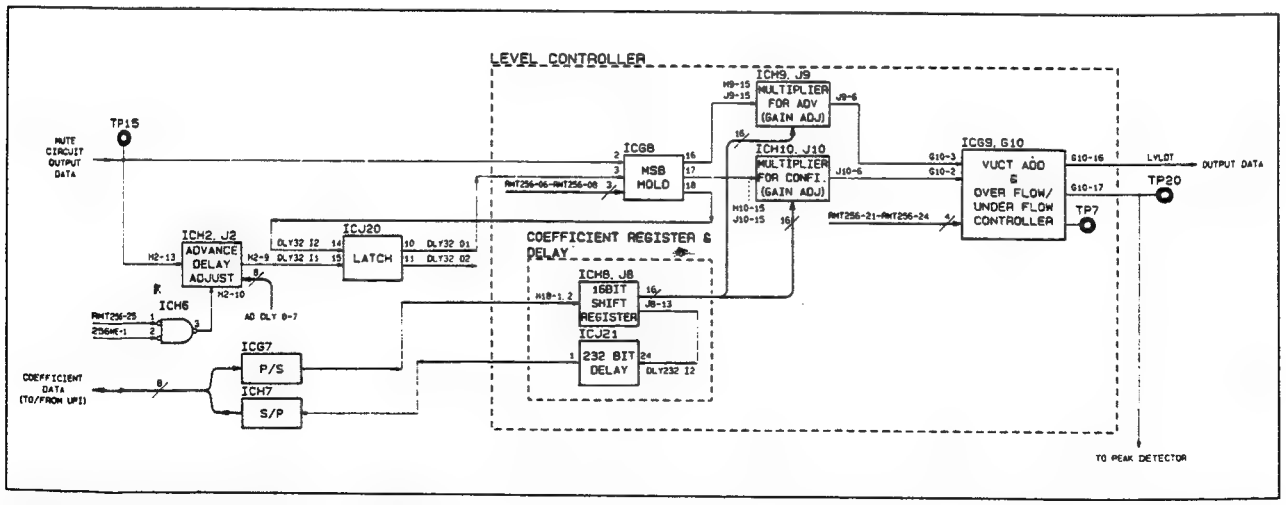



**Fig. 3-10-6. Level Controller (AN-01 Board)**

When the multiplication coefficient supplied to the multipliers has changed suddenly, the gain in the output level will also change suddenly, and this causes noise. For this reason, the coefficient must be changed smoothly, and on a board with a "−11" number suffix this is controlled by the UPI software. On a board with the "−12" suffix, this part is configured by the hardware and controlled to produce a change of 1 level per sample (1 level is equivalent to 1 LSB of the multiplication coefficient).

### 7. Peak Level Detector (AN-01 board)

This circuit serves to detect the peak level in the playback system and it processes the data for 8 channels by means of time division.
The "INILV SET" initial value setting command is supplied from the UPI and the input data ("A" in the figure) at this timing serve as the initial peak value. Subsequently, the current peak level ("B" in the figure) and the input data absolute value are compared, the higher of the two levels is selected and the peak value is updated. Immediately before the "INILV SET" command is supplied, the serial peak value is converted into a parallel value and then output to the UPI.
The data A and B magnitude is detected by means of both the MSB provided after the two levels have been added and subtracted and the MSB of data A and data B. The data are a 2's complement binary code.

| A | B | A+B | A − B |
|---|---|---|---|
| 1 | 1 | 1 | 1 ; A > B<br>0 ; A < B |
| 1 | 0 | 1 ; A > B<br>0 ; A < B | 1 |
| 0 | 1 | 1 ; A < B<br>0 ; A > B | 0 |
| 0 | 0 | 0 | 1 ; A < B<br>0 ; A > B |

0 ; NEGATIVE
1 ; POSITIVE

**Table 3-10-1. Peak Level Detection (AN-01 Board)**

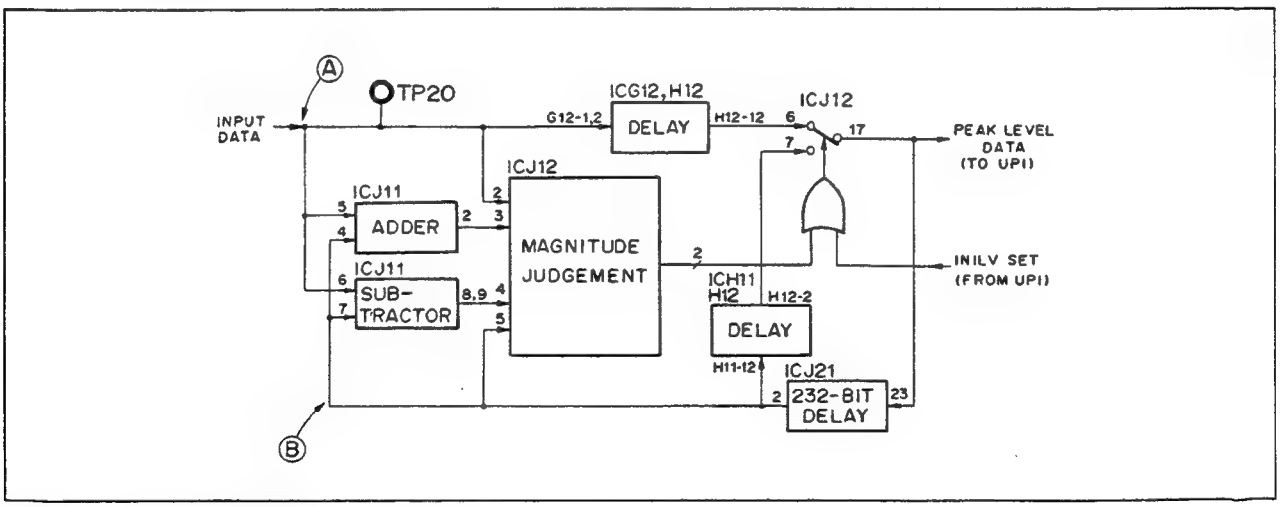



**Fig. 3-10-7. Peak Level Detector (AN-01 Board)**

## 8. Data Format Converter (AN-01 board)

The 8-channel data are processed by time division from the above-mentioned concealment circuit as far as the peak level detector. However, the data need to be processed by individual channel in the subsequent blocks and so their format is converted as shown in Fig. 3-10-8.

The data rate applying after the data format conversion is 64fs and this corresponds to the rate for the AN-01 board output data. Furthermore, after conversion the same data are output twice within the 1-sample time so that they will correspond to the AES/EBU format stereo mode.

The format converter is configured by the shift registers and data selector. The two blocks configured by ICD12, E11, E12 and F11 and by ICD10, E10, F10 and F12 operate in a complementary way by performing read/write operations alternately in each 1-sample time.

Figs. 3-6-8 and 3-10-10 outline the conversion operation. The block at the left-hand side of Fig. 3-10-10 operates in the write mode while that on the right-hand side operates in the read mode.

For data writing, 8 shift registers are connected in series and the data (256 bits) of 8 channels are written in sequence. When writing is completed and the read mode is established, the registers are isolated, the data are output by the 64fs clock while at the same time the output data are returned to each register, and the same data read out twice within the same sample time.

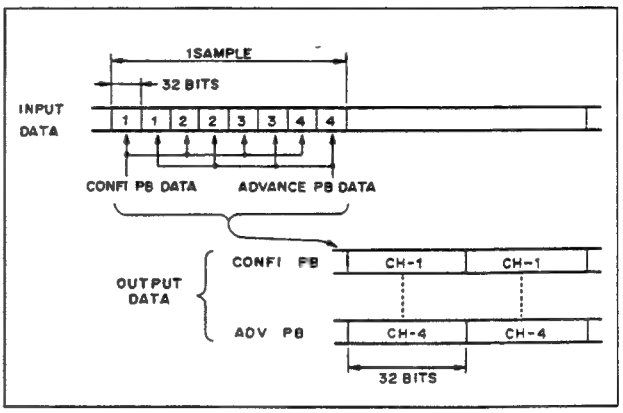



**Fig. 3-10-8. Data Format Conversion (AN-01 Board)**

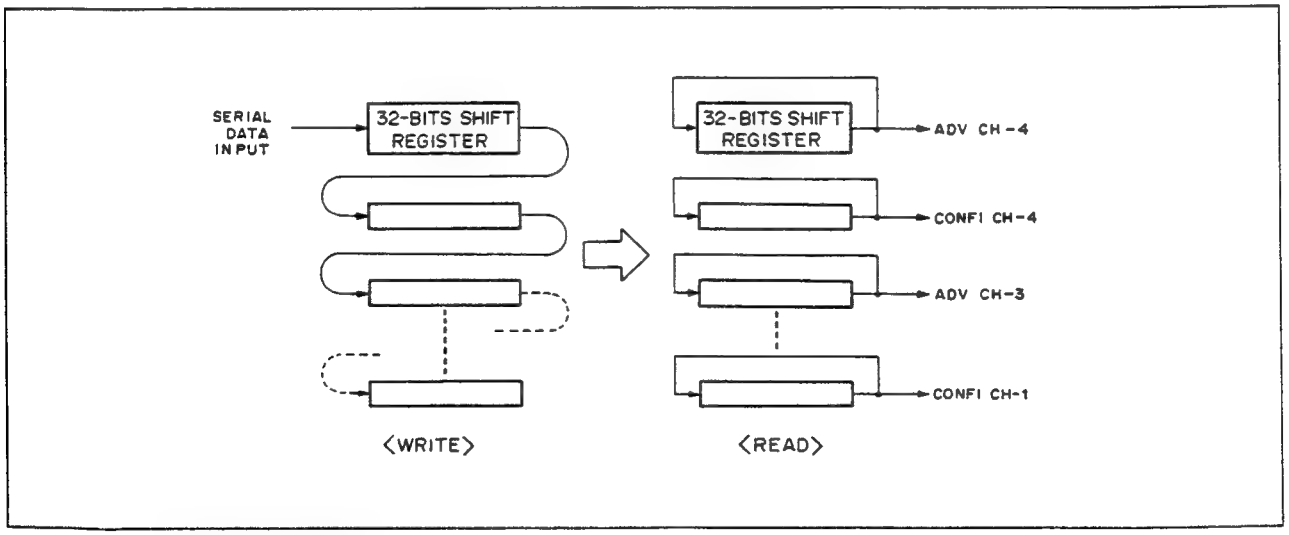



**Fig. 3-10-9. Write/Read Operation (AN-01 Board)**

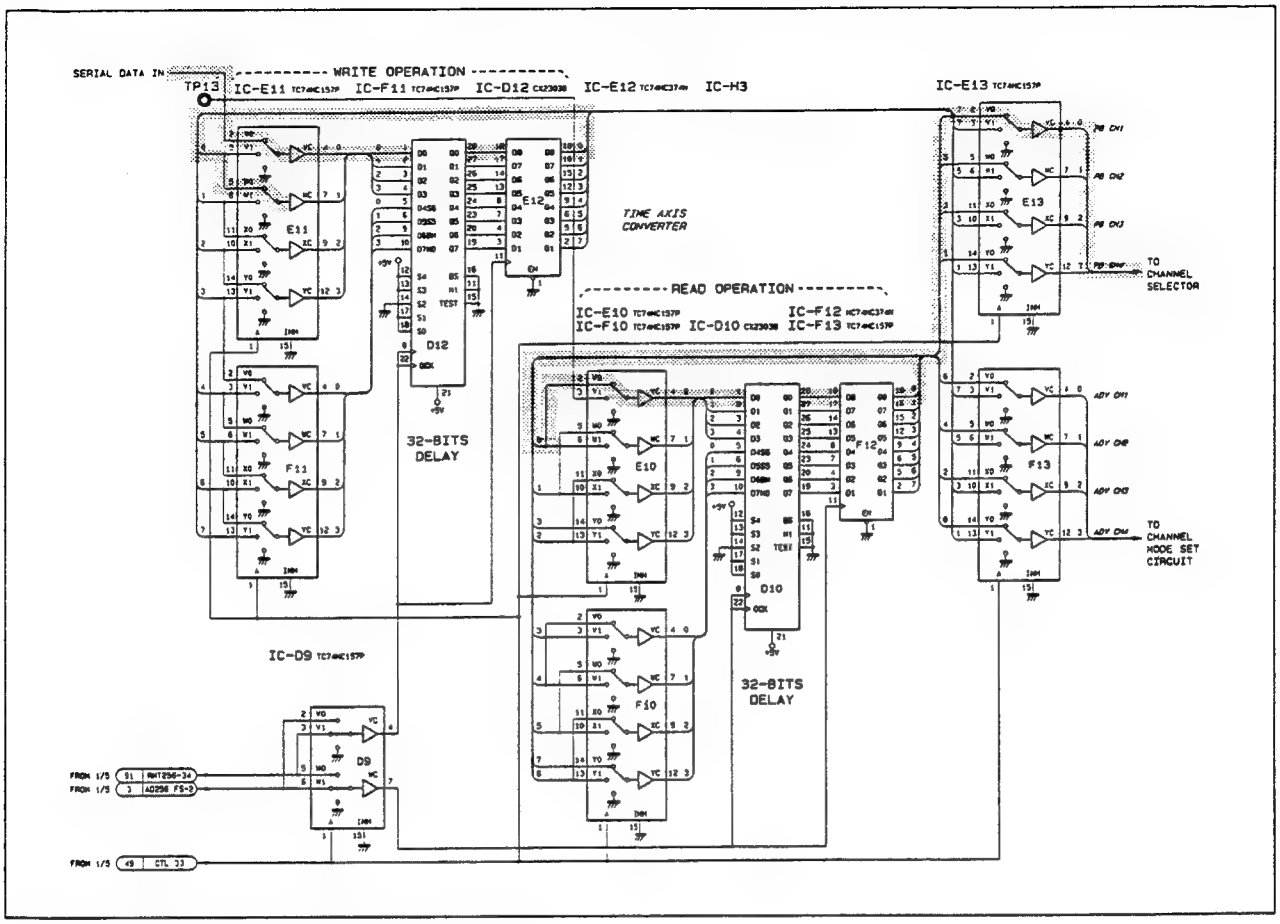



**Fig. 3-10-10. Data Format Converter (AN-01 Board)**

### 9. CRC Generator (AN-01 board)

After they have been converted to the AES/EBU format, the data are output from the AN-01 board. For each channel, the stereo/monophonic mode is set and output. As shown in Table 3-10-2, the channel mode is indicated in bits 0, 1, 2 and 3/byte-1 of the channel status data.

When the output data channel mode is set, bits 0, 1, 2 and 3/byte-1 of the channel status data among the playback data must be converted in accordance with that mode. At the same time, the byte-23 cyclic redundancy check (CRC) data must be re-calculated and added. The 8-channel CRC calculation is processed here using time division.

The changes in the channel mode bits and in the CRC data are divided into the following two stages.

(1) When the playback data have received the four mode settings shown in Table 3-10-2, the channel mode bits and the CRC needing to be changed are calculated for each mode and the results are stored in a vacant time slot.

(2) The data are read out from the time slot corresponding to the output channel mode which has actually been set, and they are exclusively OR-ed with the original channel status data to form the channel status data of the output data.

In this circuit, step (1) is processed. Step (2) is processed in the channel mode setting circuit (see 10.) at the next stage.

One example is shown in Fig. 3-10-11 which shows the CRC output and changes in the channel mode bits for each mode setting when the playback data are in the 2-channel mode and their CRC is "CRC A." In this context, CRC (0011) signifies the CRC which corresponds to the "0011" bit change.

Fig. 3-10-12 shows the time slots which store the CRC data and changed bits produced by the calculation.

Fig. 3-10-13 is a block diagram of the CRC generator. This circuit is composed of counter ICD3, D5 and D6 which show the bit positions of the channel status data, CRC generator ICA2, C1, C2, C3, D1 and D2, and their peripheral circuits. ICD3 is a sample counter in the AES/EBU block which outputs (N + 1) when it receives input (N). The bits of the channel mode data changed in response to the mode setting are also output from ICD3.

ICD2 outputs CRC (8 bits) for the changed bits. This output is exclusively OR-ed and stored in register ICA2, C2 and C3. The 8-bit parallel CRC data are converted into serial data by multiplexer ICB2 and then inserted into the designated slot.

CRC is calculated on the basis of the generating polynominal below.

$$G(X) = X^8 + X^4 + X^3 + X^2 + 1$$

| BIT 0-3 | | | | MODE |
|---|---|---|---|---|
| 0 | 1 | 2 | 3 | |
| 0 | 0 | 0 | 0 | DEFAULT |
| 0 | 0 | 0 | 1 | 2 CHANNEL |
| 0 | 0 | 1 | 0 | SINGLE (MONO) |
| 0 | 0 | 1 | 1 | PRIMARY/SECONDARY |
| 0 | 1 | 0 | 0 | STEREO PHONIC |

**Table 3-10-2. Channel Mode Setting (AN-01 Board)**

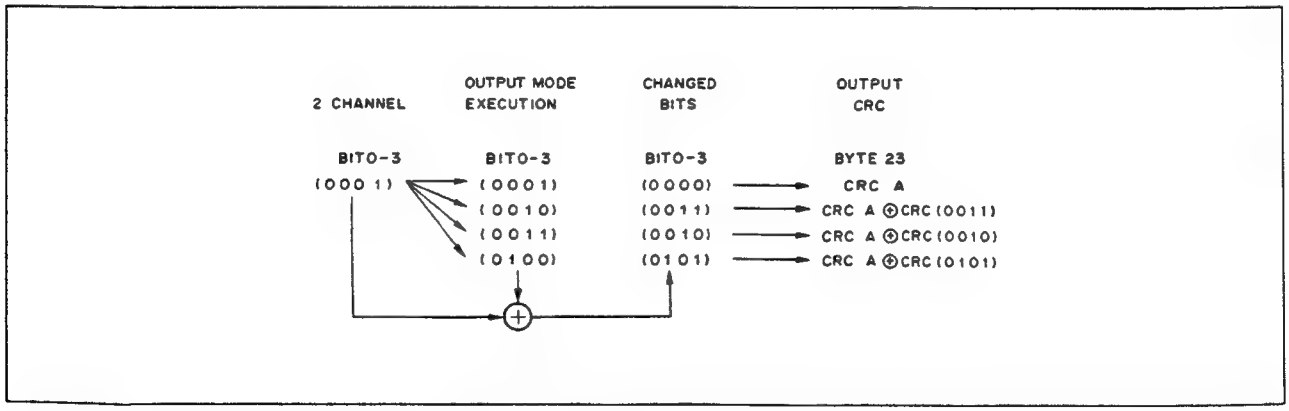



**Fig. 3-10-11. Changed Bits and Output CRC (AN-01 Board)**

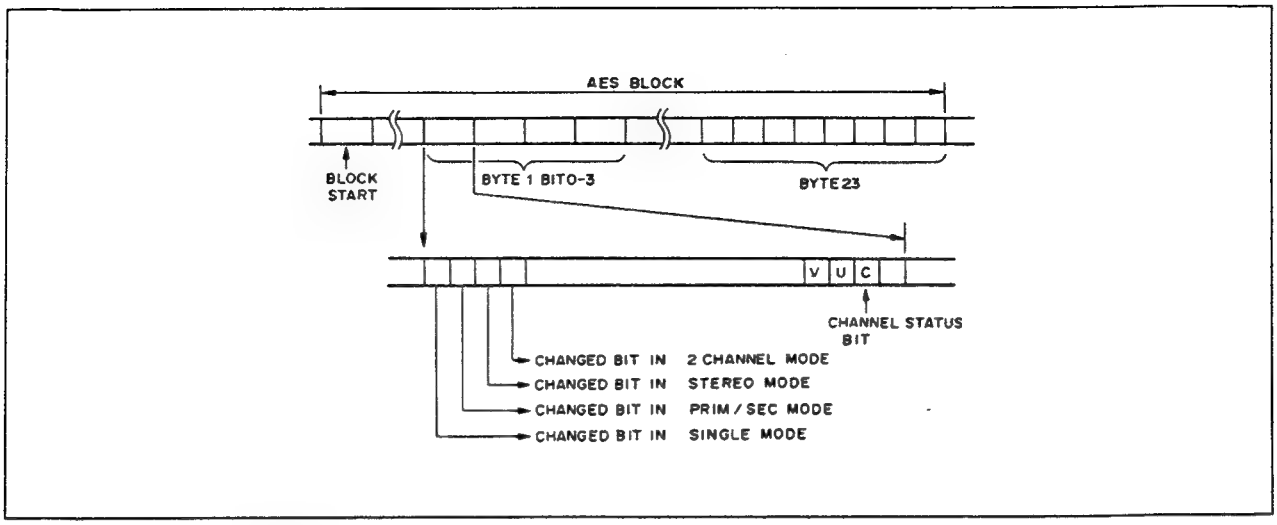



**Fig. 3-10-12. Storage Time Slots (AN-01 Board)**

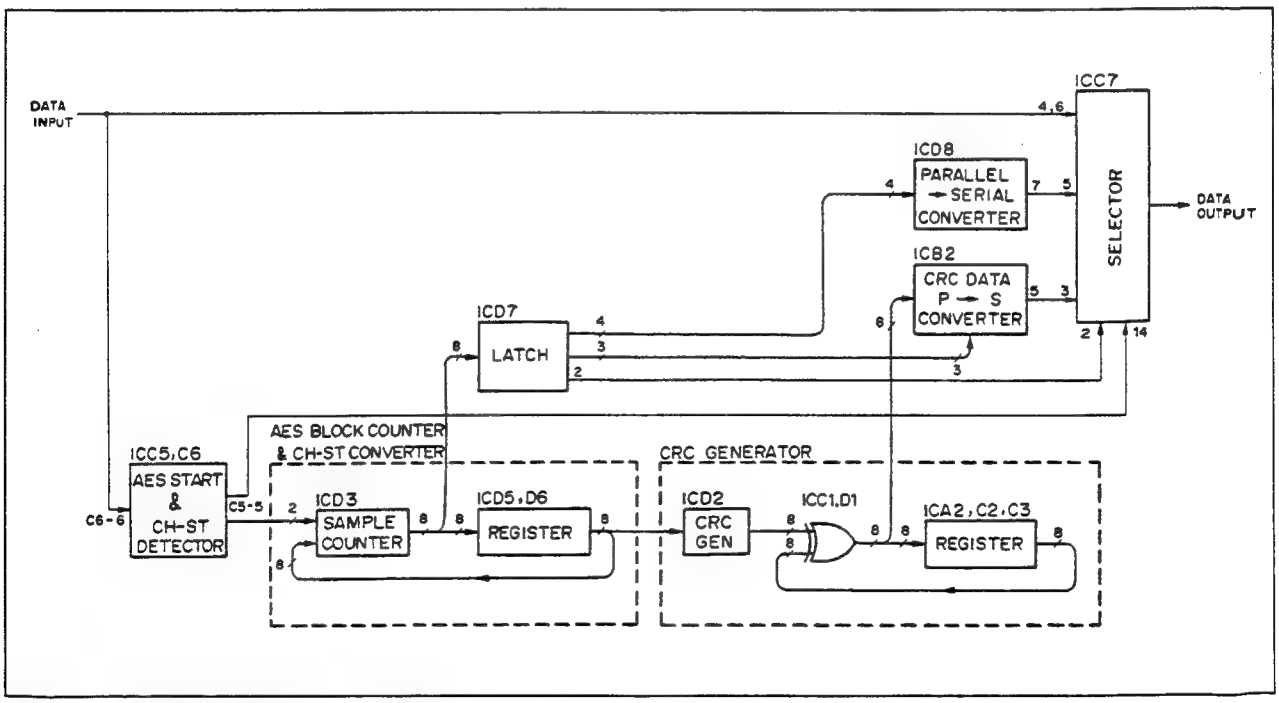



**Fig. 3-10-13. CRC Generator (AN-01 Board)**

## 10. Channel Mode Setting Circuit (AN-01 board)

### 1. ADVANCE head playback data

The ADVANCE head playback data are output for all 4 channels in the monophonic mode from the AN-01 board. The output channel status data are therefore obtained by exclusively OR-ing the changed bits which are read from the time slot corresponding to the monophonic mode and the channel status data of the original data. ICF20 is responsible for this processing.

### 2. CONFI head playback data

In order to regulate the output data from the DIGITAL AUDIO OUTPUT connector, the 2-bits channel mode setting command and 4-bits channel selection command for each channel are supplied to this circuit via the DVR-1000 control panel, IF-139 board and UPI on the AN-01 board. Tables 3-10-3 and 3-10-4 show the bit allocation for each of the commands for CH-1. The allocation is the same for the other channels.

The "ACHMD-0" and "ACHMD-1" channel mode setting commands are supplied to ICE17. In ICE17, the changed bits are read out from the time slot which corresponds to the set channel mode, they are exclusively OR-ed with the channel status data of the original data, and the result is written into the designated slot as the new channel status data.

The "ACH-L0(R0)" and "ACH-L1(R1)" channel selection commands are selected either the left channel or right channel by ICF8 and supplied to data selector ICD17. The output channel is selected by ICD17 according to the resulting contents. With a monophonic mode output, all the bits in subframe B are set to "0" and the "V" flag is raised and output. The same data as for subframe A are output for the "U" and "C" flags.

| ACHMD | | OUTPUT MODE |
|---|---|---|
| 1 | 0 | |
| 0 | 0 | SINGLE |
| 0 | 1 | PRIM/SEC |
| 1 | 0 | STEREO |
| 1 | 1 | 2-CHANNEL |

**Table 3-10-3. Channel Mode Setting (AN-01 Board)**

| ACH | | CHANNEL SELECT |
|---|---|---|
| L1/R1 | L0/R0 | |
| 0 | 0 | CH-1 |
| 0 | 1 | CH-2 |
| 1 | 0 | CH-3 |
| 1 | 1 | CH-4 |

**Table 3-10-4. Channel Selection (AN-01 Board)**

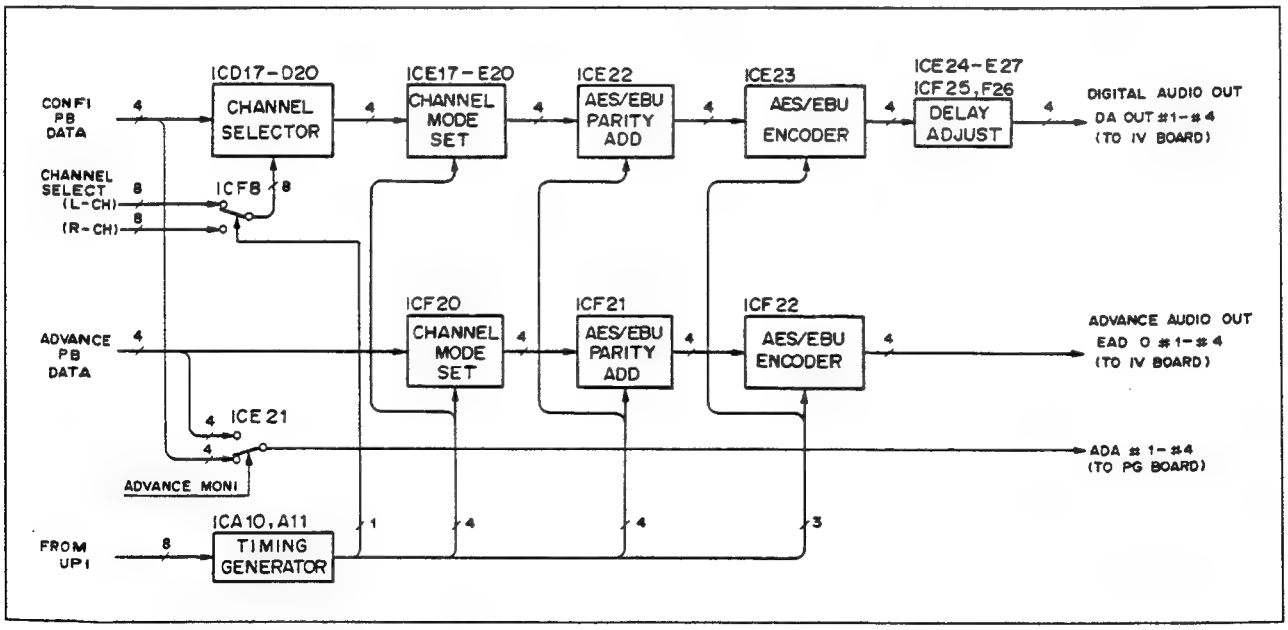



**Fig. 3-10-14. Channel Mode Setting Circuit/AES/EBU Encoder (AN-01 Board)**

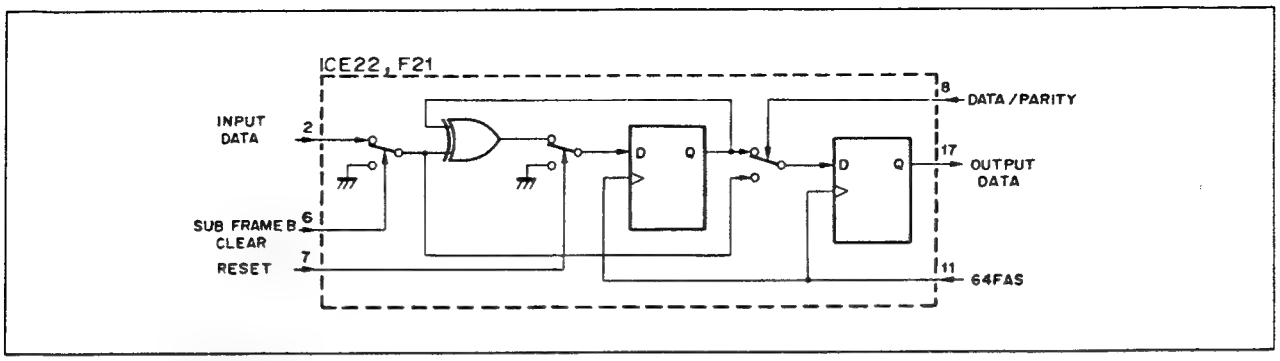



**Fig. 3-10-15. Parity Calculation Circuit (AN-01 Board)**



### 11. AES/EBU Encoder (AN-01 board)

The AES/EBU encoder is composed of parity calculation circuit ICE22/F21 and biphase mark encoder ICE23/F22.

**(1) Parity bit calculation**

The even parity of the audio data in the subframe is calculated, and the result is inserted to the parity bit position and output. ICE22 is for the CONFI head playback data and ICF21 is for the ADVANCE head playback data.

**(2) Biphase mark encoder**

This encoder provides biphase mark modulation for the audio data and, at the same time, it adds the preamble data and outputs them. The CONFI head playback data are processed by ICE23 while the ADVANCE head playback data are processed by ICF22.

Fig. 3-10-16 is a block diagram of the circuit, and Fig. 3-10-17 is a timing chart of the encoder.

In the preamble period, the "PREAMBLE1" signal is selected at the AES/EBU block start position and "PREAMBLE2" is selected at other positions, and these are supplied to the exclusive OR gate and the D-type flip-flop. In a period with a high preamble level, the signals are synchronized to the 128fs clock and the output is inverted.

In audio data periods, the data are inverted at the center and end of the bit at areas where the input data level is high and output; they are inverted at the end of the bit at areas where the input data level is low and output.

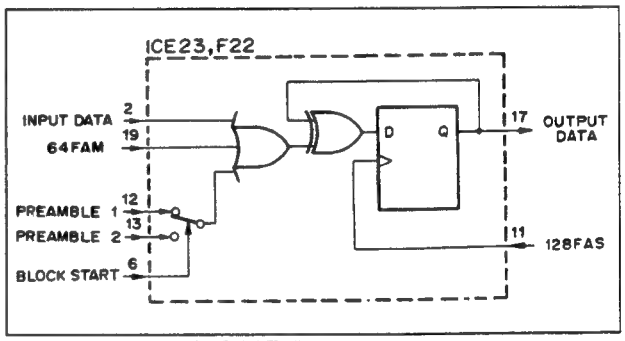



**Fig. 3-10-16. Biphase Mark Encoder (AN-01 Board)**

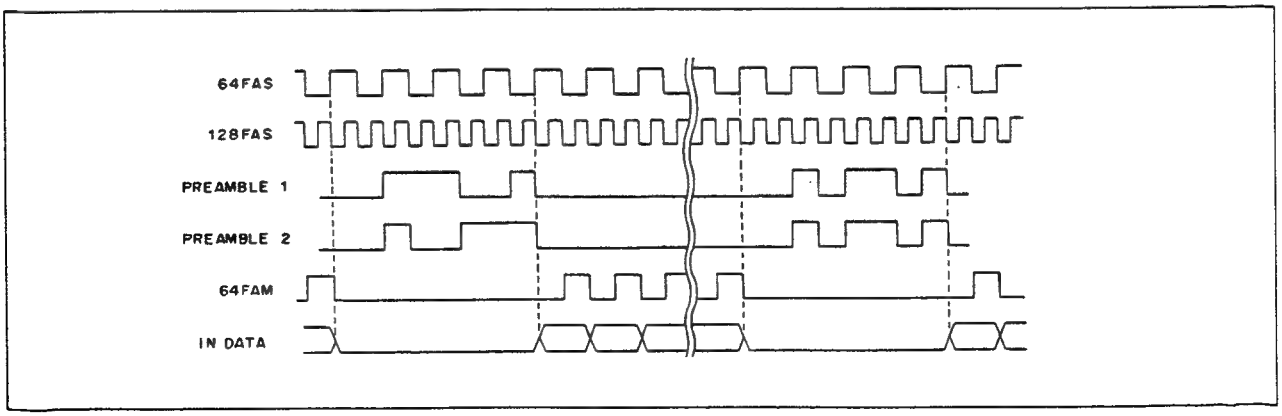



**Fig. 3-10-17. Encoder Timing Chart (AN-01 Board)**

### 12. Digital Audio Output Delay Circuit (AN-01 board)

This is the delay circuit for the CONFI head playback digital audio data which are output from the DIGITAL AUDIO OUTPUT connector, and it is composed of ICE24 to E27, F25 and F26.
It is provided to adjust the phases of the digital audio output and analog audio output, and the delay compensation is provided by the D/A converter, the digital filter and the analog filter in the analog audio output system. The delay amount is set by S4 and S5. At present, S4 is set to "1" and S5 to "2." The current amount of delay is 33 samples. The maximum delay provided by this circuit is 128 samples.

### 13. Output Data to D/A Converter System (AN-01 board)

The audio data which are output from the data format converter are supplied to the PG-13 board via ICD22 and E21. These data are converted into analog signals on the AA-29 board and output externally from the ANALOG AUDIO OUTPUT connector.
Normally, the CONFI head playback data are output to the ANALOG AUDIO OUTPUT connector but when advance monitor jumper JP2 is shorted, the ADVANCE head playback data can be output to this connector.

## 4-4. IE-17 BOARD

The IE-17 board may have the board number suffix of "−11" or "−12." In either case, the configuration of the circuitry is virtually identical although the reference numbers of some parts differ between boards with the "−11" suffix and boards with the "−12" suffix. The following description applies to a board with the "−11" suffix unless otherwise noted.

The IE-17 board is the digital signal processing board for the recording system and it is composed of the following circuits.

- Audio shuffling circuit
- Video/audio/ID data mixing circuit
- Inner encoder
- ID encoder
- Sync adder
- Scrambler
- Data serializer

The IE-17 board serves to shuffle the data which have been output from the audio outer encoder on the AE-06 board, mix these data with the video data supplied from the VE-12 board, add the sync and ID data, convert these data into program track data which conform to the D-1 format, and output them. The resulting data are sent to the DVR-1000 and recorded onto tape.

Also output from the IE-17 board are the data (BYPASS-3) from the inner encoder which are output as bypass system data to the CI-01 board and both the scrambler output (BYPASS-2) and serializer output data (BYPASS-1; EE DATA) which are sent to the SY-70 board.



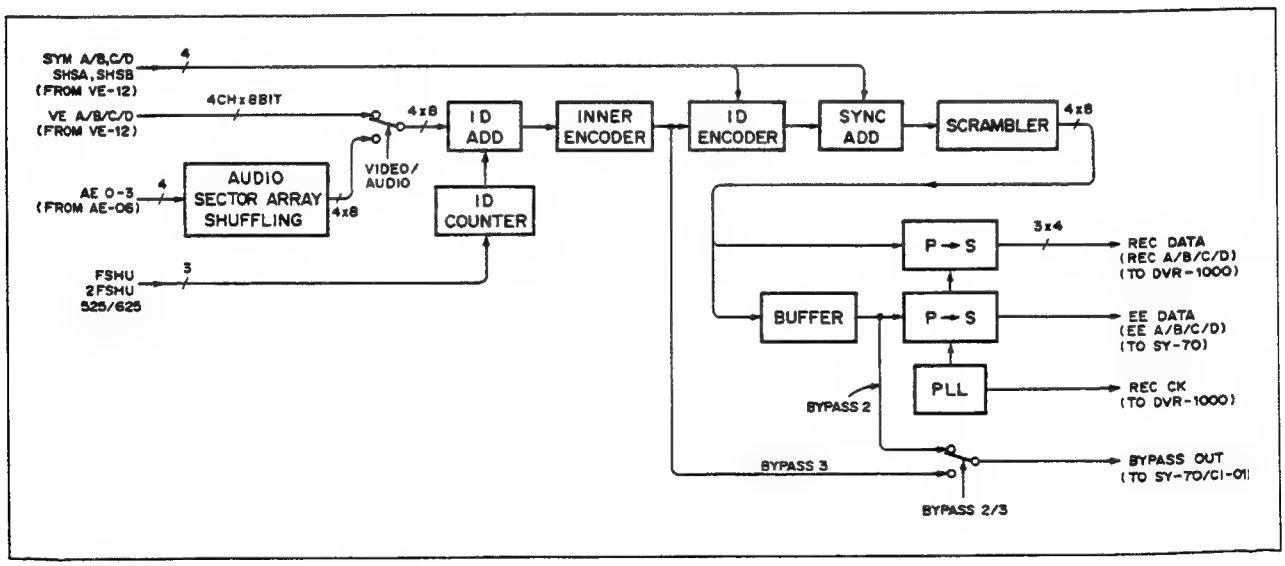



**Fig. 4-1. Function Diagram (IE-17 Board)**

## 1. Audio Shuffling Circuit (IE-17 board)

The audio data (including the addition data) which have been processed by the outer encoder on the AE-06 board are supplied to the sector array shuffling circuit on the IE-17 board. The shuffling size is one audio sector (120 outer code blocks = 600 bytes).

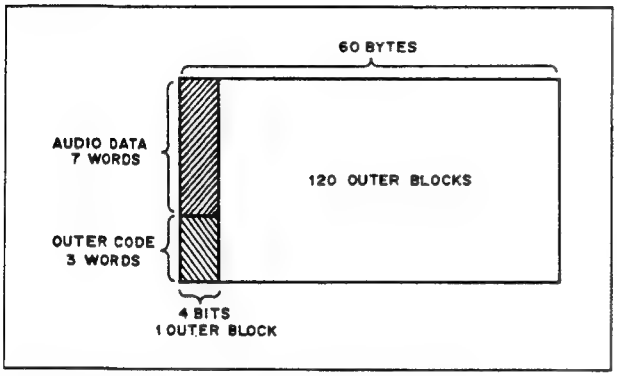



**Fig. 4-2. Audio Sector Array (IE-17 Board)**

The 4-bit parallel data with a bit rate of 3.072 MHz (64×48 kHz) are supplied to the IE-17 board in outer code block units in the sequence of 1E (CH-1 EVEN OUTER CODE) → 2E → 3E → 4E →1O (CH-1 ODD OUTER CODE) →2O → 3O → 4O.

A block diagram of the audio shufflig memory is shown in Fig. 4-4 and a block diagram of the shuffling memory address control circuit is shown in Fig. 4-5.

The shuffling memory is composed of 8 SRAMs. Data are written into four of these SRAMs (#1, #2, #3, #4) while data are read out from the other four ($\#\overline{1}$, $\#\overline{2}$, $\#\overline{3}$, $\#\overline{4}$).

The audio data supplied to the IE-17 board are assigned for each audio sector and they are written into the designated area of the shuffling memory (SRAM). Shuffling is done by controlling the memory write addresses. Fig. 4-6 shows the layout of a product block after shuffling.

Each memory is divided into 4 areas as shown in Table 4-1 and each area is made to correspond to the audio sectors (1E, 2E, 3E, 4E, 1O, 2O, 3O, 4O). The 4-bit data adjoining each audio sector are written into shuffling memory #1/#2 (or #3/#4). For readout, the same addresses are given to #1/#2 (or #3/#4) and 8-bit data are provided.

The point at which data readout starts from the shuffling memory is determined by the audio shuffling start pulse "ASH A/C" change point. In other words, this start point for the CH-A/CH-B data readout is determined on the basis of the ASH A/C fall and the start point for the CH-C/CH-D readout is determined on the basis of its rise.

| | SRAM / ADDR | #1 | #2 | #3 | #4 |
|---|---|---|---|---|---|
| −1 | 000 − 257 | 1E 2K+1 | 1E 2K | 2E 2K+1 | 2E 2K |
| −2 | 400 − 657 | 1O 2K+1 | 1O 2K | 2O 2K+1 | 2O 2K |
| −3 | 800 − A57 | 3E 2K+1 | 3E 2K | 4E 2K+1 | 4E 2K |
| −4 | C00 − E57 | 3O 2K+1 | 3O 2K | 4O 2K+1 | 4O 2K |

**Table 4-1. Audio Sector Assignment in SRAMs (IE-17 Board)**

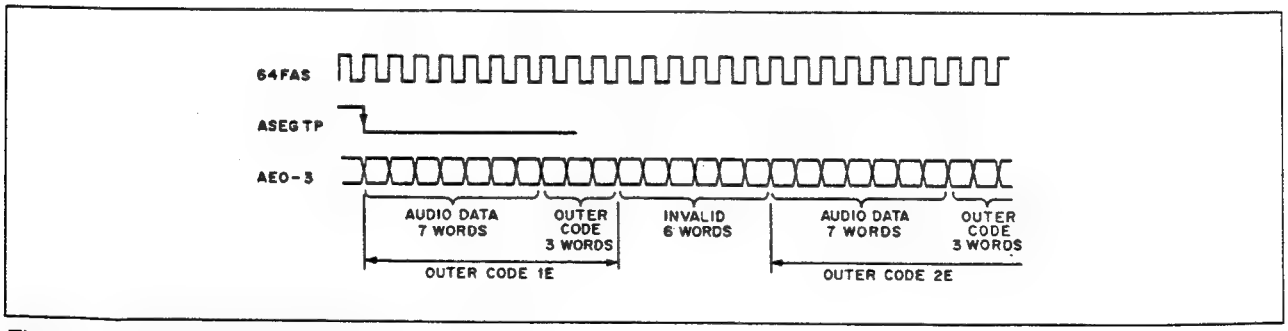



**Fig. 4-3. Audio Data Input Format (IE-17 Board)**

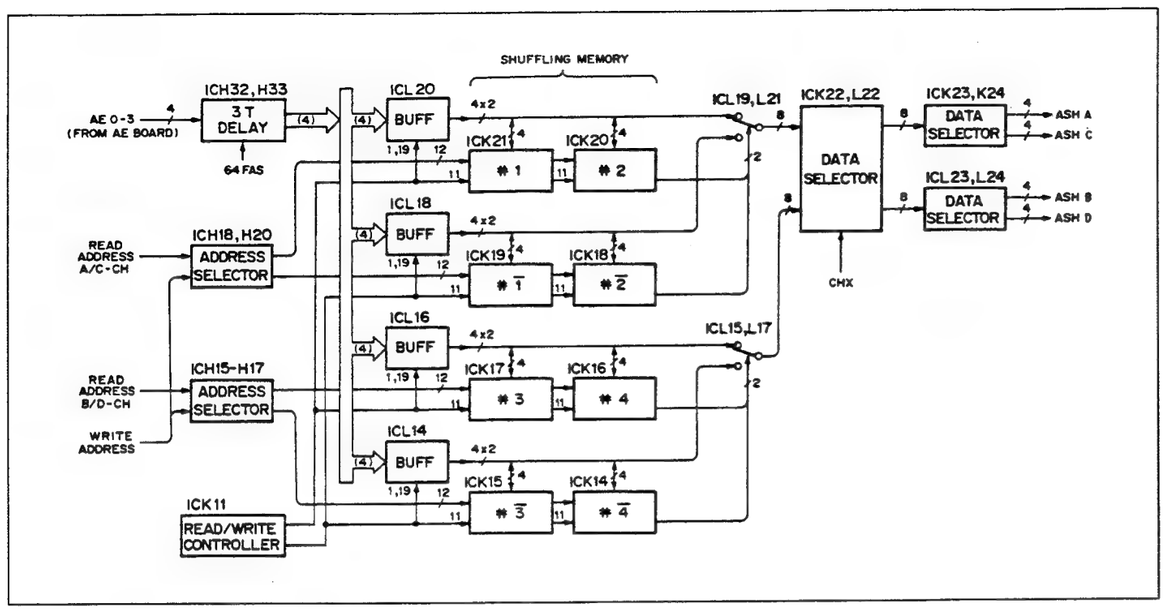



Fig. 4-4. Audio Shuffling Memory (IE-17 Board)

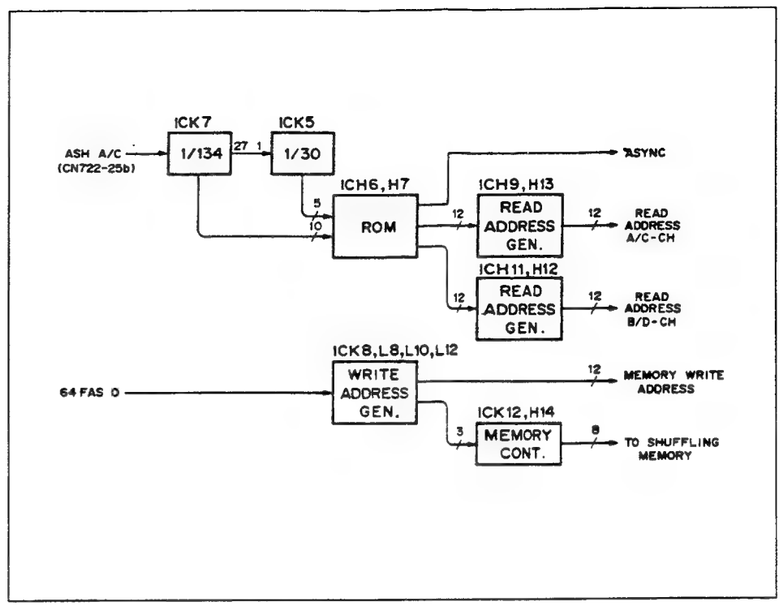



Fig. 4-5. Audio Shuffling Memory Address Controller (IE-17 Board)

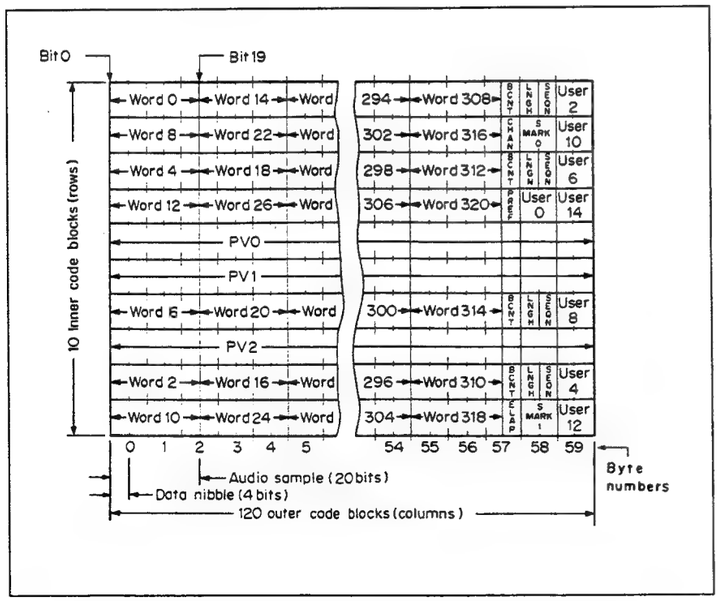



Fig. 4-6. Digital Audio/Ancillary Data Product Block (Even sample block/IE-17 Board)

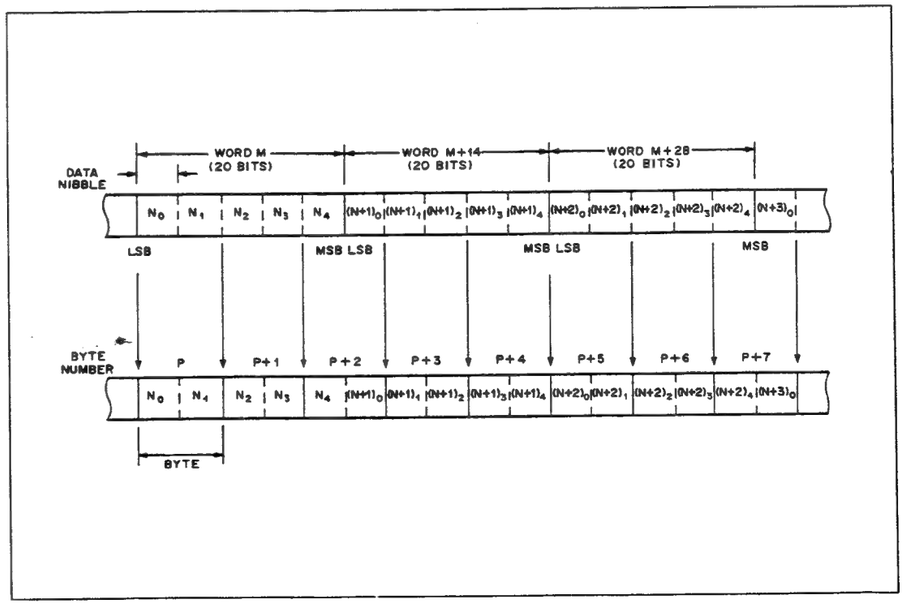



Fig. 4-7. Word/Byte Conversion (IE-17 Board)

The audio sector array prescribed by the D-1 format is shown in Fig. 4-8. In order to simplify the circuitry, the shuffling memory #1/#2 data are output to recordings channels CH-A/CH-C and the shuffling memory #3/#4 data are output to channels CH-B/CH-D. The CH-C/CH-D and CH-A/CH-B data are now exchanged by the channel change signal "CHX" to provide the designated data sequence. This operation is shown in Fig. 4-9. Under the D-1 format, the audio data are written twice, and the same data are output to CH-A and CH-C and to CH-B and CH-D.

In the shuffling memory, the audio data which were supplied at a bit rate of 64 FAS (3.072 MHz) are replaced by the system clock signal (9.83682 MHz) and output. At the same time, empty slots are provided and output for the SYNC/ID data and inner error code which will be added at a later stage. The reference signal "A SYNC" for audio data processing is also output.

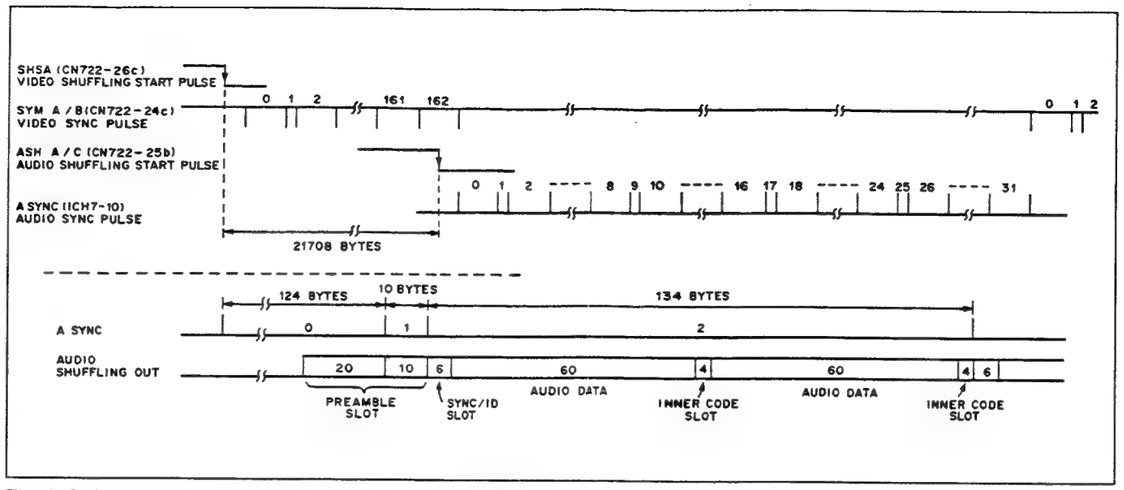



**Fig. 4-10. Audio Shuffling Memory Output Timing (IE-17 Board)**

**2. Video/Audio/ID Data Mixing Circuit (IE-17 board)**

This circuit mixes the video data supplied from the VE-12 board with the ID data and the audio data shuffled on the IE-17 board, and it outputs program track format data. The ID data added here are regulated inside the processor and the ID encoder described later converts them into ID data conforming to the D-1 format.

The mixing of the data is based on the sync pulses "SYM A/B" and "SYM C/D" supplied from the VE-12 board and the "A SYNC" signal provided by the audio shuffling circuit. In actual fact, it is after the ID data and inner error code slots and the edit gaps have been provided in the previous circuit that the video and audio data are supplied to the mixing circuit where the output enable pins of the registers are controlled and the data are multiplexed.

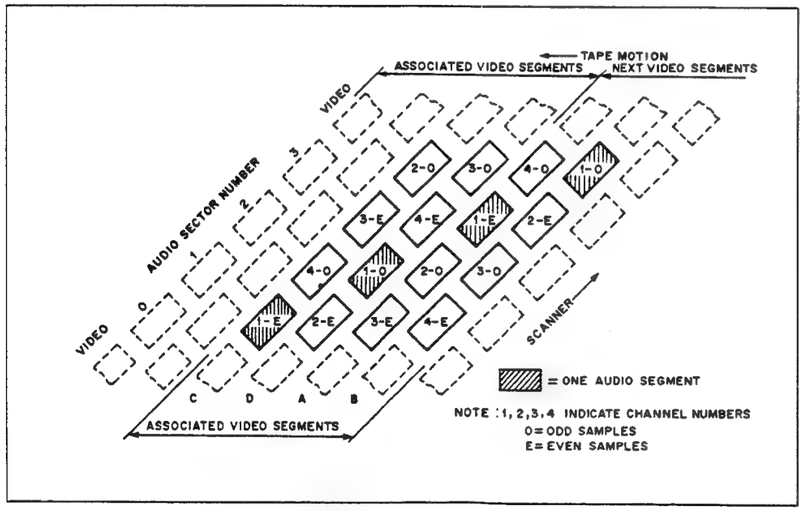



**Fig. 4-8. Audio Sector Array (IE-17 Board)**

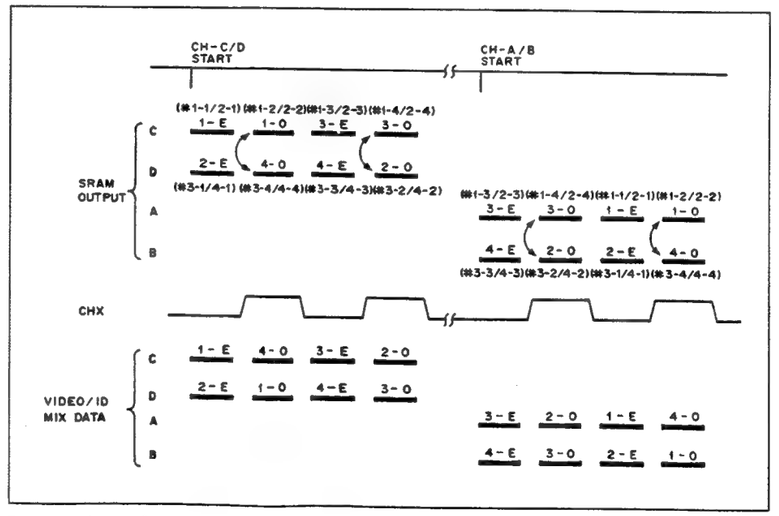



**Fig. 4-9. Audio Channel Exchanging (IE-17 Board)**

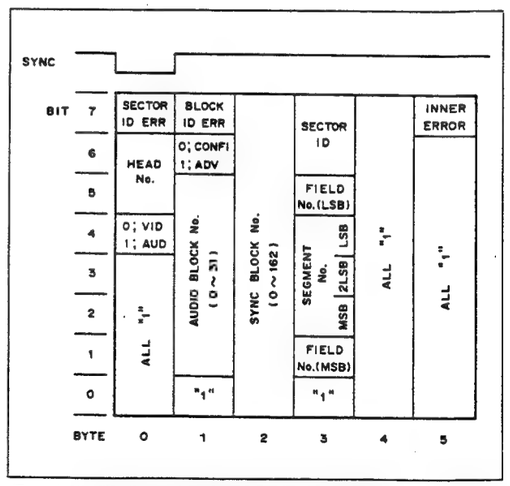



**Fig. 4-12. ID Data Regulated Inside Processor (IE-17 Board)**

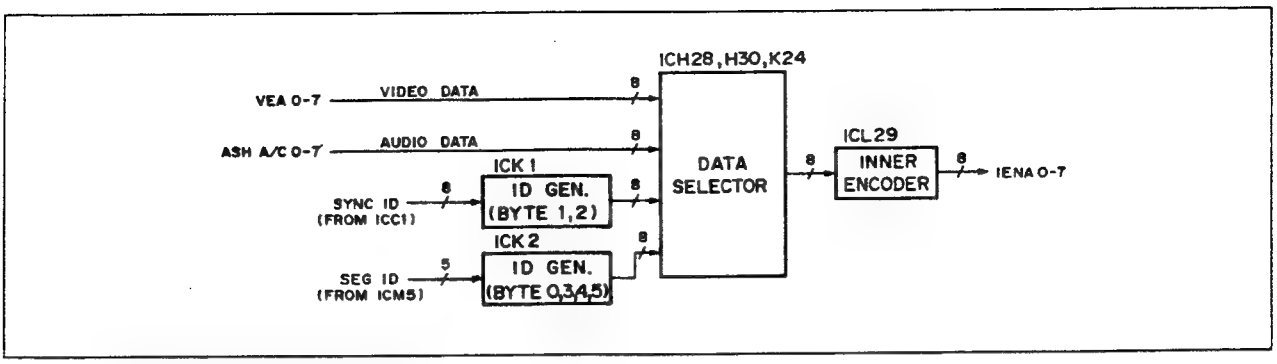



**Fig. 4-11. Video/Audio/ID Data Mixing Circuit (IE-17 Board)**

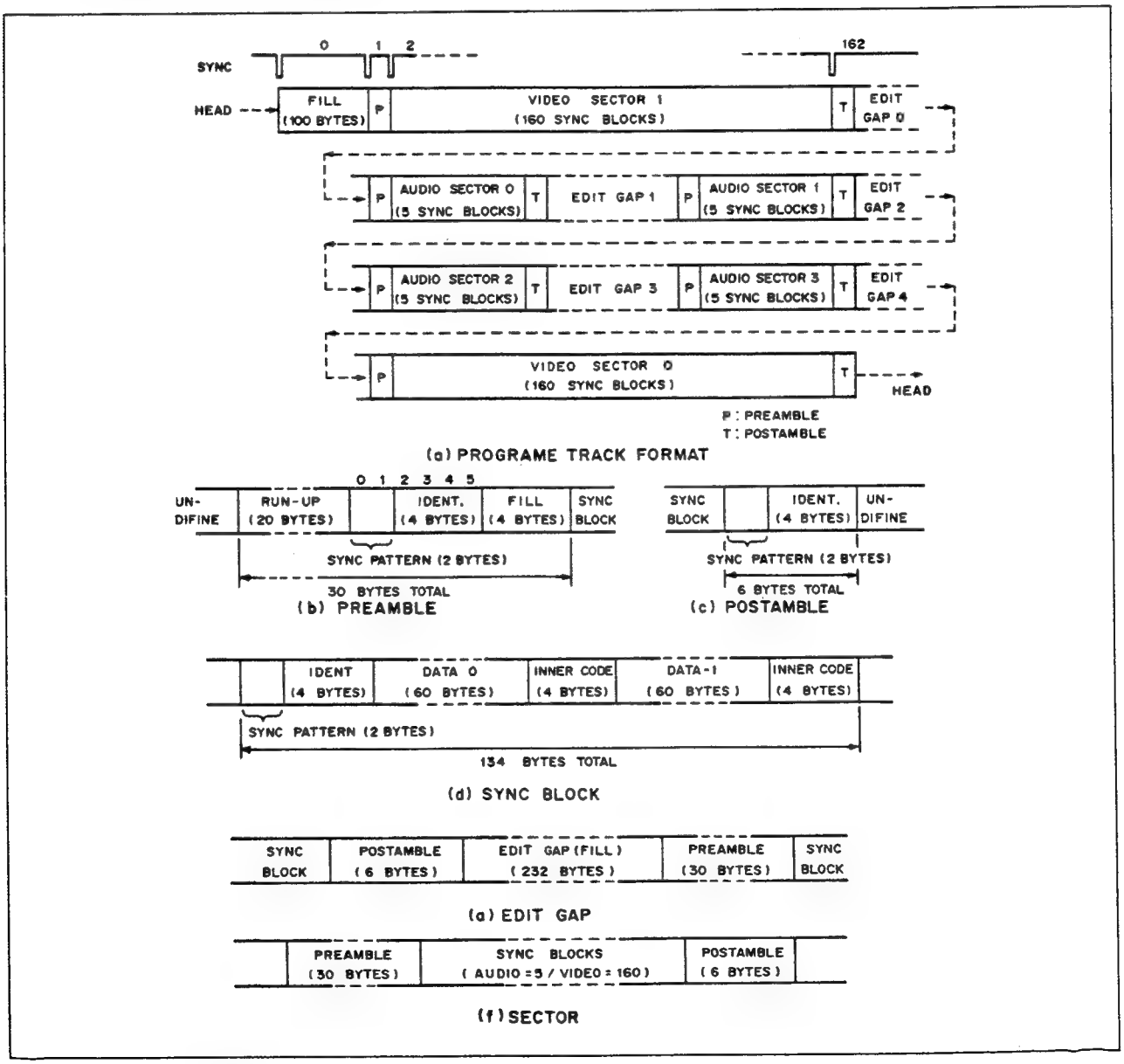



**Fig. 4-13. Sector Configurations (IE-17 Board)**

### 3. Inner Encoder (IE-17 board)

The inner encoder generates the 4-byte R-S inner correction codes for the 60-byte video and audio data and it does this for each channel. These codes are inserted into the designated slots and output. This processing is done by ICL26, L29, M26 and M29 (CXD1037G, Sony).

### 4. ID Encoder/SYNC Adder Circuit (IE-17 board)

In this circuit, the ID data of the processor internal format are extracted from the inner encoder output data (IENA, IENB, IENC and IEND) and converted to ID data conforming to the D-1 format. This processing is done by PROM ICC8, D8, F8 and G8. The ID data added have undergone the 4-8 mapping process shown in Table 4-2.
At the same time, the sync pattern ($30_H$ and $F5_H$) and FILL data ($CC_H$) are inserted so that the ultimate program track format is formed.

### 5. Scrambler (IE-17 board)

After they have been output from the ID encoder, the 8-bit data are converted into serial data and recorded on tape. Leaving them untreated, however, presents the possibility of long strings of "0" or "1" only which results in the generation of DC components in the recording data. The recording data are therefore randomized and the DC components with long periods are extracted.
In actual fact, the data are randomized by exclusive OR-ing the recording data and dummy random signal output from PROM ICC13 and F13. However, only the video data, audio data and error codes are processed at this stage.
This operation enables the correlation between those images which could not be extracted by shuffling to be suppressed. There are 5 random sequences (A/B/C/D/E) and Fig. 4-15. shows how they correspond on the screen.

| INPUT (ID NIBBLE) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OUTPUT (ID BYTE) | 1B | 2E | 35 | 47 | 5C | 69 | 72 | 8D | 96 | A3 | B8 | CA | D1 | E4 | ILLEGAL | |

**Table 4-2. ID Code Mapping (IE-17 Board)**

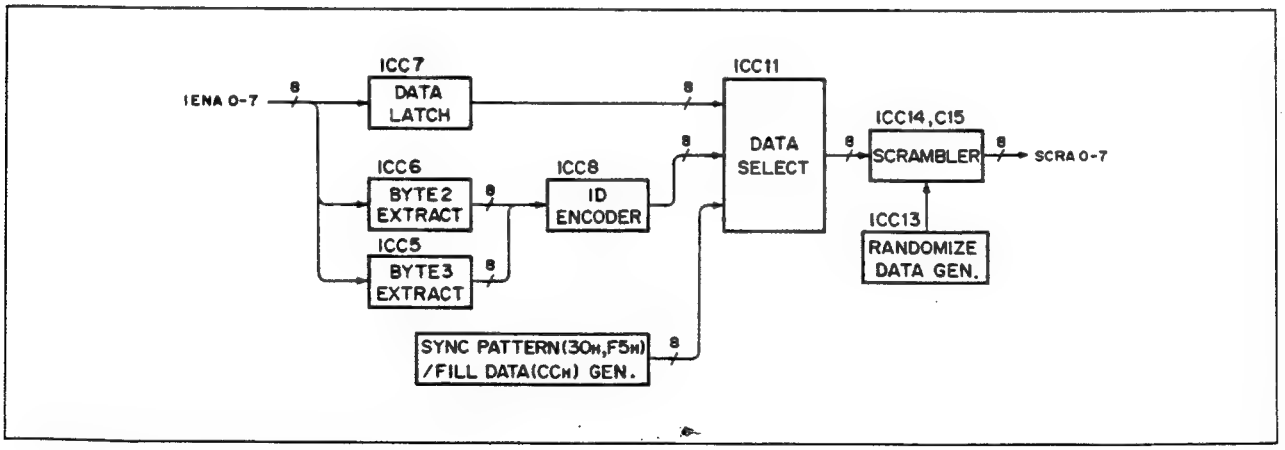



**Fig. 4-14. ID Encoder/Scrambler (IE-17 Board)**

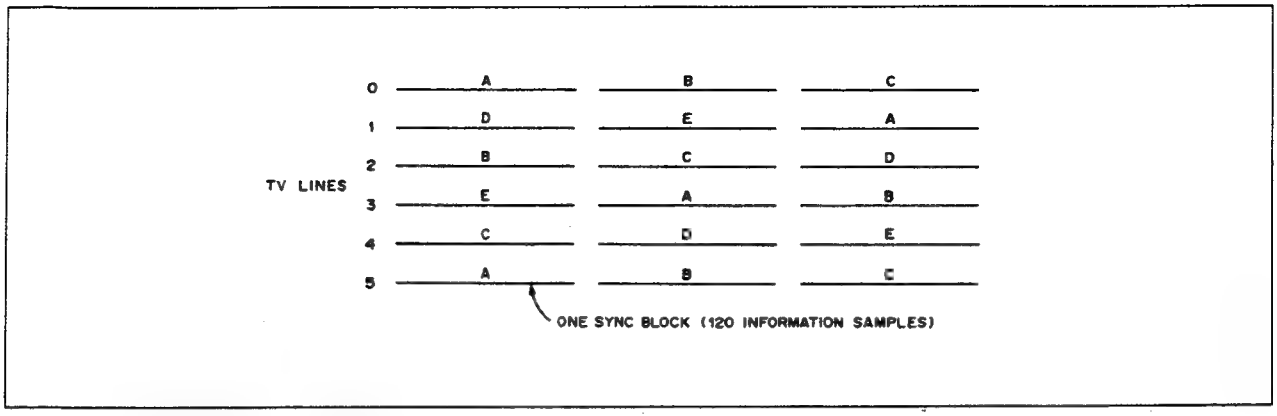



**Fig. 4-15. Relationship Between Random Sequences and TV Lines (IE-17 Board)**



### 6. CH-B/CH-D Delay Circuit

Since the CH-A/CH-B and CH-C/CH-D recording heads are mounted with the prescribed clearance between them, the data supplied to the CH-B and CH-D heads must be delayed beforehand so that they will come after the CH-A and CH-C head data. This delay circuit uses an FIFO memory to delay the CH-B and CH-D data by 1460 bytes. Because of the characteristics of the ICs used on an IE-17 board with the board number suffix of "−11," these 1460 bytes are divided into 910 bytes and 550 bytes and processed by two FIFO memories.

### 7. Preview Buffer (IE-17 board)

In order for signals to be played back by the playback-only head on the DVR-1000, they are played back at a timing which is delayed by 106° 42' (1.976 msec) from the recording. Therefore, in order to provide EE signals at the same timing as the playback data, it is necessary to delay the EE data by an amount equivalent to the above delay.

Two sets of data are output from the scrambler. One set of data is sent as the recording data through the data serializer to the DVR-1000; the other set of data is delayed in this circuit by 19,284 bytes (525/60 systems) or 19,272 bytes (625/50 systems) and sent through the data serializer to the PB/EE selector on the SY-70 board as the EE data.

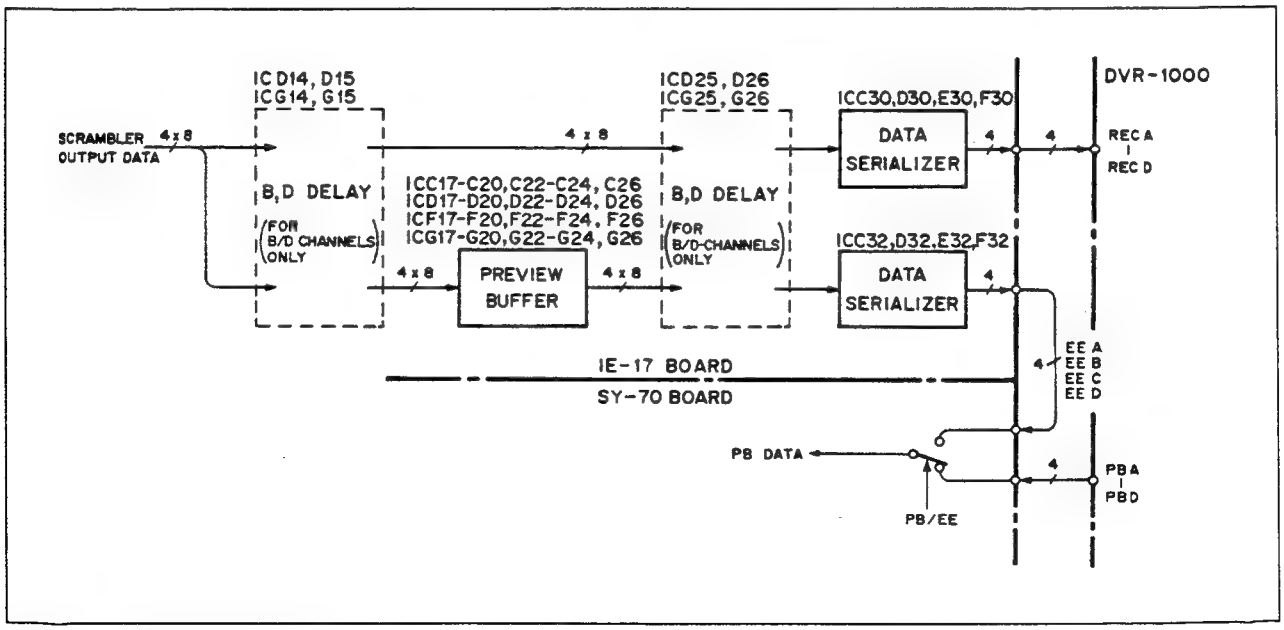



**Fig. 4-16. Preview Buffer (IE-17 Board)**

### 8. Data Serializer/PLL (IE-17 board)

The data serializer is designed to convert 1-byte data (clock frequency of 9.83682 MHz) into serial data (clock frequency of 78.69456 MHz) and to output them. The circuitry configuration of each channel is identical and so only CH-A will be described here.

Upon output from the scrambler, the 8-bit parallel data are first converted into 4-bit parallel data by ICC27 and C28 and further converted from the TTL level to ECL level by ICC29 at the next stage. The "RECCDA" signal is input from the TG-28 board to pin 6 of ICC29 and all areas (edit gaps and undefined areas) not for the recording data are converted into the prescribed data. These data are converted into serial data by ICC30 and output.

The bit clock signal "RECCK" (78.69456 MHz) is generated by the PLL circuit shown in Fig. 4-18.

The EE data which are output to the SY-70 board are also converted into serial data by the same kind of serializer circuit. However, the EE data are not gated by the "RECCDA" pulse.

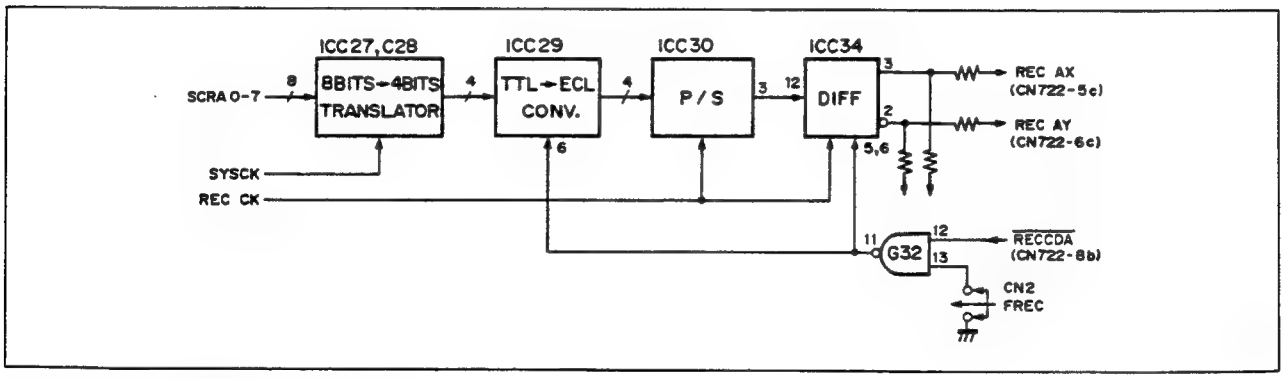



**Fig. 4-17. Data Serializer (IE-17 Board)**

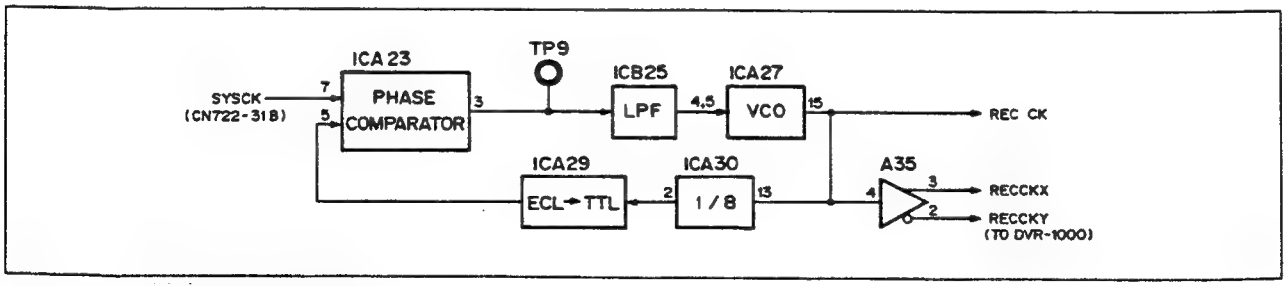



**Fig. 4-18. PLL Circuit (IE-17 Board)**

## 4-5. SY-70 BOARD

The SY-70 board is composed of the following circuits.

- Data input circuit
- PLL circuit
- Serial-parallel converter
- TBC
- Sync/ID detector
- De-scrambler

On the SY-70 board, the clock signal is extracted from the playback serial data, the input data is synchronized with the extracted clock signal and, in order to facilitate the subsequent data processing, the playback serial data is converted into parallel data at the appropriate phase. Furthermore, in order to simplify the subsequent circuit for handling data rate fluctuations at ±40 times normal speed, the parallel converted data is converted into data whose rate is fixed by the time base corrector.

Block synchronization is undertaken for the data which is then de-scrambled and, together with the sync pulses which are extracted from the data, it is supplied to the CI-01 board.

On the SY-70 board, the ID data is also extracted, ID errors are detected and the data is converted into the format ID inside the processor. The ID error information and the ID data obtained through conversion are inserted into the data lines and sent to the CI-01 board.

Each DVPC-1000 is equipped with two SY-70 boards: one board processes either the A and B or C and D channel signals. Consequently, two sets of the above circuits are provided for each board. The following description is confined to channel A (C).

### 1. Data input circuit (SY-70 board)

The playback data from the DVR-1000 is supplied to the SY-70 board at the ECL differential level. Furthermore, serial EE data is supplied from the IE-17 board.

When the EE mode is designated from the control panel in the preview mode, or when the test mode (BYPASS-1) is designated, the serial EE data is selected and supplied to the PLL circuit described next. The input signal applying in the preview mode is selected in accordance with the "SRE A/C" (or SRE B/D) signal which is supplied from the TG-28 board. The input data for preventing malfunctioning in the PLL circuit is gated when the head is not touching the tape.



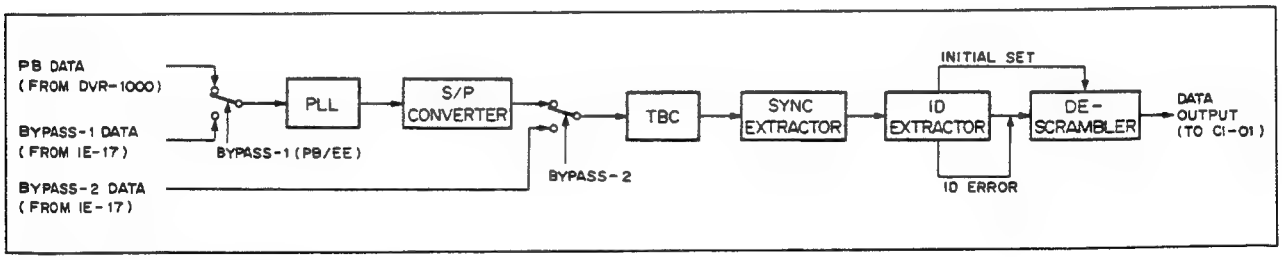



**Fig. 5-1. Function Diagram (SY-70 Board)**

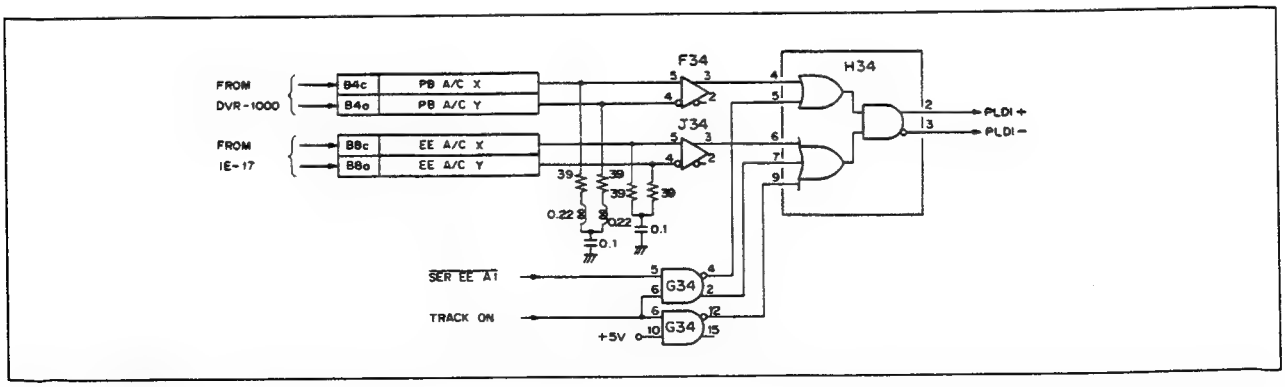



**Fig. 5-2. Data Input Circuit (SY-70 Board)**

## 2. PLL circuit (SY-70 board)

The playback serial data which contains jitter and which is characterized by changes in the data rate is supplied to the SY-70 board at speeds ranging from 40 times slower (approximately 52 MHz) to 40 times faster (approximately 107 MHz) than normal tape speed. The PLL circuit serves to extract the clock component from this data, synchronize the data and output the data together with the clock signal to the serial-parallel converter.

### (1) Timing extractor

As shown by Fig. 5-3, this circuit is an exclusive NOR circuit which uses an ECL gate. It differentiates the input data and extracts the clock component.

### (2) Phase comparator/charge pump

The phases of the timing pulse (C) and playback clock signal (D, E) output from the voltage-controlled oscillator (VCO) are compared here, the charge pump is charged by the pulse in the advance phase direction and it is discharged by the pulse in the delayed phase direction. This functions to control the oscillation frequency of the VCO by the resulting error voltage (average value of both pulses) and the phase of the playback clock is locked to the input data when the phases of the two pulses do not coincide.

In order to maintain this locking range with speeds extending from 40 times slower to 40 times faster than normal tape speed, the tape speed information is supplied from the DVR-1000 via the IF-139 board and UPI ICB32 to the charge pump. Since this information is approximate, it will be electrically isolated when the phase is locked by the PLL circuit. Whether or not this information is to be made valid is determined by $V_{BE}$ of transistors Q106 and Q107, time constant capacitor voltage "Vc" and external speed information voltage "Vs." When $|Vc - Vs|$ is greater than $V_{BE}$, the tape speed information supplied from the external source is made valid.

### (3) VCO

The voltage-controlled oscillator is controlled by the above-mentioned error voltage, and its oscillation frequency is double the input data rate (±40 times normal tape speed: 104 MHz to 214 MHz).

The VCO output is divided down to half by ICE29 and this is used as the clock signal to latch the input data.

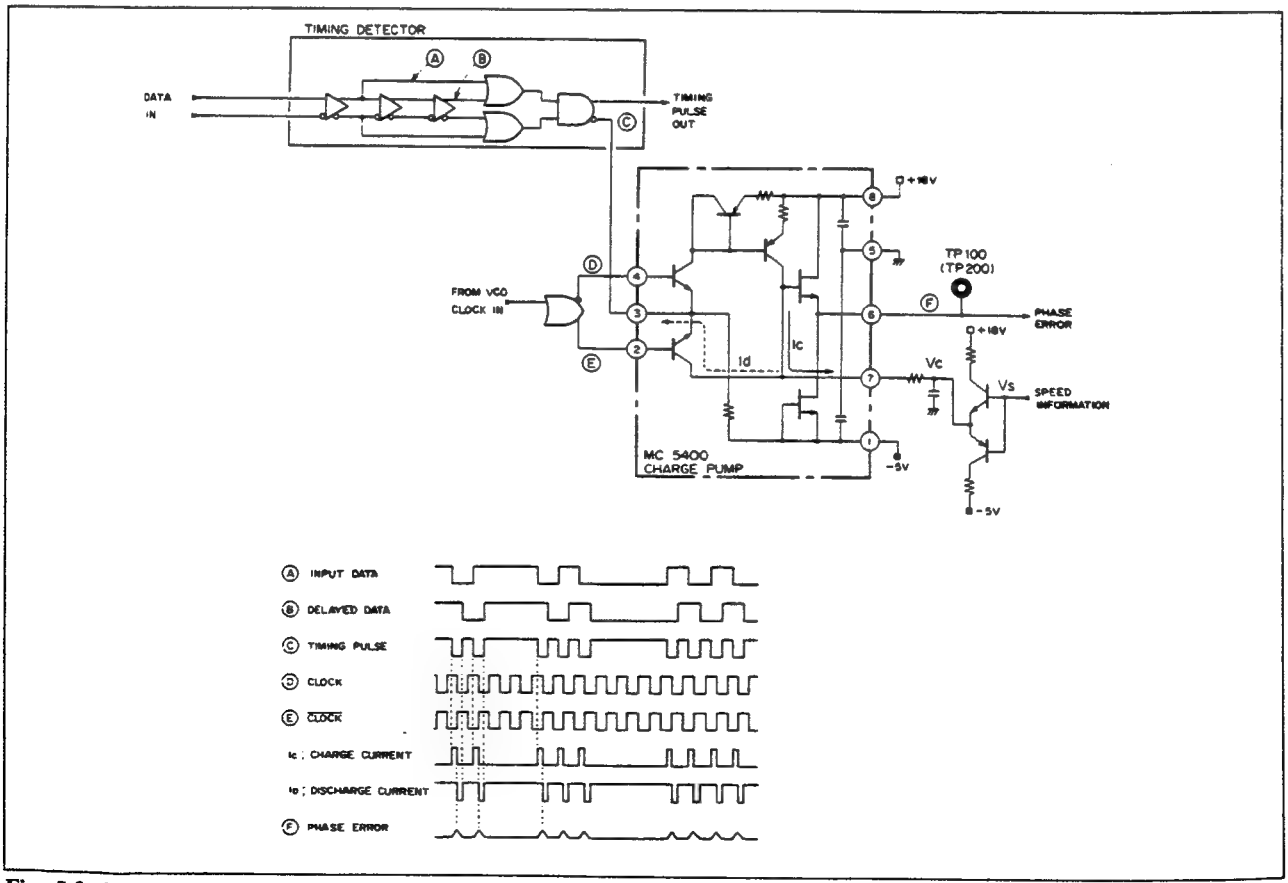



**Fig. 5-3. PLL Circuit and Timing Chart (SY-70 Board)**

### 3. Serial-parallel converter (SY-70 board)

This serves to convert serial data with a data rate of between 52 MHz and 107 MHz into 8-bit parallel data at the appropriate phase.
Fig. 5-4 is a block diagram and an input/output timing chart.

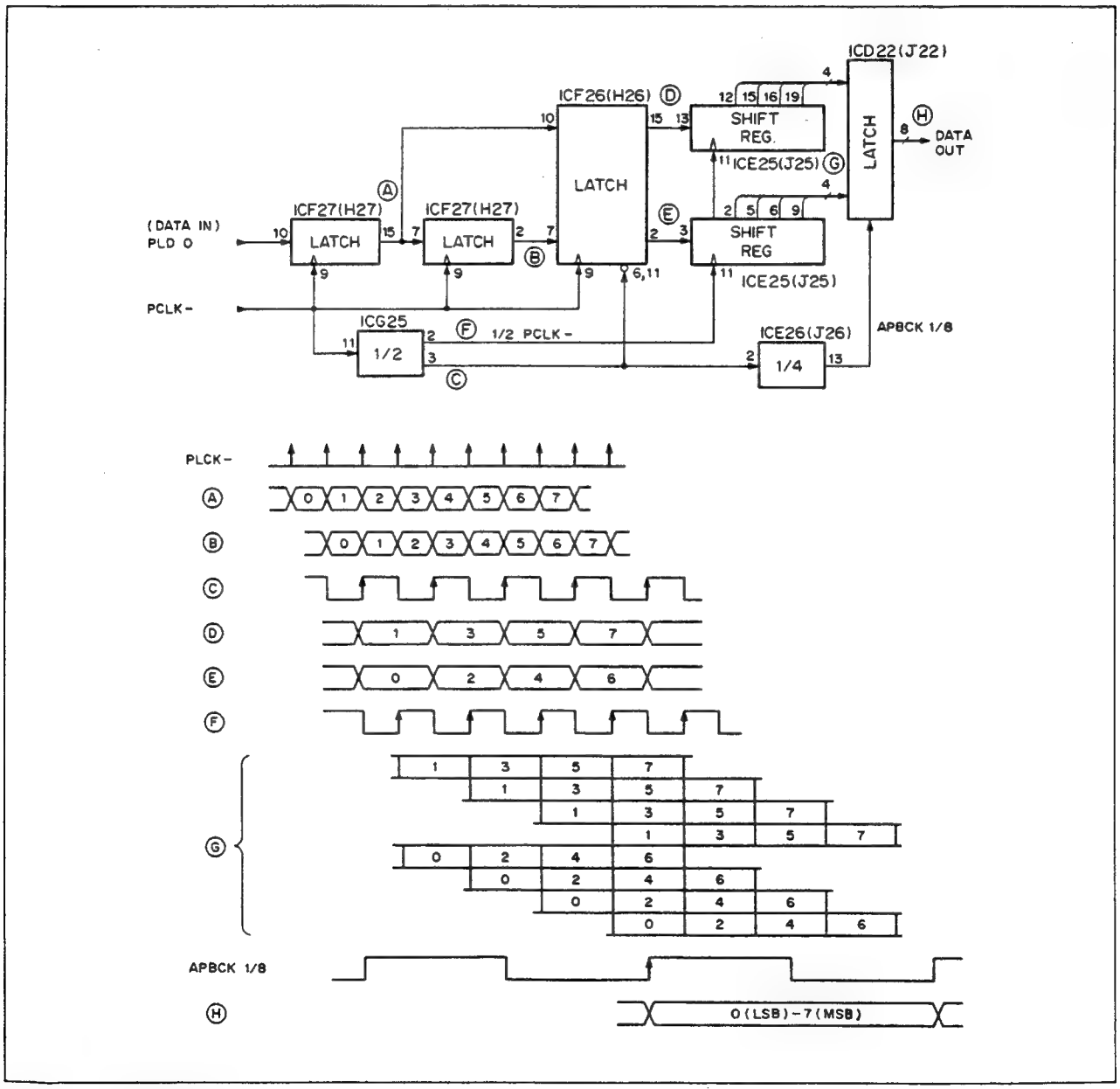



**Fig. 5-4. Serial-Parallel Converter (SY-70 Board)**

### 4. TBC (SY-70 board)

At tape speeds of ±40 times normal speed, the data rate fluctuates by about 30 per cent compared with normal playback. Although these fluctuations can be absorbed by the frame memory, it is difficult to assign properly the data played back at different rates from different heads to each channel using the frame memory. A time base corrector is therefore provided in order to facilitate the subsequent processing, and the readout rate is aligned with the recording frequency.

The TBC uses six SRAMs (16K×4) per channel, and they yield a memory size of 48 K bytes for each channel.

In order to safeguard against addresses overtaking or being overtaken during stunt playback, the "*RSTART" read start signal of the TBC is controlled by the tape speed. Memory read/write control is exercised by the 12.288 MHz (FAS256=48 kHz×256) clock signal. Writing takes precedence over reading, and data is read at times when no data writing is being undertaken.

The parallel EE data (BYPASS-2) for test purposes is supplied from the VE-12 board to the TBC.

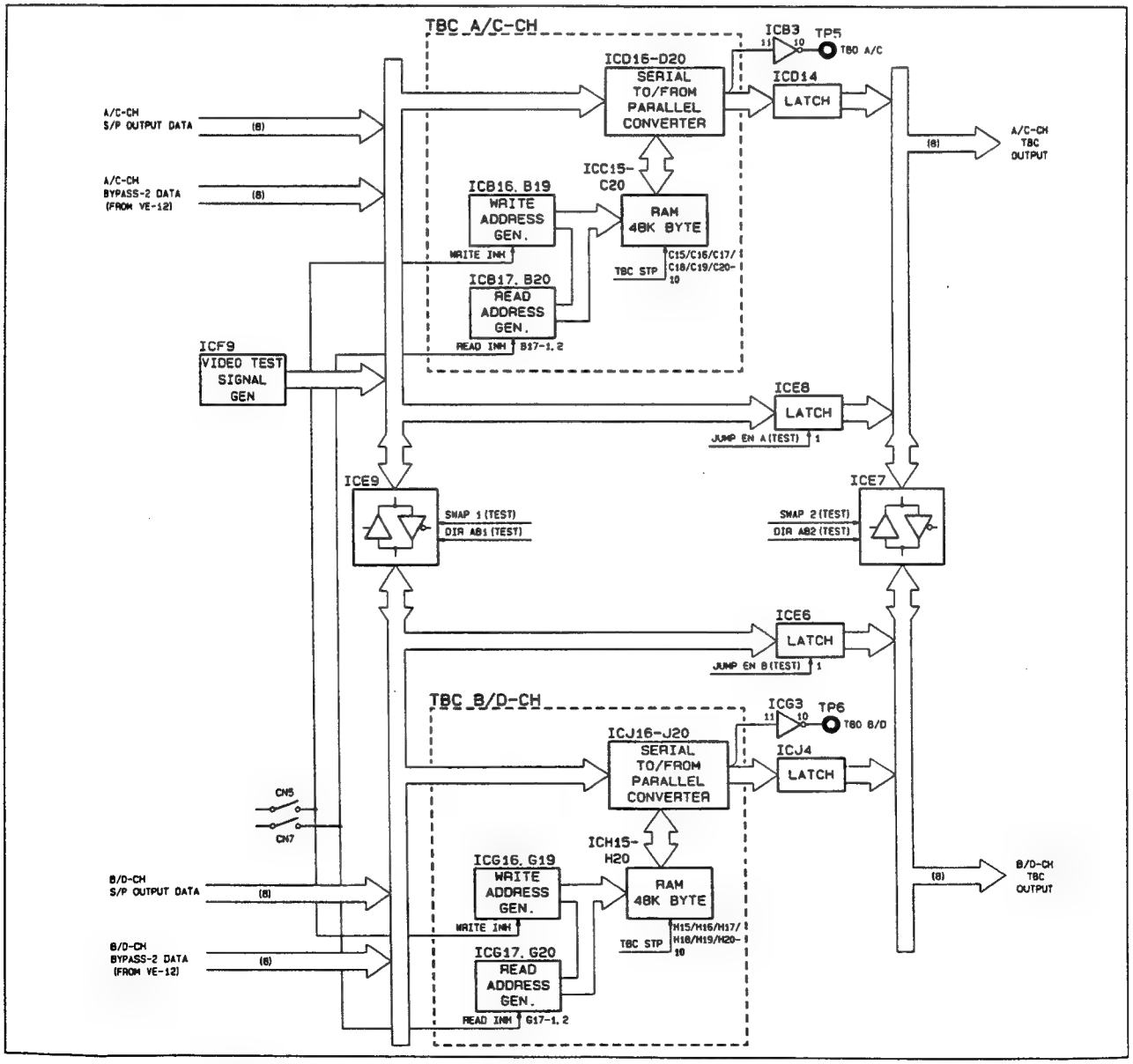



**Fig. 5-5. TBC (SY-70 Board)**

## 5. Sync/ID extractor (SY-70 board)

### (1) Sync bit pattern detector (SY-70 board)

The input data is converted into 8-bit parallel data at the appropriate phase by the above-mentioned serial-parallel converter, and the samples are not aligned in sequence from the regular most significant to least significant bit. This circuit serves to detect the sync pattern ($OCAF_H$) in the data lines and reproduce the bit phase of the samples based on the phase information.

Since the input data is converted into 8-bit parallel data at the appropriate phase, there are 8 possible phases. The sync pattern consists of 16 bits and so if a 23-bit pattern is involved, as shown in Fig. 5-6, the sync pattern can be extracted and the phase detected. In actual fact, it is hard to check a 23-bit pattern at the same time and so the check is done after the 23 bits have been divided into 3 blocks of 7 bits, 9 bits and 7 bits. Based on the coincidence information ("0 ERROR": all bits coincide; "1 ERROR": non-coincidence of 1 bit only; "A0/A1/A2": phases 0 — 7 with possibility) which is checked in each respective block, signals totaling 5 bits — "SYNC 0 ERROR" denoting that all bits coincide, "SYNC 1 ERROR" denoting that only 1 bit is does not coincide and "SYNC PHASE: 3BITS" phase information — are output. For instance, with a section such as the data section in which the sync pattern cannot be detected, the previous phase information is kept.

### (2) Bit phase reproducing circuit (SY-70 board)

The 8-bit parallel data and the "SYNC PHASE" phase information detected by the sync pattern detector are supplied to the bit rotate IC ICC13 (CX20149).

In this circuit, the data corresponding to the 8 phases is generated from the input data, and the data is selected in accordance with the detected phase information and output. This causes the input data to return to the regular bit phase.

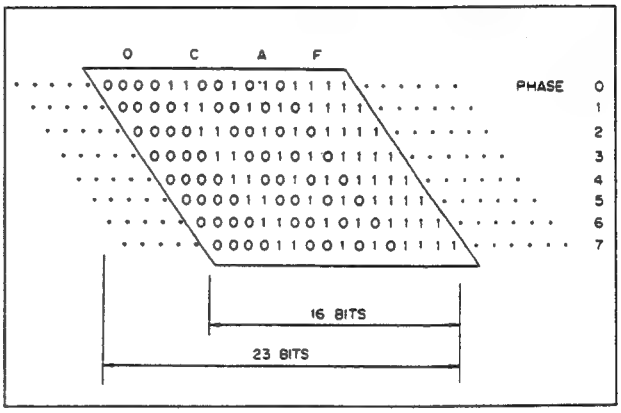



**Fig. 5-6. Sync Pattern (SY-70 Board)**



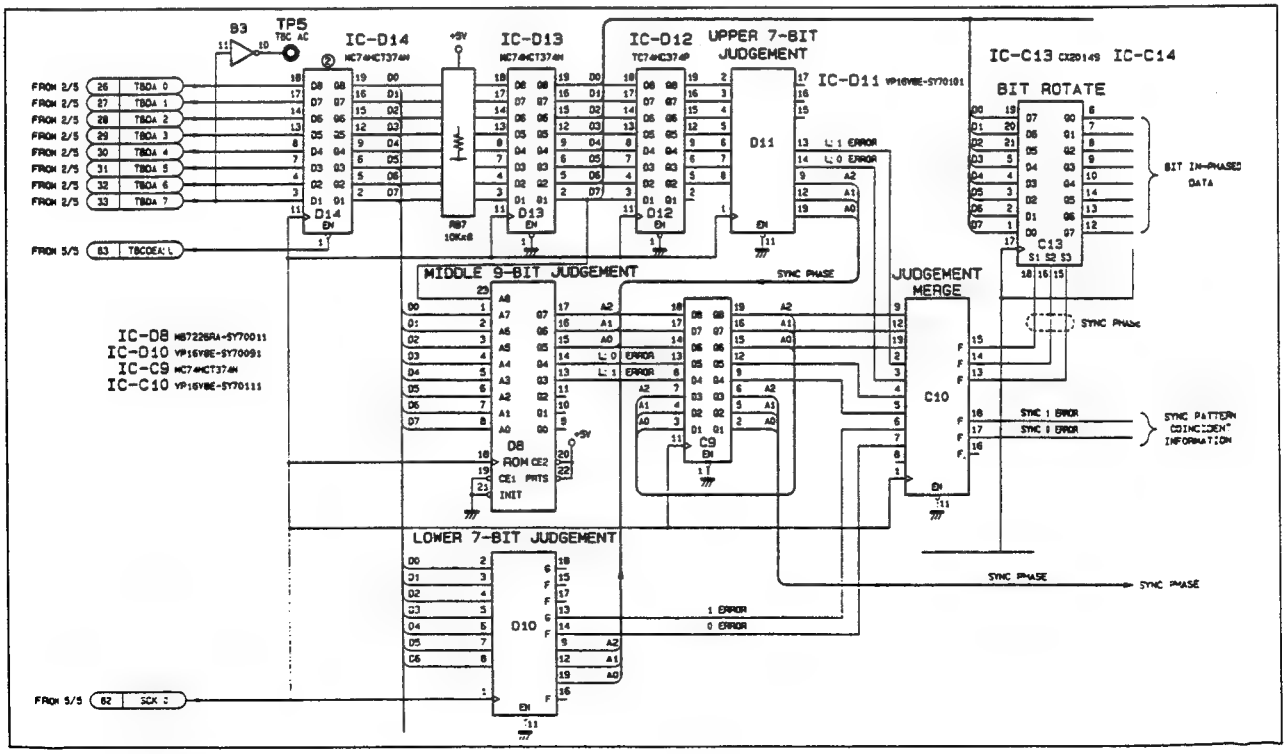



**Fig. 5-7. Sync Bit Pattern Detector (SY-70 Board)**

**(3) Sync Judgement Circuit (SY-70 board)**

Based on the current coincidence information and the coincidence information of one sync block before and after, it is determined whether the currently judged data section is the sync pattern. This is done by ICB13 and G13. There are two sync pattern detection modes: the mode in which the sync pattern is detected (lock) and the mode in which the sync pattern is searched (unlock).

If two or more coincidences are detected among the coincidence information of 3 sync blocks used for judgement, the lock mode is established. If less than one coincidence is detected, the unlock mode is established.

In the normal playback mode or EE mode, a window is provided in the lock mode so as to safeguard against error detection, and when the next sync arrives, only the coincidence information at the projected position (1 sync block = 134 samples) is taken for judgement. Furthermore, in the normal playback mode or EE mode, up to 4 flywheel sync signals are added when errors temporarily arise in the sync.

In the high-speed shuttle mode, the lock/unlock information is not used.

**(4) ID extractor and ID judgement circuit (SY-70 board)**

As with the sync judgement, whether the ID is correct or not and which ID should be selected are judged from the continuity of the addresses.

Since the addresses expressed by 4-bit nibbles are 4-8 mapped and recorded onto tape, on the SY-70 board they are de-mapped into 4-bit addresses having a number system with a radix of 14. During de-mapping, a check is simultaneously conducted to see whether these addresses are the defined values, and they are sent to the ID judgement circuit as the error information of the addresses.

Next, the coincidence of the field ID/sector ID between the 3 sync blocks as well as the block ID continuity are checked, and the results are sent to the ID judgement circuit.

Based on the ID error information and the continuity of the addresses between the 3 sync blocks, the "*IDOK" information as to whether the ID is ultimately correct and the "ADPH" address phase information as to which address is to be selected are output in the ID judgement circuit.

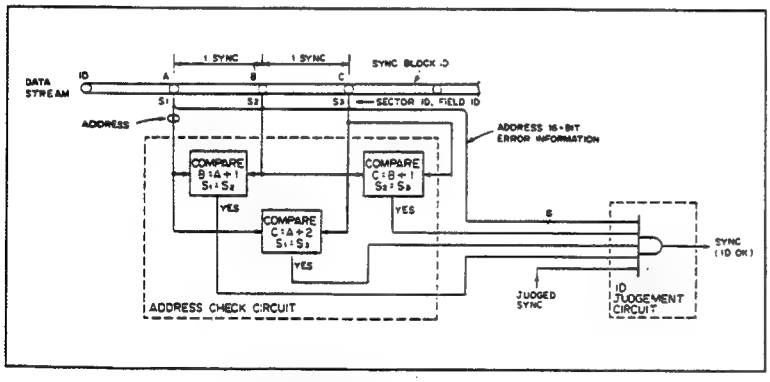



**Fig. 5-8. ID Judgement Algorithm (SY-70 Board)**

| INPUT | | OUTPUT | INPUT | | OUTPUT |
|---|---|---|---|---|---|
| 1B | | 0 | 96 | | 8 |
| 2E | | 1 | A3 | | 9 |
| 35 | | 2 | B8 | | A |
| 47 | ⇨ | 3 | CA | ⇨ | B |
| 5C | | 4 | D1 | | C |
| 69 | | 5 | E4 | | D |
| 72 | | 6 | | | |
| 8D | | 7 | | | |

VALUES EXPRESSED IN HEXADECIMAL.

**Table 5-1. 4-8 De-mapping (SY-70 Board)**

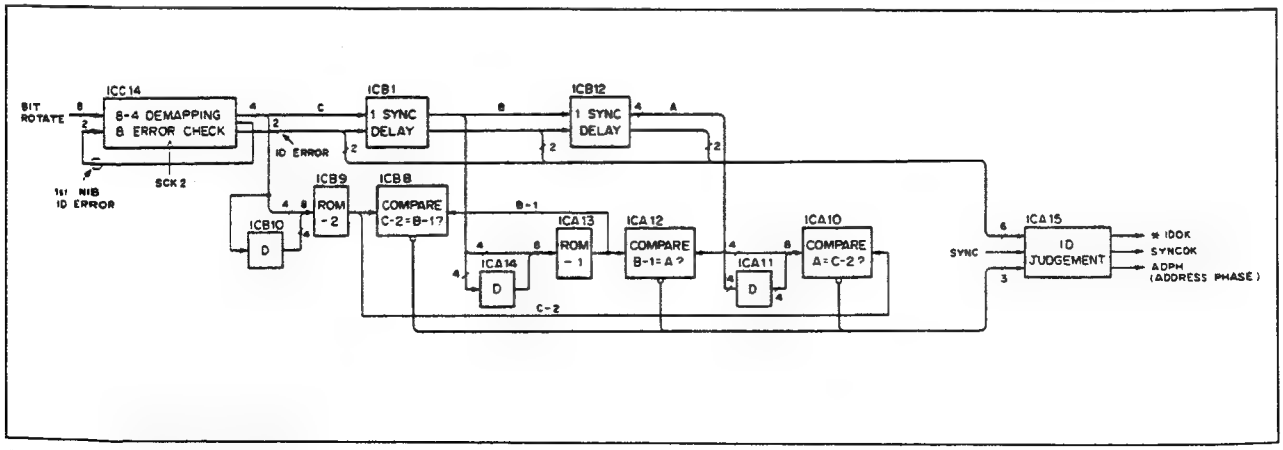



**Fig. 5-9. ID Judgement Circuit (SY-70 Board)**

**(5) ID converter and error flag adder (SY-70 board)**

The processes listed below are carried out in accordance with the phase of counter ICB4 which is initialized by the "SYNCOK" signal.

- Field ID/sector ID/block ID latching and selection
- Addition of flywheel ID according to tape speed
- Conversion to internal format ID
- Insertion of ID/ID error flags into data line

ROM ICC1, which is used for ID conversion, error flag generation and flywheel generation, is divided internally into 8 areas, and the areas are selected in accordance with the phase of the counter.

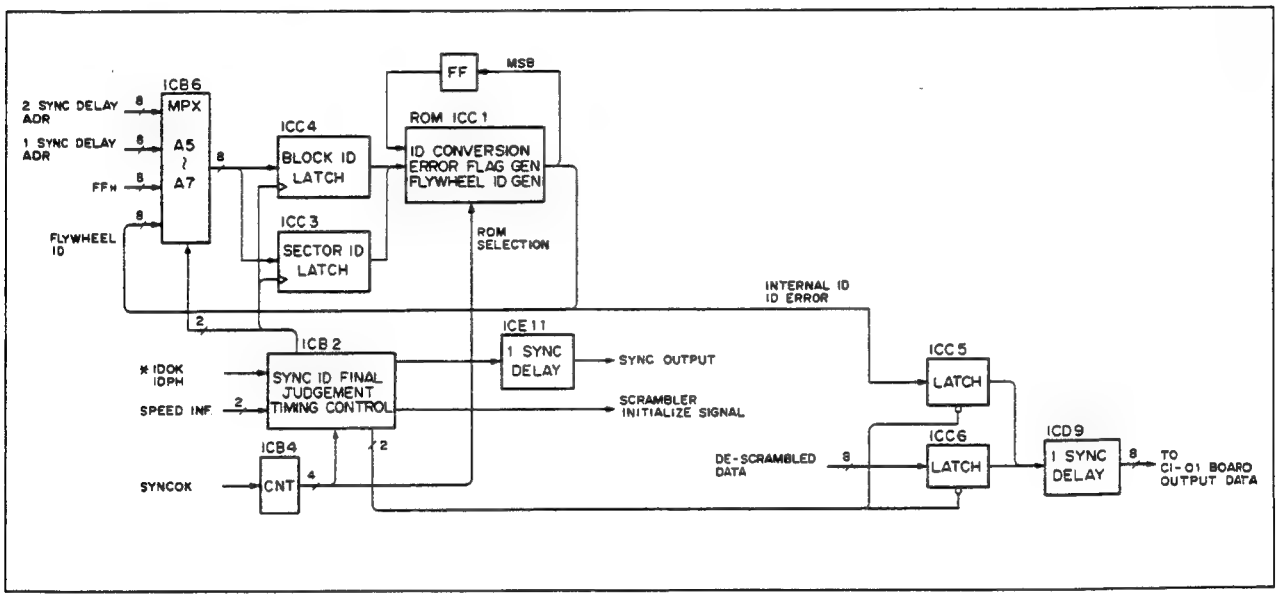
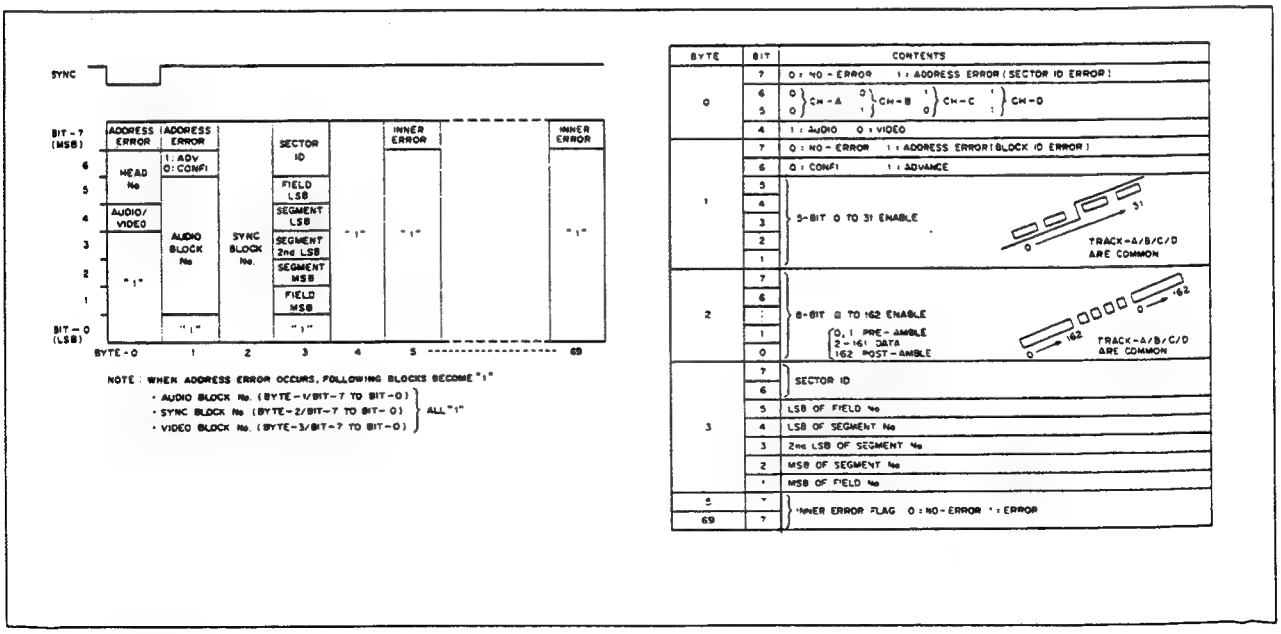



**Fig. 5-10. ID Converter and Error Flag Adder (SY-70 Board)**




| BYTE | BIT | CONTENTS |
|---|---|---|
| 0 | 7 | 0 : NO - ERROR 1 : ADDRESS ERROR (SECTOR ID ERROR) |
| | 6, 5 | CH-A / CH-B / CH-C / CH-D |
| | 4 | 1 : AUDIO 0 : VIDEO |
| 1 | 7 | 0 : NO - ERROR 1 : ADDRESS ERROR (BLOCK ID ERROR) |
| | 6 | 0 : CONFI 1 : ADVANCE |
| | 5 - 1 | 5-BIT 0 TO 31 ENABLE |
| 2 | 7 - 0 | 8-BIT 0 TO 162 ENABLE (0, 1 PRE-AMBLE; 2-161 DATA; 162 POST-AMBLE) |
| 3 | 7, 6 | SECTOR ID |
| | 5 | LSB OF FIELD No |
| | 4 | LSB OF SEGMENT No |
| | 3 | 2nd LSB OF SEGMENT No |
| | 2 | MSB OF SEGMENT No |
| | 1 | MSB OF FIELD No |
| 4 - 68 | 7 | INNER ERROR FLAG 0 : NO-ERROR 1 : ERROR |

**Fig. 5-11. Internal ID Format (SY-70 Board)**

## 6. De-scrambler (SY-70 board)

On the IE-17 board of the recording system, the recording data and dummy random signals are exclusive OR-ed, and the recording data is randomized. This circuit does the reverse processing.
The dummy random data is output in sequence from the ROM which generates the random data, this data and the playback data are exclusive OR-ed and the original data is reproduced. The sync and ID are not scrambled and so they are not processed here.

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00, | 00. | 71. | E2. | 93. | B5. | C4. | 57. | 26. | 1B. | 6A. | F9. | 88. | AE. | DF. | 4C. | 3D. |
| 10, | 47. | 36. | A5. | D4. | F2. | 83. | 10. | 61. | 5C. | 2D. | 8E. | CF. | E9. | 98. | 0B. | 7A. |
| 20, | 8E. | FF. | 6C. | 1D. | 3B. | 4A. | D9. | A8. | 95. | E4. | 77. | 06. | 20. | 51. | C2. | B3. |
| 30, | C9. | B8. | 2B. | 5A. | 7C. | 0D. | 9E. | EF. | D2. | A3. | 30. | 41. | 67. | 16. | 85. | F4. |
| 40, | 1C. | 6D. | FE. | 8F. | A9. | D8. | 4B. | 3A. | 07. | 76. | E5. | 94. | B2. | C3. | 50. | 21. |
| 50, | 58. | 2A. | B9. | C8. | EB. | 9F. | 0C. | 7D. | 40. | 31. | A2. | D3. | F5. | B4. | 17. | 66. |
| 60, | 92. | E3. | 70. | 01. | 27. | 56. | C5. | B4. | 89. | F8. | 6B. | 1A. | 3C. | 4D. | DE. | AF. |
| 70, | D5. | A4. | 37. | 46. | 60. | 11. | 82. | F3. | CE. | 9F. | 2C. | 5D. | 7B. | 0A. | 99. | E8. |
| 80, | 38. | 49. | DA. | AB. | 8D. | FC. | 6F. | 1E. | 23. | 52. | C1. | B0. | 96. | E7. | 74. | 05. |
| 90, | 7A. | 0B. | 9D. | EC. | CA. | BB. | 2B. | 59. | 64. | 15. | 86. | F7. | D1. | A0. | 33. | 42. |
| A0, | 86. | C7. | 54. | 25. | 03. | 72. | E1. | 90. | AD. | DC. | 4F. | 3E. | 18. | 69. | FA. | 8B. |
| B0, | F1. | 80. | 13. | 62. | 44. | 35. | A6. | D7. | EA. | 9B. | 08. | 79. | 5F. | 2E. | BD. | CC. |
| C0, | 24. | 55. | 06. | 67. | 91. | E0. | 73. | 02. | 3F. | 4E. | DD. | AC. | 8A. | FB. | 68. | 19. |
| D0, | 63. | 12. | 81. | F0. | D6. | A7. | 34. | 45. | 78. | 09. | 9A. | EB. | CD. | BC. | 2F. | 5E. |
| E0, | AA. | D8. | 48. | 39. | 1F. | 6E. | FD. | 8C. | B1. | C0. | 53. | 22. | 04. | 75. | E6. | 97. |
| F0, | ED. | 9C. | 0F. | 7E. | 58. | 29. | 8A. | CB. | F6. | 87. | 14. | 65. | 43. | 32. | A1. | D0. |

**Fig. 5-12. De-scramble Sequence (SY-70 Board)**

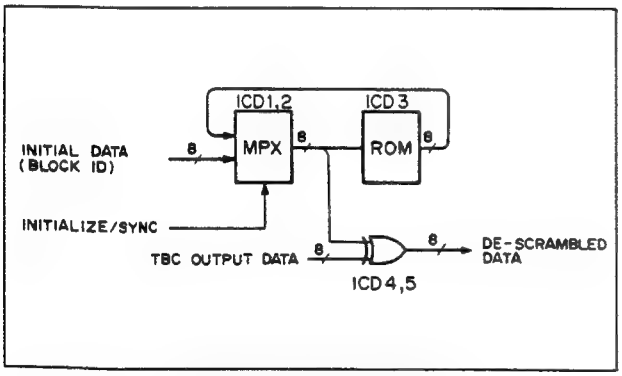



**Fig. 5-13. De-scramble Circuit (SY-70 Board)**

## 4-6. CI-01 BOARD

The CI-01 board is composed of the following circuits.

**Circuits common to video and audio signals**
- Inner decoder (The same circuit is used for all 4 channels.)
- Channel exchanger

**Audio system circuits**
- Audio 2-write memory
- Audio LIP sync memory (Audio de-shuffle memory)
- Audio outer decoder

After processing on the SY-70 board, the playback parallel data and sync signals for all 4 channels are supplied to the CI-01 board. The data supplied to this board first enters the inner decoder where any errors are corrected using the inner error code. Error flags are added for those data whose errors cannot be corrected.
After error correction, the data is supplied to the channel exchanger. This assigns the data, which has been played back from the multiple number of heads during stunt playback, to the original channel line and it processes this data.
Until this stage, the video data and audio data are multiplexed and processed but in the subsequent circuitry they are processed separately.
The separated video data is sent to the FM-09 board together with the sync signal.

The audio data, on the other hand, is sent to the audio 2-write memory where the original data and copy data are compared, and error-free data is selected and output to the LIP sync memory (audio de-shuffle memory).
The A/B/C/D channels data are written into the LIP sync memory by time division and processed in subsequent circuitry as a single set of data. The delay is adjusted so that the output phases of the video data and audio data are aligned. Audio data de-shuffling is also done at the same time. The CONFI head playback data and ADVANCE head playback data are read out alternately from the LIP sync memory and are sent to the audio outer decoder.
After any errors are corrected by the audio outer decoder, the audio data is output together with any error flags to the AP-14 board.
The inner encoder output data of the IE-17 board is supplied as the test signal (BYPASS-3) to the inner decoder of the CI-01 board.



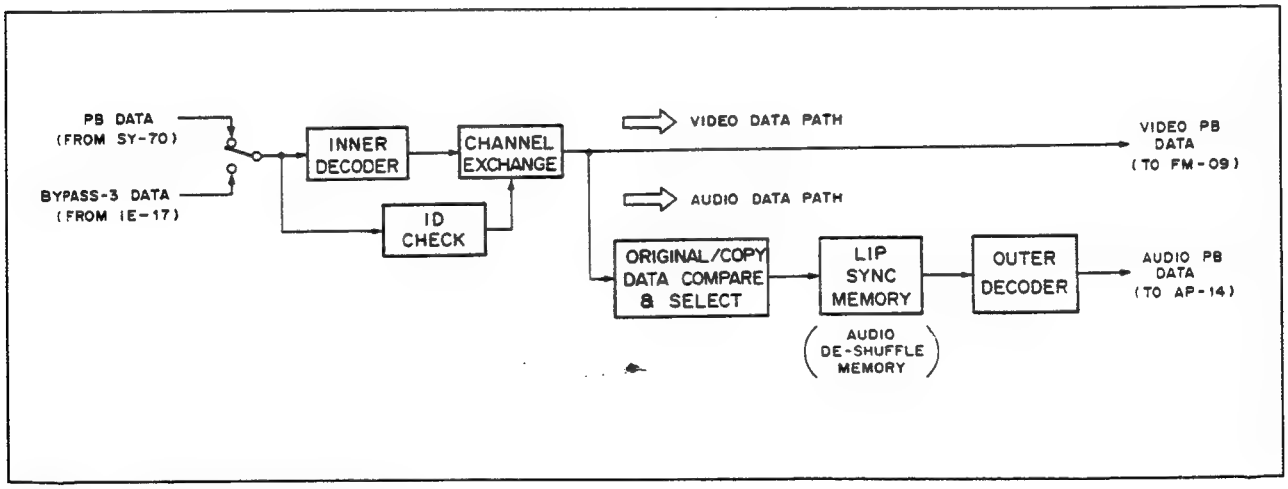



**Fig. 6-1. Function Diagram (CI-01 Board)**

**1. Inner decoder (CI-01 board)**

- Galois field: GF(256)
- Field generating polynomial:
  $P(X) = X^8+X^4+X^3+X^2+1$
- Code generating polynomial:
  $G(X) = (X+\alpha^0)(X+\alpha)(X+\alpha^2)(X+\alpha^3)$
  $= X^4+\alpha^{75}X^3+\alpha^{249}X^2+\alpha^{78}X+\alpha^6$
  $\alpha^0$, $\alpha$, $\alpha^2$ and $\alpha^3$ are the roots of G(X).
- Companion matrix

$$\alpha = \begin{vmatrix} 0&1&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0 \\ 1&0&0&0&1&0&0&0 \\ 1&0&0&0&0&1&0&0 \\ 1&0&0&0&0&0&1&0 \\ 0&0&0&0&0&0&0&1 \\ 1&0&0&0&0&0&0&0 \end{vmatrix}$$

The inner decoder uses the (64,60) Reed Solomon code determined by the above formula. Up to 2 samples can be corrected with this code.
If it is assumed that "i" and "j" are the error positions and "ei" and "ej" are the error sizes, then syndromes S0, S1, S2 and S3 will be as follows:

$S0 = ei+ej$
$S1 = \alpha^i ei+\alpha^j ej$
$S2 = \alpha^{2i} ei+\alpha^{2j} ej$
$S3 = \alpha^{3i} ei+\alpha^{3j} ej$

In order for erasures to be corrected by the outer decoder, the inner decoder provides 1-sample correction and the remaining redundancy is used for error detection. This means that the syndromes for 1-sample corrections will be as follows:

$S0 = ei$
$S1 = \alpha^i ei$
$S2 = \alpha^{2i} ei$
$S3 = \alpha^{3i} ei$

The error size and position can be determined from the above formulae as follows:

$ei = S0$
$\alpha^i = S1/ei = S1/S0$

Sony's IC CXD1038G (ICK16, K17, K25, K35) is used for the inner decoder. The correction mode (CMB, CMC, OSA, OSB) is designated by the universal peripheral interface (UPI: ICA38). The ID section is not encoded and so only the ID is extracted from the data line, the encoder is bypassed and it is inserted into the encoder output data. The data of which channel is being processed is detected from the extracted ID, and the "CHARQ, CHBRQ, CHCRQ, CHDRQ" channel exchanger control signals are supplied.

**2. Channel exchanger (CI-01 board)**

During stunt playback the various heads cross over the tracks and so the data of one track is played back from a multiple number of heads. This means that the data of track A is played back not merely by head A but also by heads B, C and D. In order to output from the multiple number of heads the data which has been played back fragmentarily as the data for a single screen, the data from each head must be returned to its respective original channel lines, and it is in the channel exchanger that it is exchanged with the channel data.
The sync signal is further added to the data which has been assigned to the proper channel, and the video data is output to the FM-09 board while the audio data is output to the audio 2-write memory.

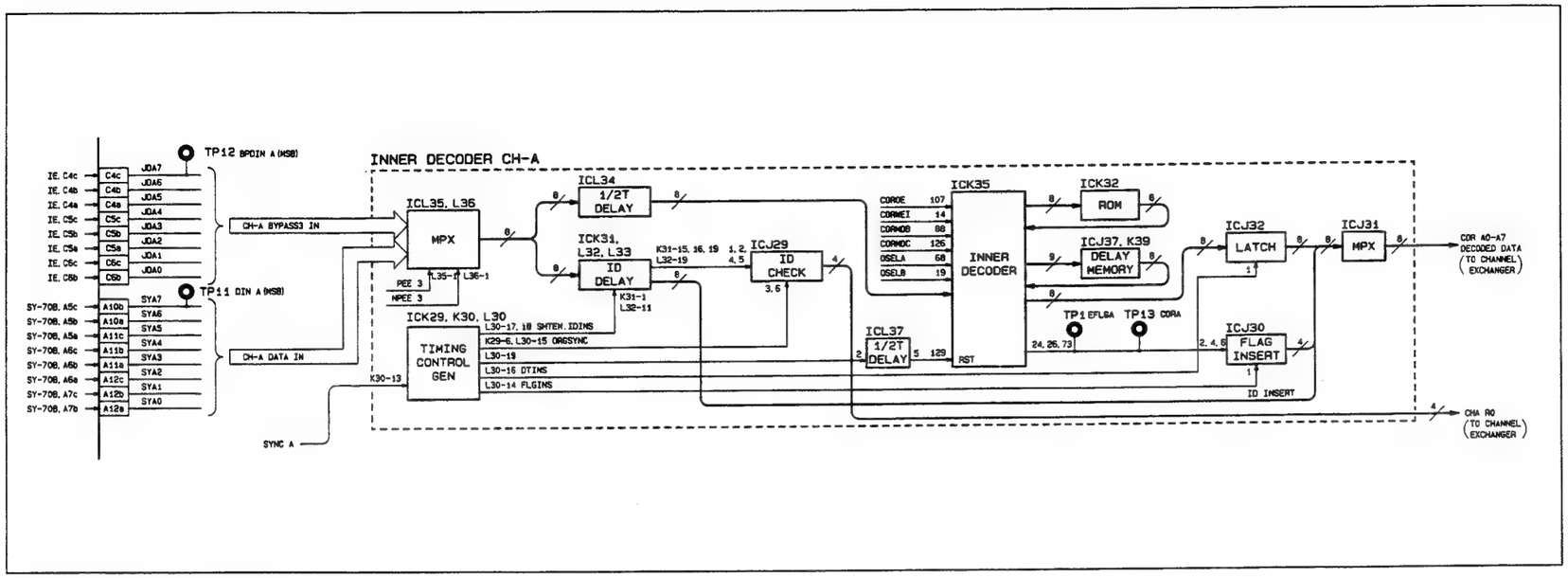



Fig. 6-2. Inner Decoder (CI-01 Board)

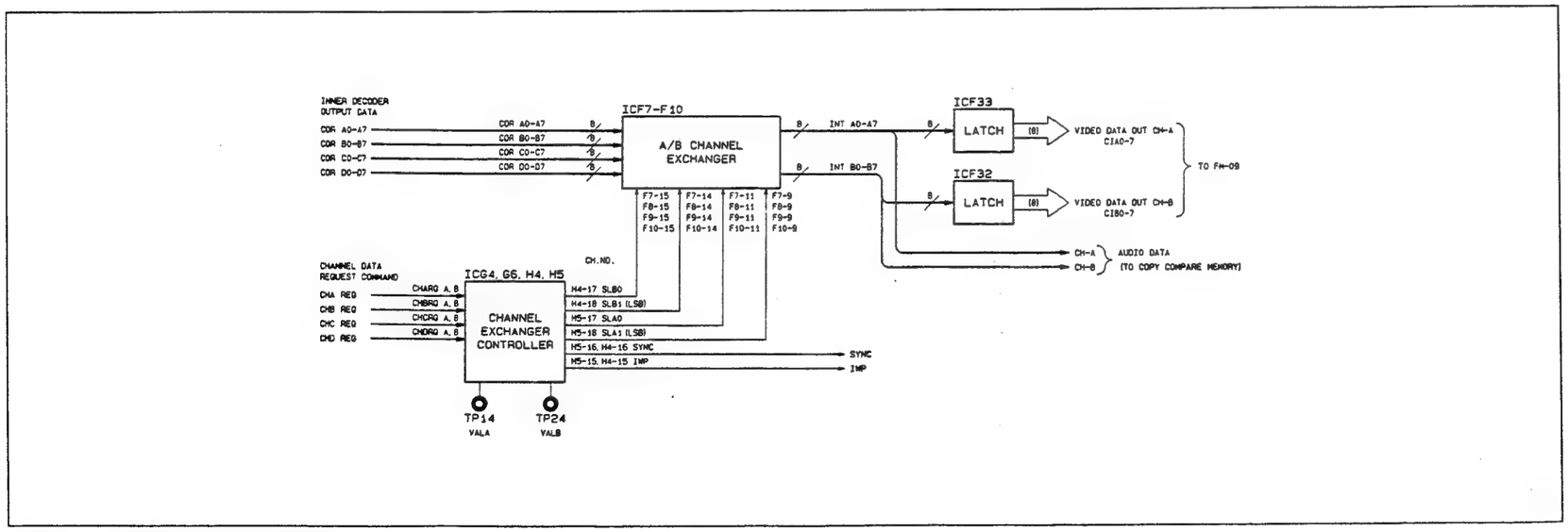



Fig. 6-3. Channel Exchanger (CI-01 Board)

### 3. Audio 2-write memory (CI-01 board)

As shown by Fig. 6-4, the audio data is duplicated onto two different tracks and recorded. This means that even when two neighboring channels cannot be used at all due to head clogging, the original data can be completely reproduced without error correction and error concealment, provided that there are no errors in the other two channels.

In the audio 2-write memory, the original data and copy data are compared, and the correct data is output to the LIP sync memory. At the write side, the timing control section is initialized by the sync signal which has been extracted by the SY-70 board and, at the same time, the address generating counter inside the sync block is reset. Next, the block ID in the data lines is extracted. This block ID is held until the next signal sync is supplied. In order to facilitate control over data reading, data equivalent to 128 samples (minus first 2 or last 4) of the 134 samples (1 sync block) and the ID are written into the memory.

The memory read addresses are generated from the counter which is initialized by the "SEGTOP" segment top signal. The data written in the memory is read out at the timing shown by Fig. 6-5 and compared in sequence.

The original data and copy data differ in the ELAP (EDIT OVERLAP) section and so selection cannot rely on the same method used for other data section. This means that when the ELAP flags have been raised, one set of data will be selected uniformly.

When the internal error flag is in the error status for both the original data and copy data, the error flag is raised and the data is output to the LIP sync memory. The sector ID is extracted and output to the LIP sync memory.

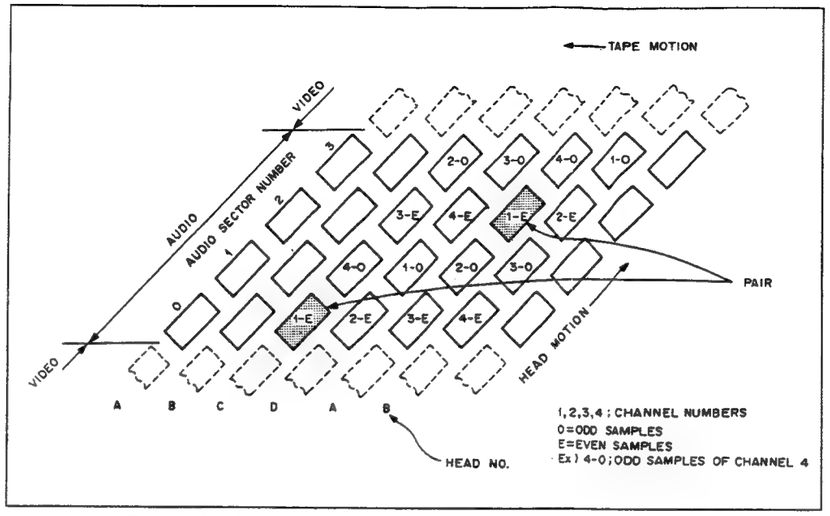



Fig. 6-4. Tape Format (CI-01 Board)

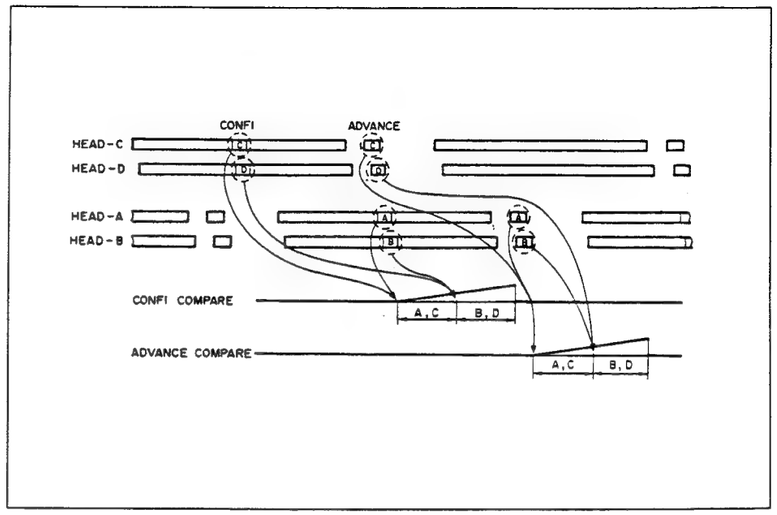



Fig. 6-5. Data Read Timing Chart (CI-01 Board)

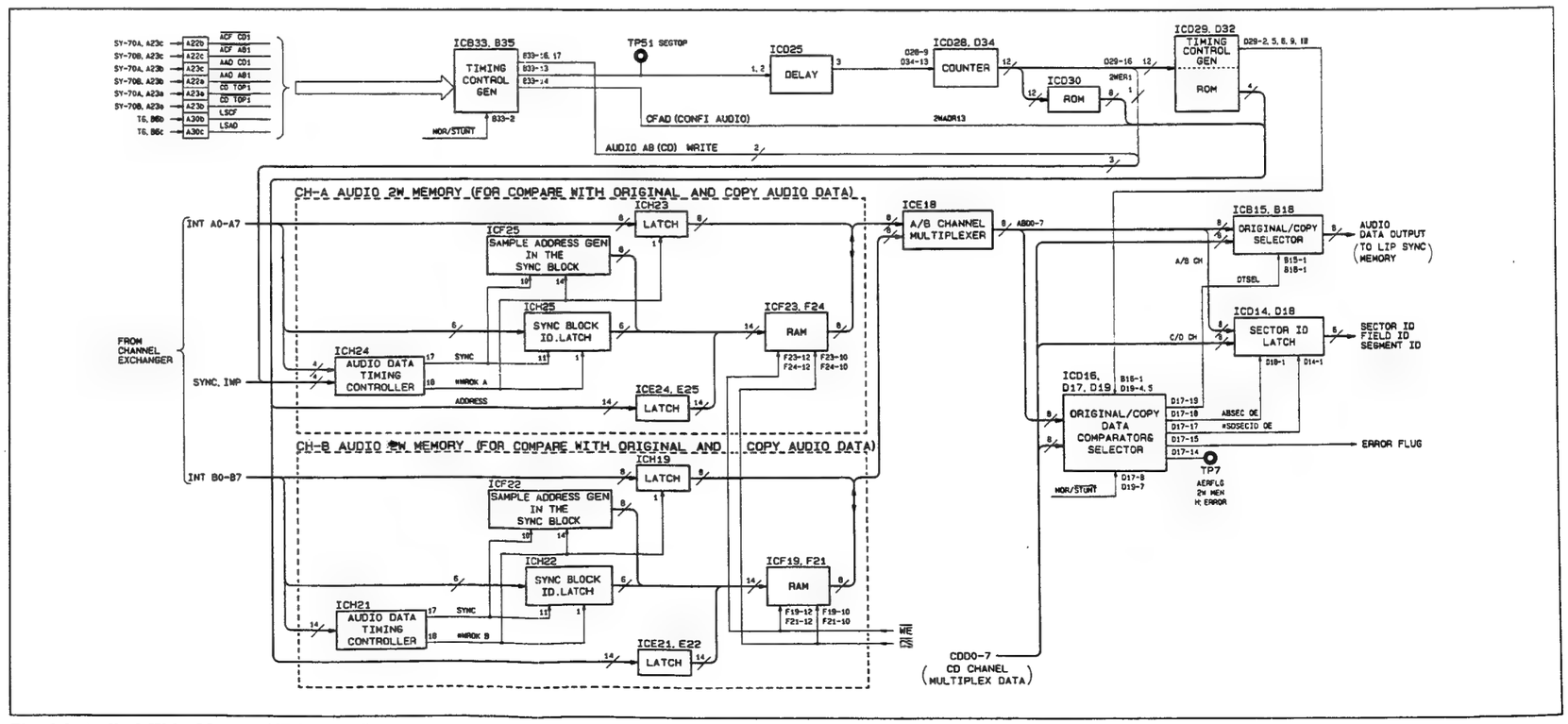



Fig. 6-6. Audio 2-Write Memory (CI-01 Board)

### 4. Audio LIP sync memory (CI-01 board)

This circuit is a frame memory for aligning the phases of the video data and audio data. It also de-shuffles the audio data at the same time. The audio shuffling size is 1 segment (160 or 161 samples).

The memory write addresses are initialized by the "SEGTOP" segment top signal, the sector ID is then referenced and the data is written in the prescribed address.

Readout is commenced by the "LSCF" and "LSAD" signals supplied from the TG-28 board. However, since the interval with the outer 10 samples does not coincide with the frame interval, the frame pulse is latched again by the free-running decimal counter, and the "CONF TOP" and "ADV TOP" CONFI and ADVANCE read start signals are created respectively.

The data for CONFI head playback and ADVANCE head playback are read out alternately one outer code block at a time from the LIP sync memory. During read out, the addresses are converted by the de-shuffling ROMs provided for CONFI and ADVANCE, and de-shuffling is done.

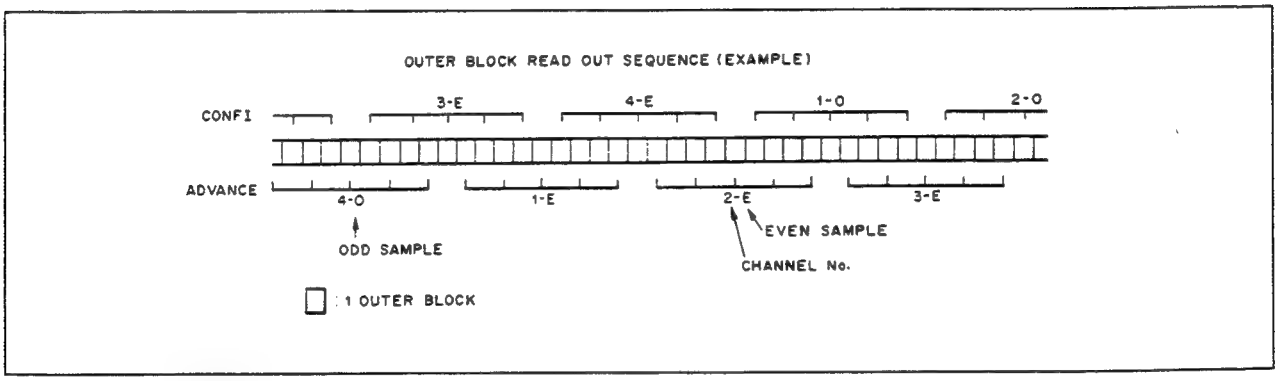



**Fig. 6-7. LIP Sync Memory Read Timing (CI-01 Board)**

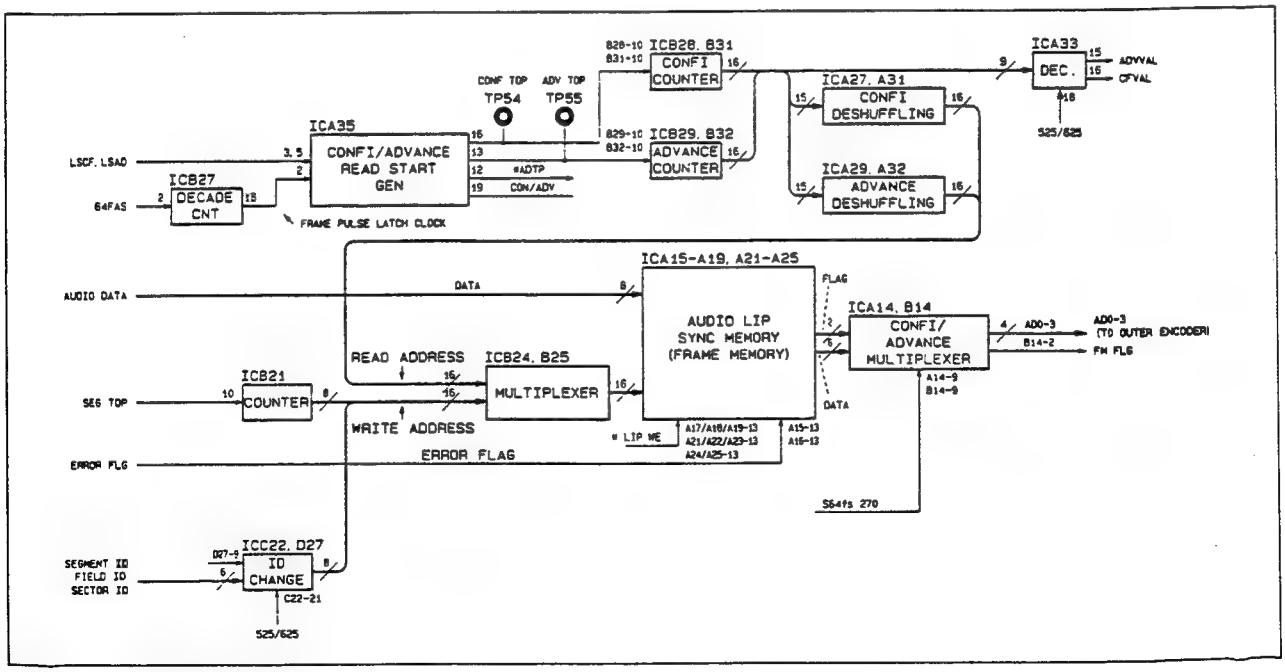



**Fig. 6-8. LIP Sync Memory (CI-01 Board)**

## 5. Audio outer decoder (CI-01 board)

- Galois field: GF(16)
- Field generating polynomial: $P(X) = X^4+X+1$
- Code generating polynomial:
  $G(X) = (X+\alpha^0)(X+\alpha)(X+\alpha^2)$
  $\alpha^0$, $\alpha$ and $\alpha^2$ are the roots of G(X).
- Companion matrix

$$\alpha = \begin{vmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \end{vmatrix}$$

The audio outer decoder uses the (10,7) Reed Solomon code determined by the above formula. This code enables erasure correction of up to 3 samples.
If it is assumed that "i," "j" and "k" are the error positions and "ei," "ej" and "ek" are the error sizes, then syndromes S0, S1, and S2 will be as follows:

$S0 = ei+ej+ek$
$S1 = \alpha^i ei+\alpha^j ej+\alpha^k ek$
$S2 = \alpha^{2i} ei+\alpha^{2j} ej+\alpha^{2k} ek$

When this equation with three unknowns is solved, the error sizes will be as follows:

$$ei = \frac{S0\alpha^{j+k}+S1(\alpha^j+\alpha^k)+S2}{(\alpha^i+\alpha^j)(\alpha^i+\alpha^k)}$$

$$\cdot ej = \frac{S0\alpha^{i+k}+S1(\alpha^i+\alpha^k)+S2}{(\alpha^i+\alpha^j)(\alpha^j+\alpha^k)}$$

$$ek = \frac{S0\alpha^{i+j}+S1(\alpha^i+\alpha^j)+S2}{(\alpha^i+\alpha^k)(\alpha^j+\alpha^k)}$$

The error positions are detected by the inner decoder and so the error sizes are calculated, these sizes and the playback data are exclusively OR-ed and the proper data is sought.

**(1) Error pattern calculation (CI-01 board)**
In the error pattern operator, error sizes "ei," "ej" and "ek" are sought from syndromes S0, S1 and S3 and from the erasure flags.

**(2) Error correction (CI-01 board)**
In the error corrector, the playback data and the error sizes "ei," "ej" and "ek" sought by the error pattern operator are exclusively OR-ed, and the errors are corrected.

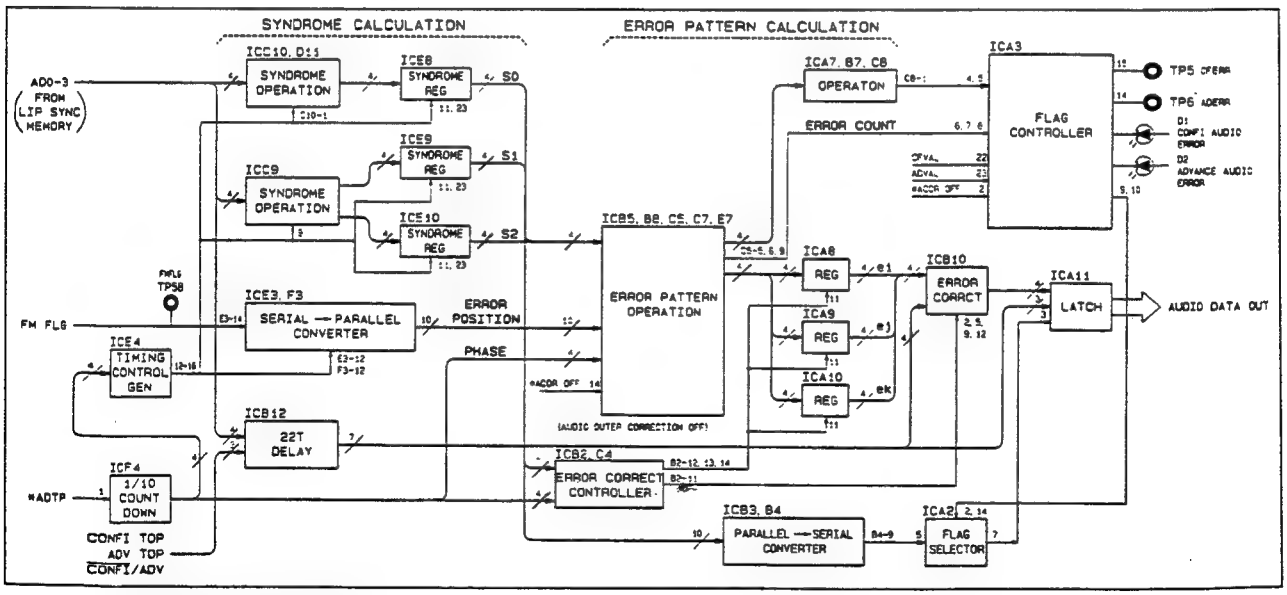



**Fig. 6-9. Outer Decoder (CI-01 Board)**

## 4-7. TG-28 BOARD

The TG-28 board may come with any of the following board number suffixes: "−11," "−12," "−13" or "−14." The configuration of the circuits is partially different for boards with the "−11/12/13" suffixes and for boards with the "−14" suffix. Whereas section 4-7-1 describes the TG-28 board with the "−11/12/13" suffixes, section 4-7-2 describes how the TG-28 board with the "−14" suffix differs from boards with the other 3 suffixes.

### 4-7-1. TG-28 Board (Board Number Suffix: −11/12/13)

This description applies only to those TG-28 boards with the "−11/12/13" suffixes.

The TG-28 board selects one of the following 4 types of input sync signals and it generates most of the timing signals required by the DVPC-1000.

- Sync signal which is separated from the digital video input signal
- Sync signal which is supplied through the DIGITAL REFERENCE INPUT connector
- Sync signal which is separated from the analog video input signal
- Sync signal which is supplied through the ANALOG REFERENCE INPUT connector

The TG-28 board is also provided with the following 4 PLL circuits for generating the timing signals.

PLL1: This generates the 27 MHz clock signal for processing the recording system video signals.

PLL2: This generates the 12.288 MHz clock signal for processing the audio signals.

PLL3: This generates the composite sync signal. (14.318 MHz for 525/60 system; 14.815 MHz for 625/50 system)

PLL4: This generates the 27 MHz clock signal for processing the playback system video signals.

The recording system timing signals include the video and audio shuffling memory read signals, the recording gate signals corresponding to the edit preset channels required for insert editing and spot eraseing, and the SELECTED EE signals, AUTO EDIT commands and SPOT ERASE commands required for preview operations. The playback system timing signals include the playback head output timing signals, frame memory read start signals, LIP sync memory read start signals and playback 5-frame signals. At the end of this section there is a brief description of each of the TG-28 board input/output signals.

The TG-28 board also provides interfacing with the DVR-1000. On the one hand, the servo frame pulse, audio frame pulse and color frame pulse are output from the DVPC-1000. On the other hand, the playback audio frame pulse and playback color frame pulse are supplied from the DVR-1000 to the DVPC-1000.



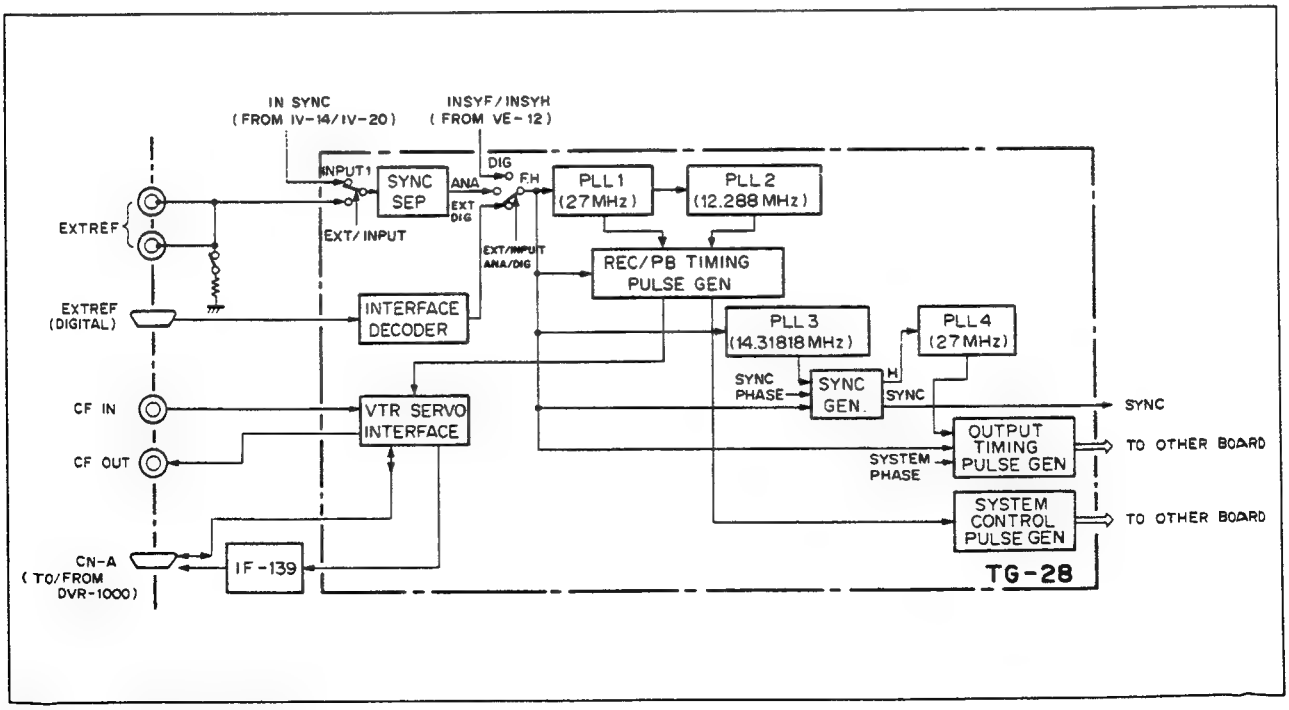



**Fig. 7-1-1. Function Diagram (TG-28 Board)**

### 1. Frame pulse/H pulse separator (ICA24, A25, A27/TG-28 board)

One of the following two types of composite sync signals is selected by ICC27 and supplied to the pulse separator.

- The composite sync signal which is first separated from the black burst or composite sync signal supplied to the ANALOG REFERENCE INPUT connector and then converted to the TTL level.
- The composite sync signal which is separated from the input video signal in the IV-14 (IV-20) board.

In this circuit, the frame pulse and H pulse are separated from the input composite sync and output. The frame pulse is output from pin 5 of ICA25 while the H pulse is output from pin 4 of ICA27. Fig. 7-1-2 shows the separation timing of the pulses and Fig. 7-1-3 shows the output frame pulse timing.

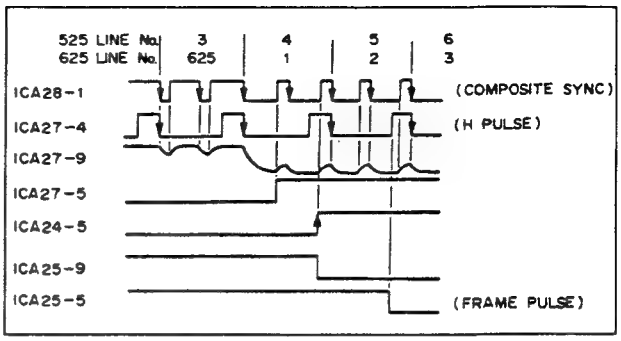



**Fig. 7-1-2. Frame Pulse/H Pulse Separation (TG-28 Board)**

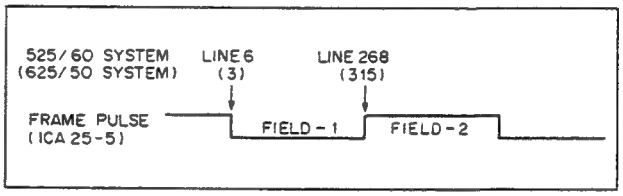



**Fig. 7-1-3. Frame Pulse Output Timing (TG-28 Board)**

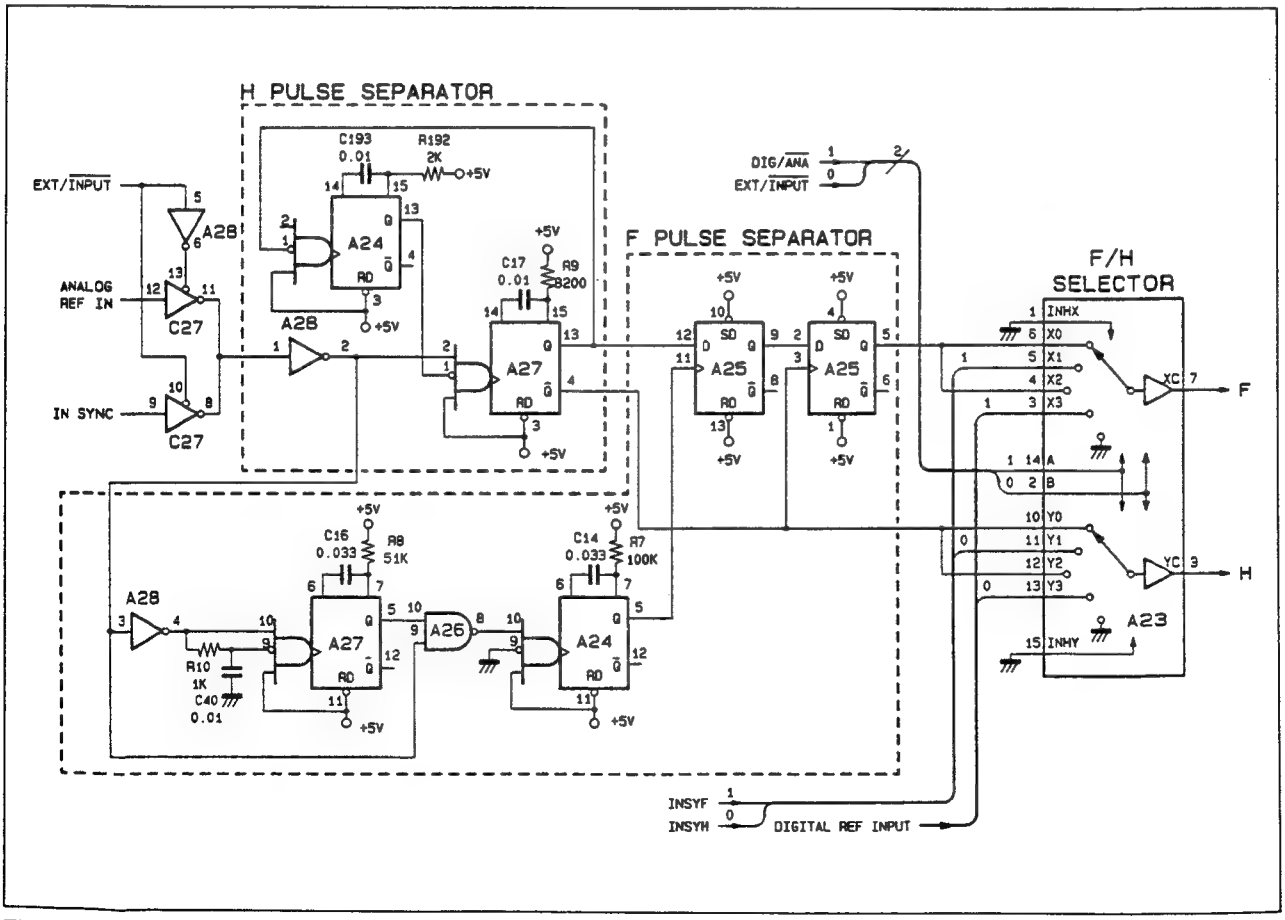



**Fig. 7-1-4. Frame Pulse/H Pulse Separator (TG-28 Board)**

## 2. Frame pulse Regenerator (ICC1, D2, F3/TG-28 board)

Frame pulses are output to enable simple playback even when the reference sync signal is not being supplied to the DVPC-1000.

Using the "SYSTEM H" H pulse from PLL1, this circuit serves to output from pin 10 of ICF3 either the frame pulse for the 525/60 system which falls at line 5 and rises at line 267 or the frame pulse for the 625/50 system which falls at line 2 and rises at line 314.

This frame pulse is shifted one line by ICK30, and either the frame pulse for the 525/60 system which falls at line 6 and rises at line 268 or the frame pulse for the 625/50 system which falls at line 3 and rises at line 315 is output from pin 10 of ICG28.

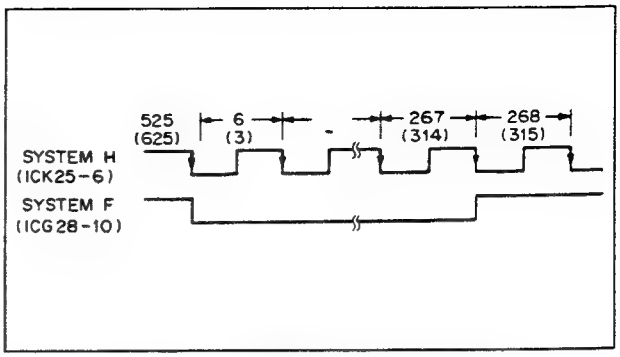



**Fig. 7-1-5. Frame Pulse Regeneration (TG-28 Board)**

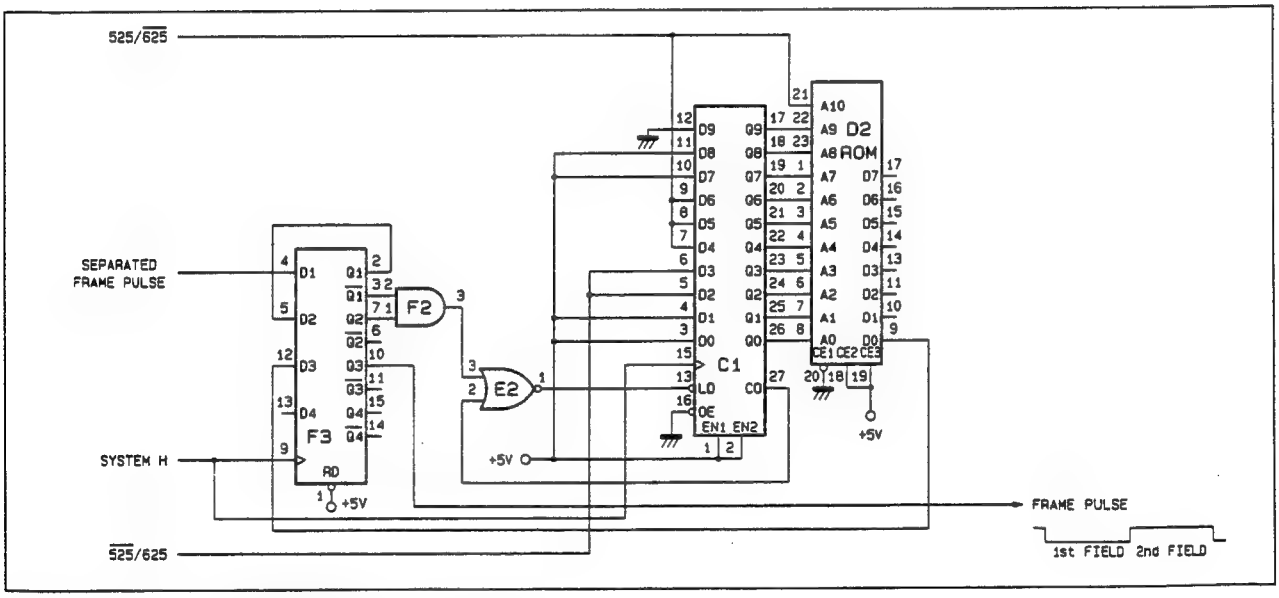



**Fig. 7-1-6. Frame Pulse Regenerator (TG-28 Board)**

### 3. System Detector (ICA21, B21, C21/TG-28 board)

The 525/60 system or 625/50 system is detected by the difference in the frame pulse period.
The frame pulse is supplied from pin 10 of ICF3 to pins 1 and 9 of monostable multivibrator ICA21. With the 525/60 system, the RV1 variable resistor has been adjusted so that the center of the low period of the pulse (TP23: ICA21 pin 9) created from the fall of the frame pulse and the rise of the monostable multivibrator output (TP24: ICA21 pin 4) will coincide. This means that the input signal system can be detected from the timing of both pulses.

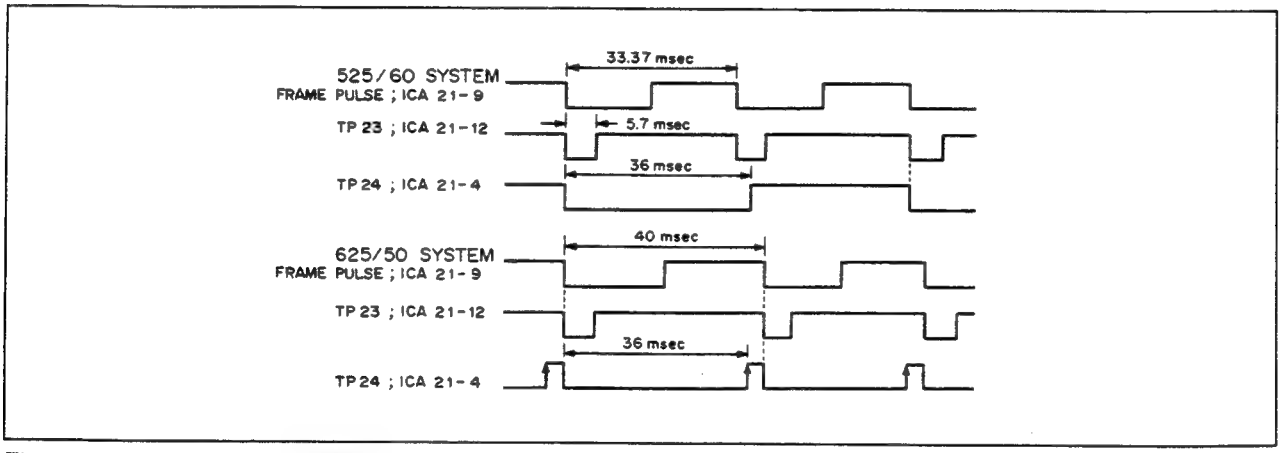



**Fig. 7-1-7. System Detection Timing (TG-28 Board)**

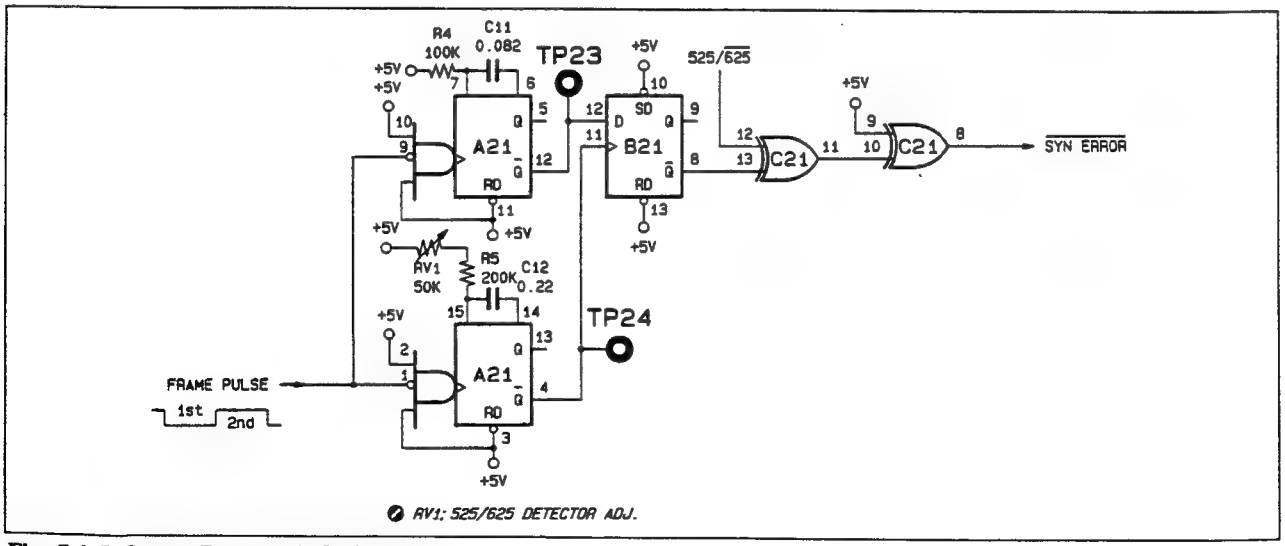



**Fig. 7-1-8. System Detector (TG-28 Board)**

### 4. PLL1 (TG-28 board)

Using the H pulse from the H pulse separator as the reference signal, this circuit creates the 13.5 MHz and 27 MHz clock signals as well as the SYSTEM H and SYSTEM 2H sync signals.

Sine waves with a frequency of 27 MHz are output from voltage-controlled crystal oscillator (VCXO) X7, and this signal has its waveform shaped into square waves by comparator ICH30 in the next stage.

After its waveform has been shaped, the 27 MHz clock signal has its frequency halved by ICG29, and it is then supplied to counter ICJ30 and to the toggling J-K flip-flop ICK30. In ICJ30 and ICK30, the 13.5 MHz clock signal "CK135" is further divided down by 858 (or by 864 for a 625/50 system), and it is fed back to phase comparator ICH25.

The $2xf_H$ clock signal "SYSTEM 2H" is output from pin 18 of ICJ30 to the audio PLL circuit (PLL2).

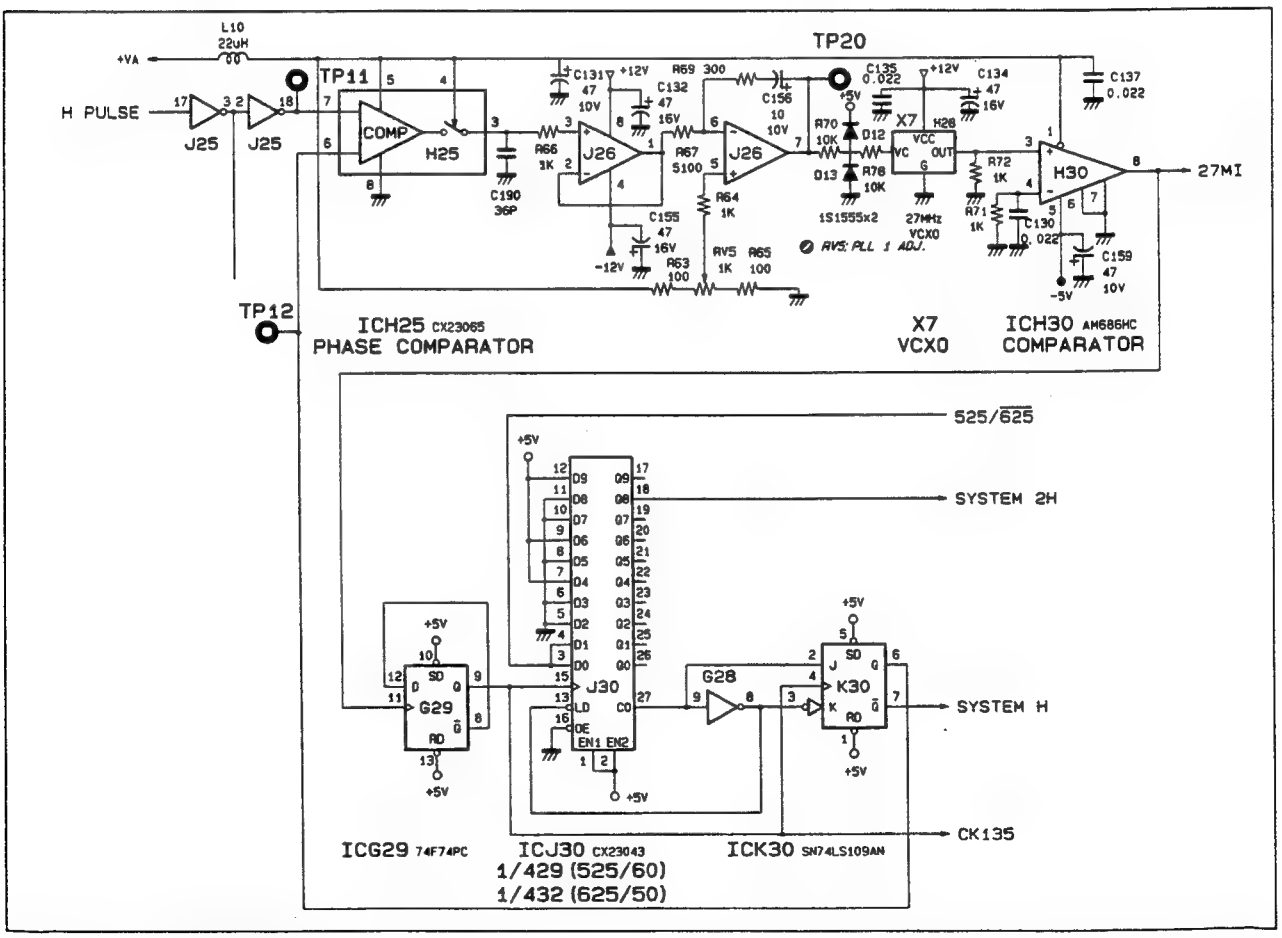



**Fig. 7-1-9. PLL1 (TG-28 Board)**

### 5. Track control pulse generator (TG-28 board)

This circuit generates the recording start pulses and playback start pulses depending on the rotational angle of the drum.
The 13.5 MHz clock signal supplied from the PLL1 circuit is divided down by 9 at counter ICJ22 which is initialized by the fall of the "SYSTEM F" frame pulse, and supplied to counter ICH22 and H24. This counter is similarly initialized by the fall of the "SYSTEM F", and the 1.5 MHz clock signal which is output from ICJ22 is divided down by 5005 (or by 5000 with the 625/50 system). This correspond to one half of a drum rotation.
The following timing pulses are output from NAND gate ICJ20 and K24 and PROM ICG22 which treats this counter output as an address.

- A/B TRST: This timing pulse determines the phase of the signal which is recorded onto track A.
- C/D TRST: This timing pulse determines the phase of the signal which is recorded onto track C.
- A/B CNFI: This timing pulse determines the start point of the track A playback RF signal, and it is output at the timing corresponding to the difference in the mounting angles of the REC and CONFI heads.
- C/D CNFI: This timing pulse determines the start point of the track C playback RF signal.
- AB TOP: This is the timing signal for cueing the RF playback signal, and it is 20 $\mu$sec ahead of the A/B CNFI signal.
- CD TOP: This is the timing signal for cueing the RF playback signal, and it is 20 $\mu$sec ahead of the C/D CNFI signal.

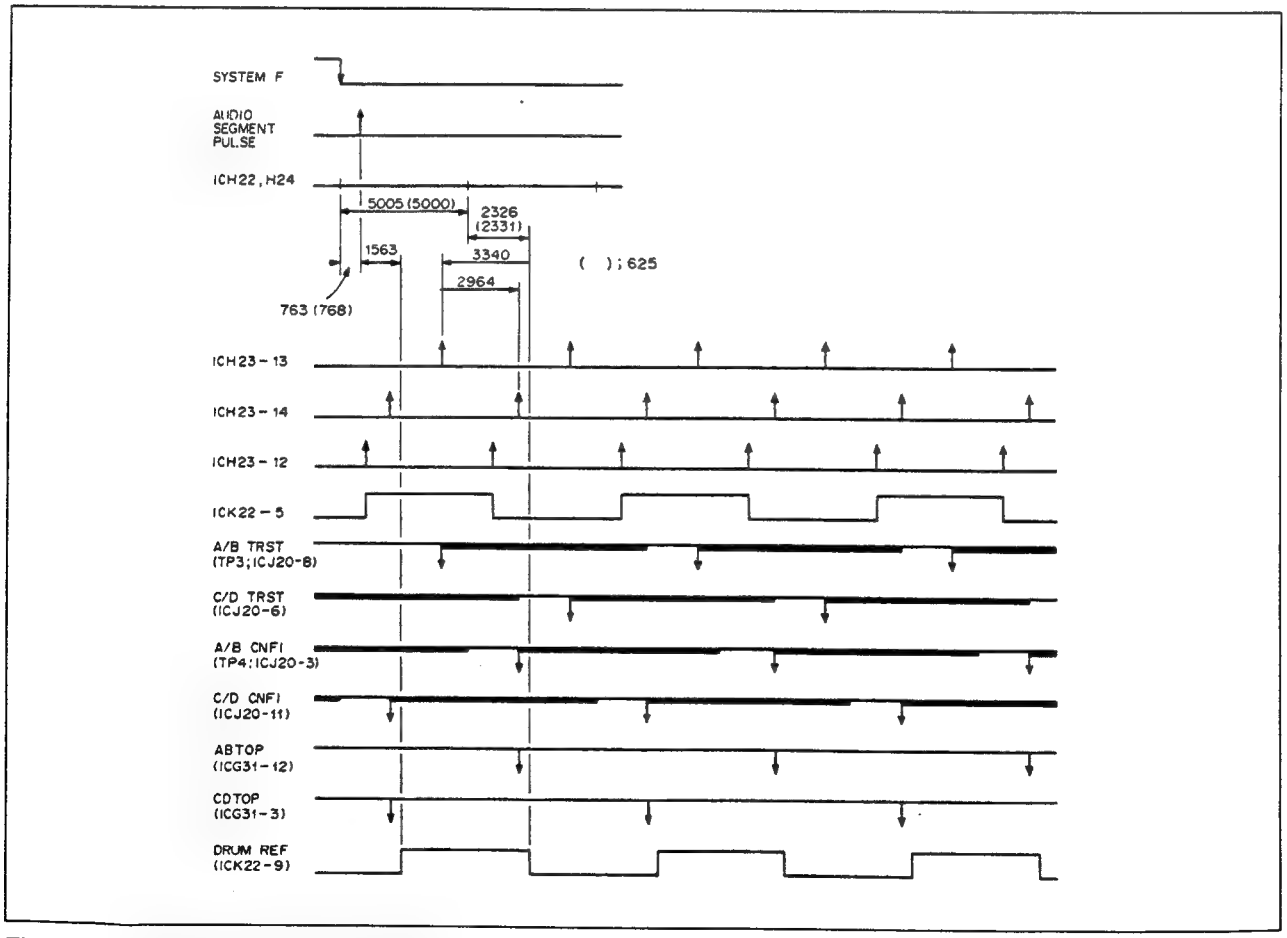



**Fig. 7-1-10. Track Control Pulse Timing (TG-28 Board)**

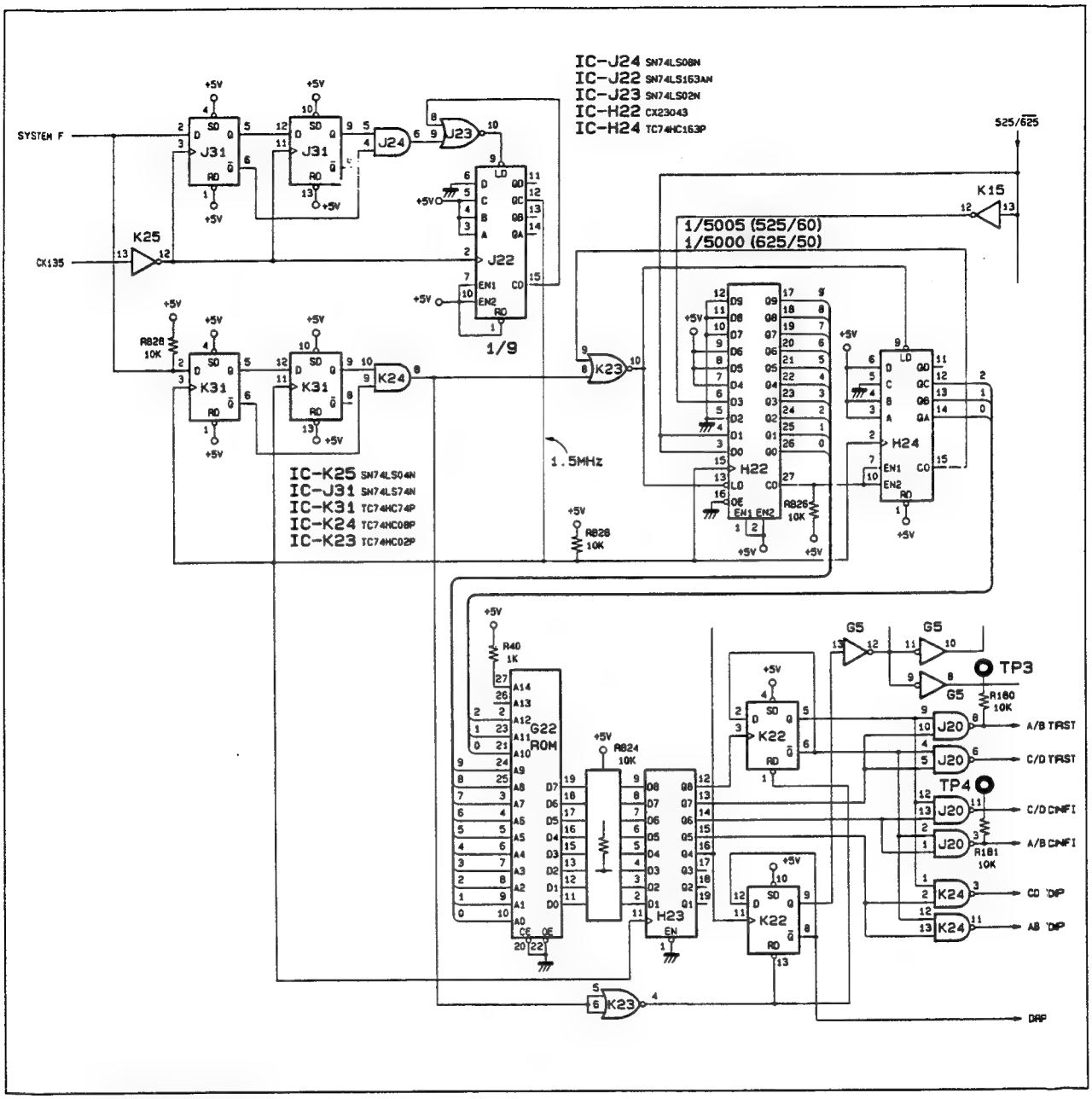



**Fig. 7-1-11. Track Control Pulse Generator (TG-28 Board)**

### 6. REC/EE gate pulse generator (TG-28 board)

The track start pulses "A/B TRST" and "C/D TRST," and the playback track start pulses "A/B CNFI" and "C/D CNFI" supplied from the above-mentioned track control pulse generator are used as count start pulses to count the recording sample clock pulse (9.83682 MHz) and generate the recording gate and EE gate signals. Also output are the video shuffling memory read start pulses "SHSA" and "SHSC" and the audio shuffling memory read start pulses "ASHA" and "ASHC" as well as the video/audio edit and EE timing pulses. The description below applies to the A/B track recording gate signals "REC CDA" and "REC CDB."

The "A/B TRST" pulse from the track control pulse generator is supplied to pin 2 of ICK11 while the recording sample clock signal (fREC: 9.83682 MHz) produced by dividing down the output (19.67364 MHz) of VCOX5 by two at ICF29 is supplied to pin 1 of ICK11. ICK11 supplies both the track start pulse which has been synchronized with the recording sample clock pulse and the 2.46 MHz clock pulse (CK0 pin 18), which is produced by dividing down the recording sample clock pulse by 4, to track counter ICK12 and K13.

Recording gate signals "REC CDA" and "REC CDB" are output from ROM ICJ11 and J13 which uses the track counter output as the address. The phase of the B channel recording gate signal "REC CDB" is delayed by an amount which is equivalent to the number of samples that corresponds to the difference in the mounting angles of the channel A and B recording heads.

The video edit timing pulses serve to determine the video edit points and they are produced from the A/B channel pulse which is output from pin 14 of ICH13 and the C/D channel pulse which is output from pin 14 of ICH10.

The audio edit timing pulses are generated only from the C/D channel and are output from pin 17 of ICH8 with every rotation of the drum (every audio segment).

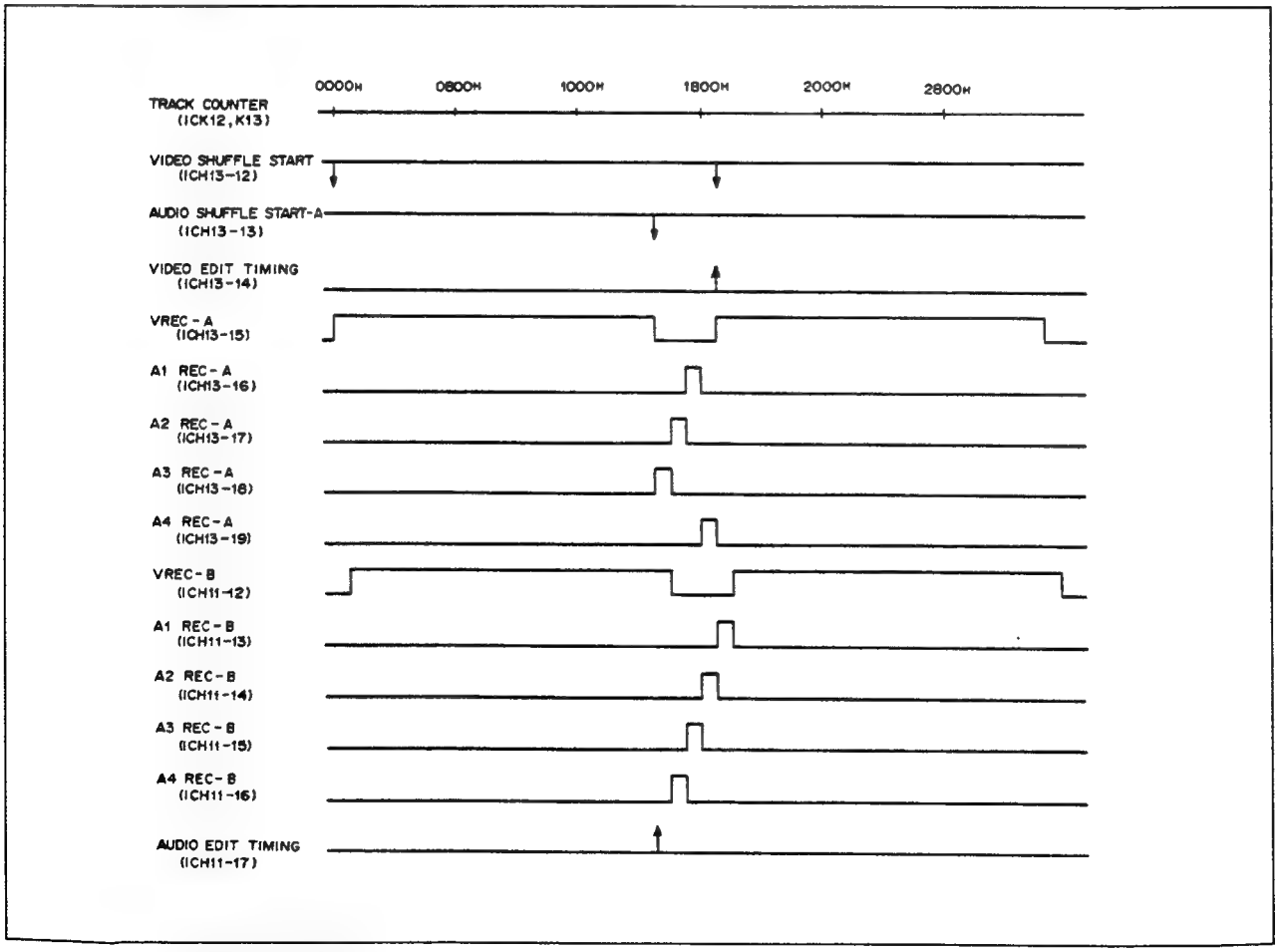



**Fig. 7-1-12. A/B Channel REC Gate Pulse (TG-28 Board)**

The recording gate signals obtained in this way are sent to the REC/EE command generator, only the recording gate signal corresponding to the preset channel in the EDIT or REC mode is selected by ICH9 and H12, and it is supplied to the IE-17 board as the "REC CD" recording command.
Similarly, the EE gate signal is sent to the REC/EE command generator, only the EE gate signal corresponding to the preset channel in the preview or EE mode is selected by ICH3 and H6, and it is supplied to the SY-70 board as the "SRE" EE command.



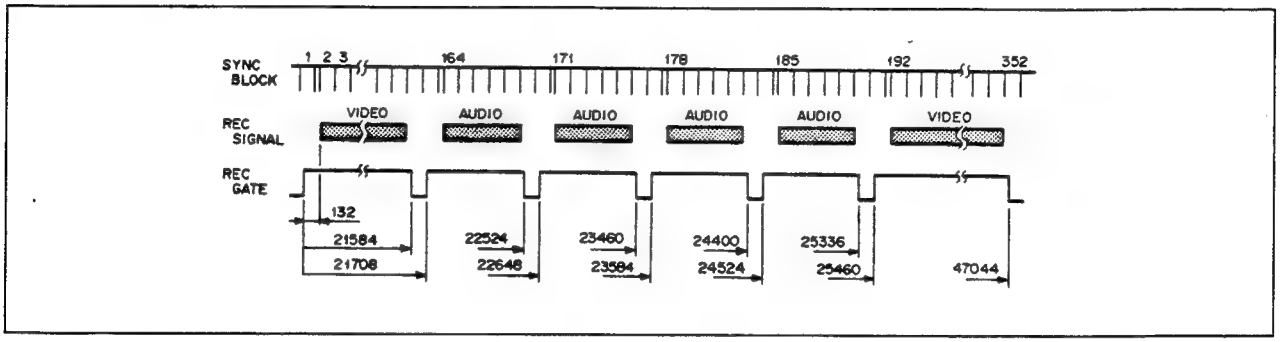



**Fig. 7-1-13. REC Gate Pulse (TG-28 Board)**

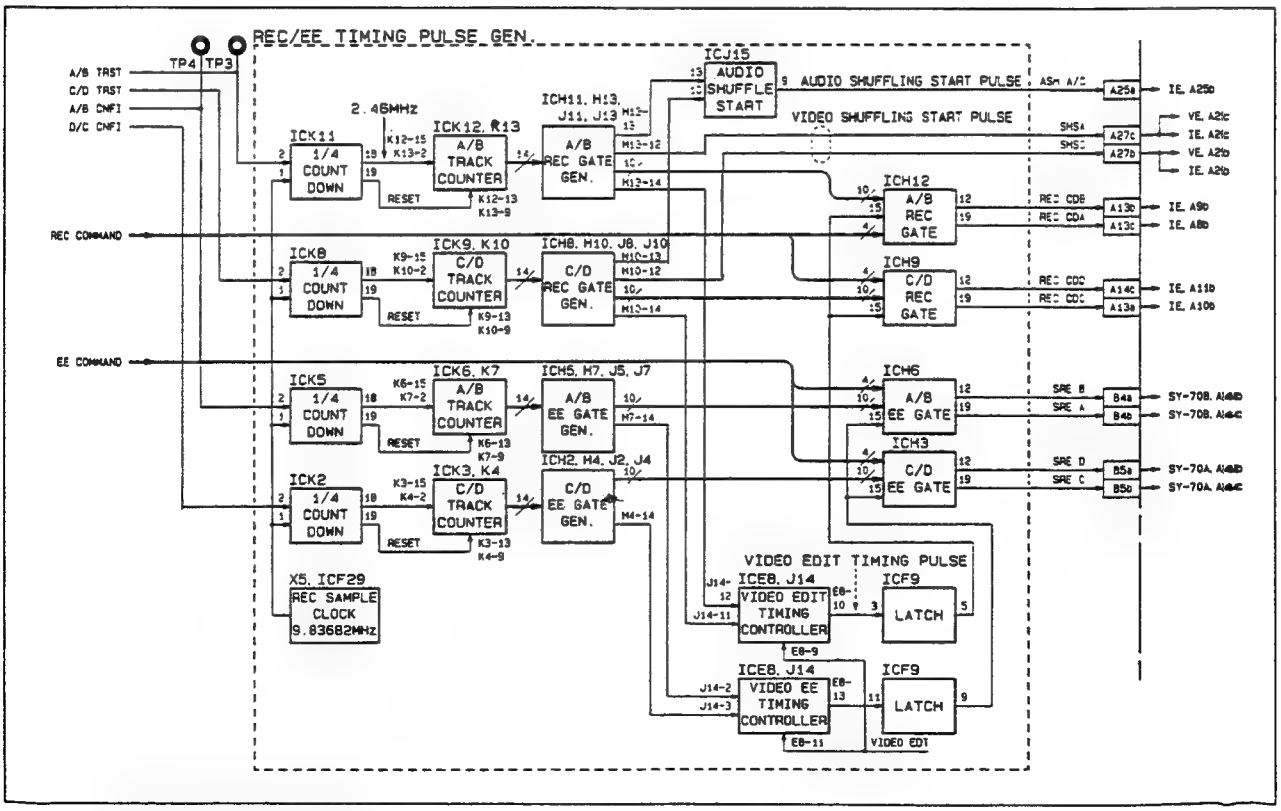



**Fig. 7-1-14. REC/EE Gate Pulse Generator (TG-28 Board)**

## 7. PLL2 (TG-28 board)

Based on the SYSTEM 2H (2xfH) signal supplied from PLL1, this circuit generates the 12.288 MHz (24 kHz × 256) clock pulse for audio signal processing whose phase is locked to the video 5-frame pulses.

The comparison frequency of phase comparator ICG24 is 83.916 Hz for the 525/60 system and 250 Hz for the 625/50 system. This means that PLL2 functions as a PLL with a multiple of 146432 for the 525/60 system and 49152 for the 625/50 system.

Although the lock-in time is increased with a PLL circuit which uses a voltage-controlled crystal oscillator to yield a high multiplication ratio, this particular circuit serves to detect the mode of the phase comparator, provide digital control and reduce the lock-in time.

After it is output from pin 18 of ICJ30, the SYSTEM 2H pulse is divided down by 375 at ICK19 for the 525/60 system and by 125 for the 625/50 system to form the reference signal (REF: ICG24 pin 1) for phase comparison.

The window pulse is output from pin 2 of ICF18 and when the VAR (VARIABLE PHASE: ICG24 pin 3) signal does not enter this window, the divide-by-572 (or divide-by-192 for the 625/50 system) counter ICK18 is preset by the output of ICH17 pin 5, the divide-by-256 counter ICF17 and G17 is reset by the output of ICH17 pin 12, the VAR signal is moved closer to the REF signal, and the lock-in time is reduced. When the preset pulse and reset pulse output timing is behind the REF signal—in other words, when the VAR signal is ahead of the REF signal—the ICH17 pin 13 output is inserted into the REF signal via ICK23 so that the VAR signal will, to all appearances, be delayed from the REF signal.

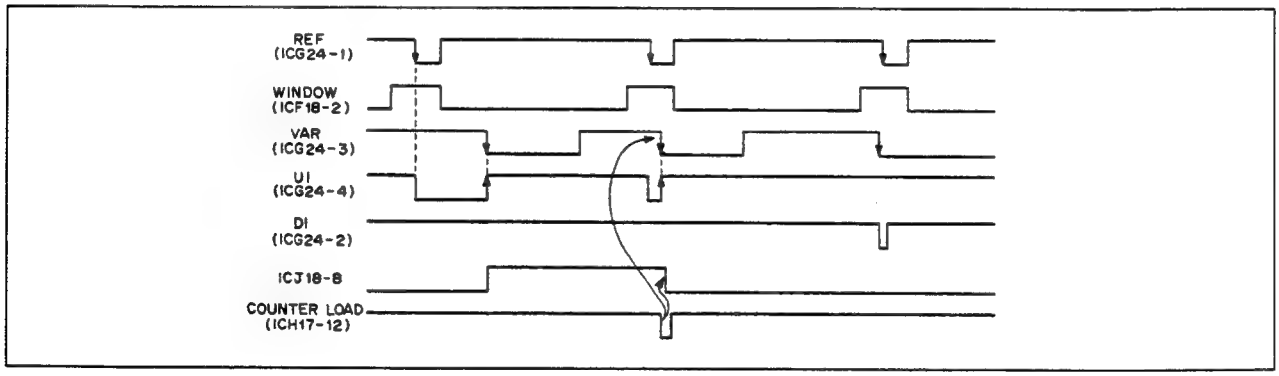



**Fig. 7-1-16. When VAR Signal is Behind REF Signal (PLL2/TG-28 Board)**

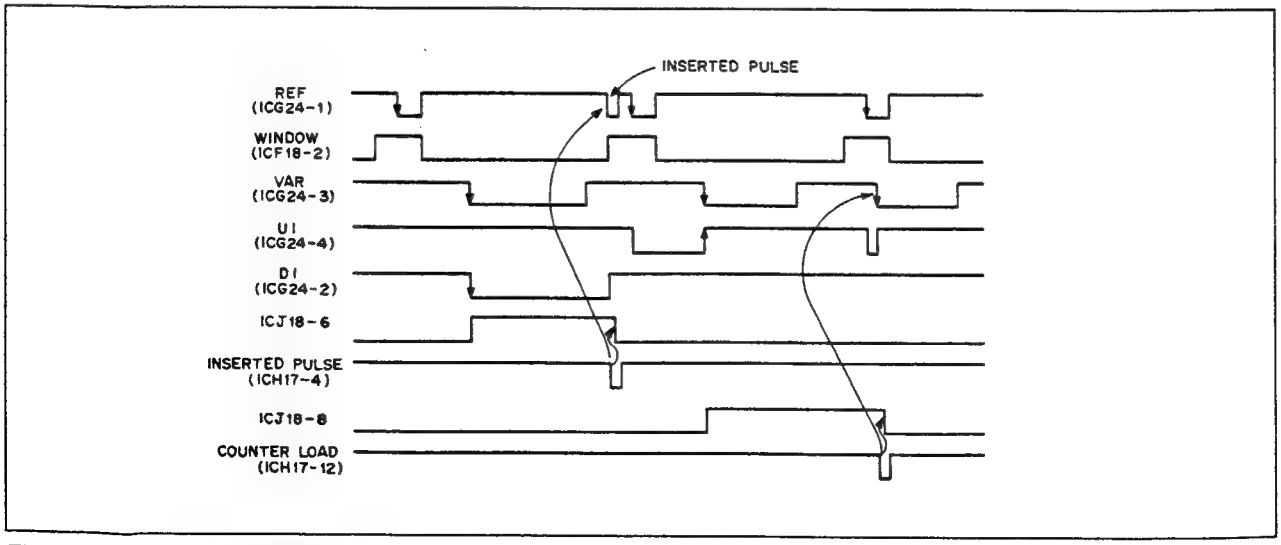



**Fig. 7-1-17. When VAR Signal is Ahead of REF Signal (PLL2/TG-28 Board)**

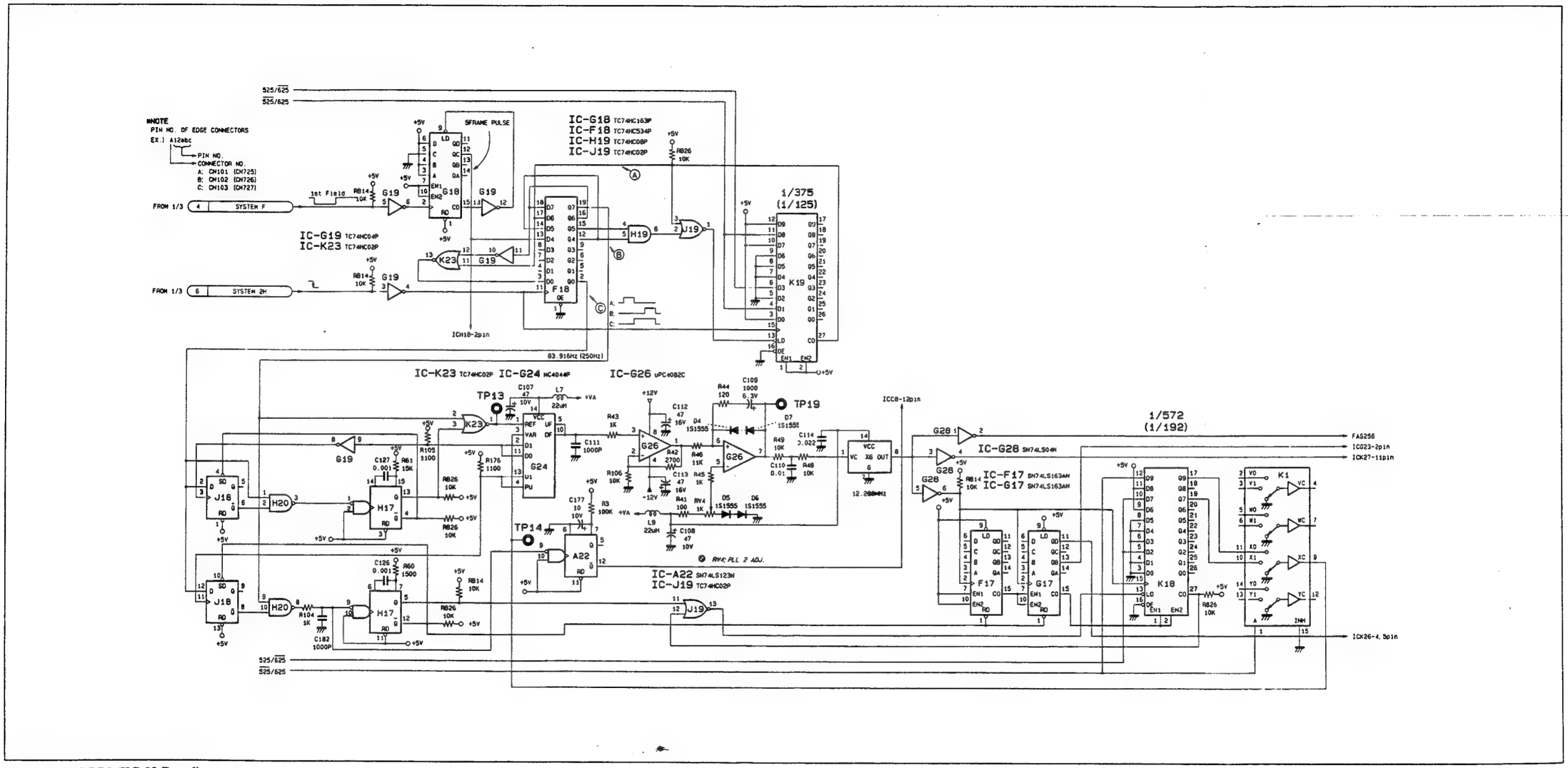



Fig. 7-1-15. PLL2 (TG-28 Board)

## 8. Audio segment counter (TG-28 board)

With a 625/50 system, 320 audio samples enter the audio segment as prescribed. However, with a 525/60 system, some audio segments have 320 samples and others 321 samples, as shown by the table 7-1-1.

The audio segment counter is provided especially for outputting the segment pulses for a 525/60 system. It is composed of audio segment counter ICK17 which is activated by the "FAS" audio sampling clock pulse and control counters ICH16 and J16 which control the segment counter.

The carry output (CO: pin 27) of audio segment counter ICK17 which is initialized by the "5 FRAME" 5-frame pulse is supplied to the enable input pins (EN1, EN2: pins 7, 10) of control counter ICH16. Control counters ICH16 and J16 count the audio segment pulses.

The initial value corresponding to the number of samples in the segments shown in Table 7-1-1 is passed to audio segment counter ICK17 from ROM ICK16 which treats the ICH16 and J16 counter output as the address. This causes the above-mentioned audio segment pulses to be generated.

| SEG. NO. / FRAME NO. | AUDIO SAMPLE COUNT | | | | |
|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 |
| 0 | 320 | 321 | 320 | 321 | 320 |
| 1 | 320 | 320 | 321 | 320 | 320 |
| 2 | 320 | 321 | 320 | 321 | 320 |
| 3 | 320 | 320 | 321 | 320 | 320 |
| 4 | 320 | 321 | 320 | 321 | 320 |

**Table 7-1-1. Audio 5-Frame Pulse Sequence (TG-28 Board)**

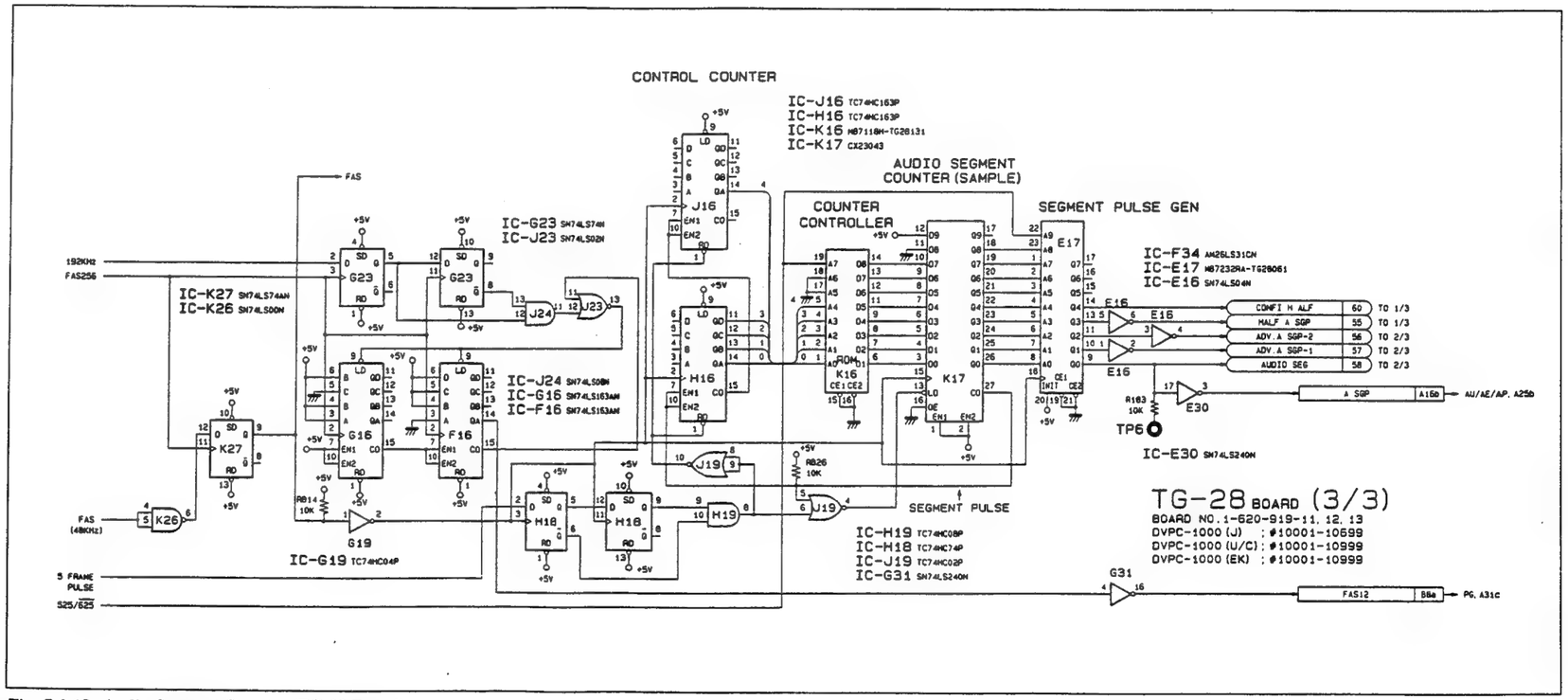



**Fig. 7-1-18. Audio Segment Counter (TG-28 Board)**

**9. Audio spot erase command generator (TG-28 board)**

The resolution for the audio spot erasure with the DVR-1000/DVPC-1000 is measured in audio segment units. However, since interfacing between the DVR-1000 and DVPC-1000 is done field by field, it is not possible to transfer commands in such small units. This problem is therefore solved during spot erasure by receiving the adjust data of the spot erase IN point and the spot erase period data from the DVR-1000.

After it is output from pin 22 of UPI ICA11, the "SPOT ERASE PLS" spot erase start command is latched to ICB11 at the SYSTEM V signal timing, synchronized with the "PLL H" H pulse and fetched to pin 3 of ICD9. With this signal acting as the load pulse, the spot erase IN point adjust counter ICF10 loads the "SEIN ADJUST0-3" IN point adjust data provided from the UPI. At ICE9, the "PLL H" H pulse is taken out for only 1 clock pulse at the timing of the load pulse, it is OR-ed with the ADV ASEGP-1 pulse whose timing precedes even the "AUDIO SEG" audio segment pulse, and the resulting pulse is sent to ICF10 as the "CK1" clock pulse. This operation determines the spot erase IN point.

The spot erase period is determined by the ADV ASEG-2 pulse which is behind the ADV ASEG-1 pulse and ahead of the audio segment pulse.

The IN point setting pulse and period end pulse are output from pin 6 of ICG10 as the spot erase command at the timing provided by ICF8 with the audio segment pulse.

This output is gated with the spot erase preset channel signals by ICD10 and is output to the AE-06 board as the "SPTE 0-3" spot erase commands for each of the 4 channels. The fade time during spot erasure can be set using switch S3. As described in the following section, the edit period for audio editing is determined by the REC1 pulse and the fading is completed by the REC2 pulse. However, in order for this to be controlled by the IN point adjust data and period data with spot erasure, a pulse corresponding to REC2 pulse of audio editing is generated since it cannot be received from the DVR-1000.

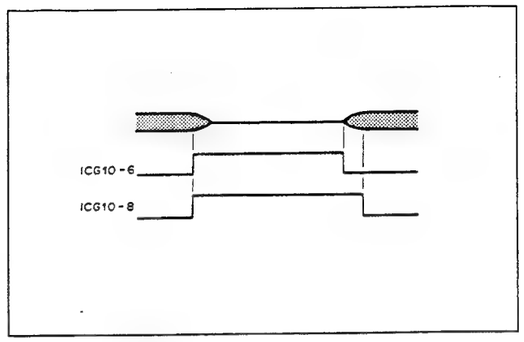



**Fig. 7-1-19. Audio Spot Erase Fade-out Timing (TG-28 Board)**

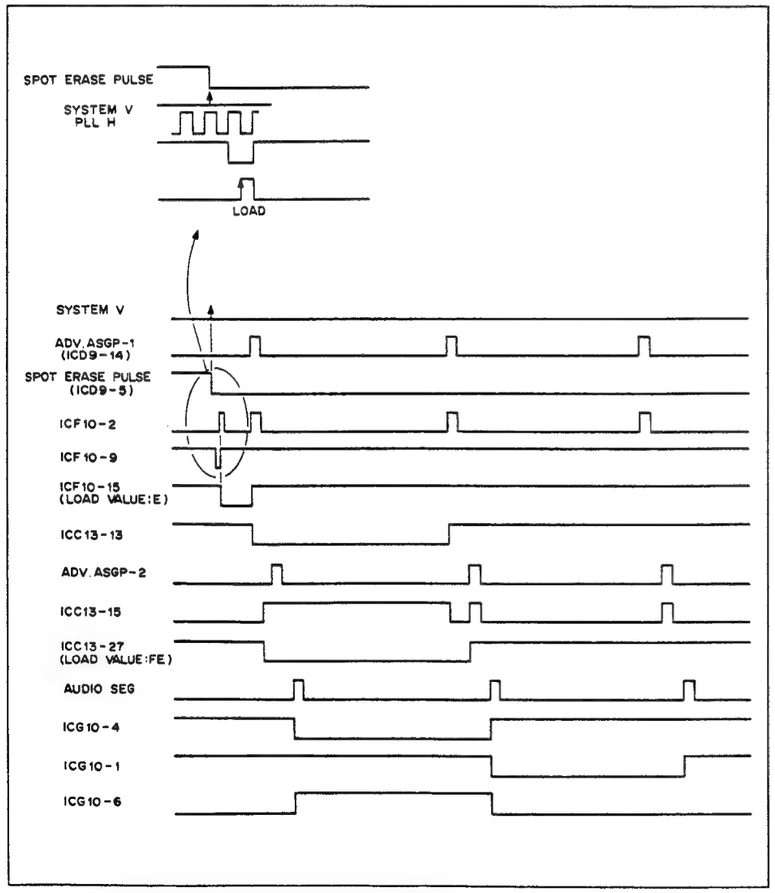



**Fig. 7-1-20. Audio Spot Erase Timing (TG-28 Board)**

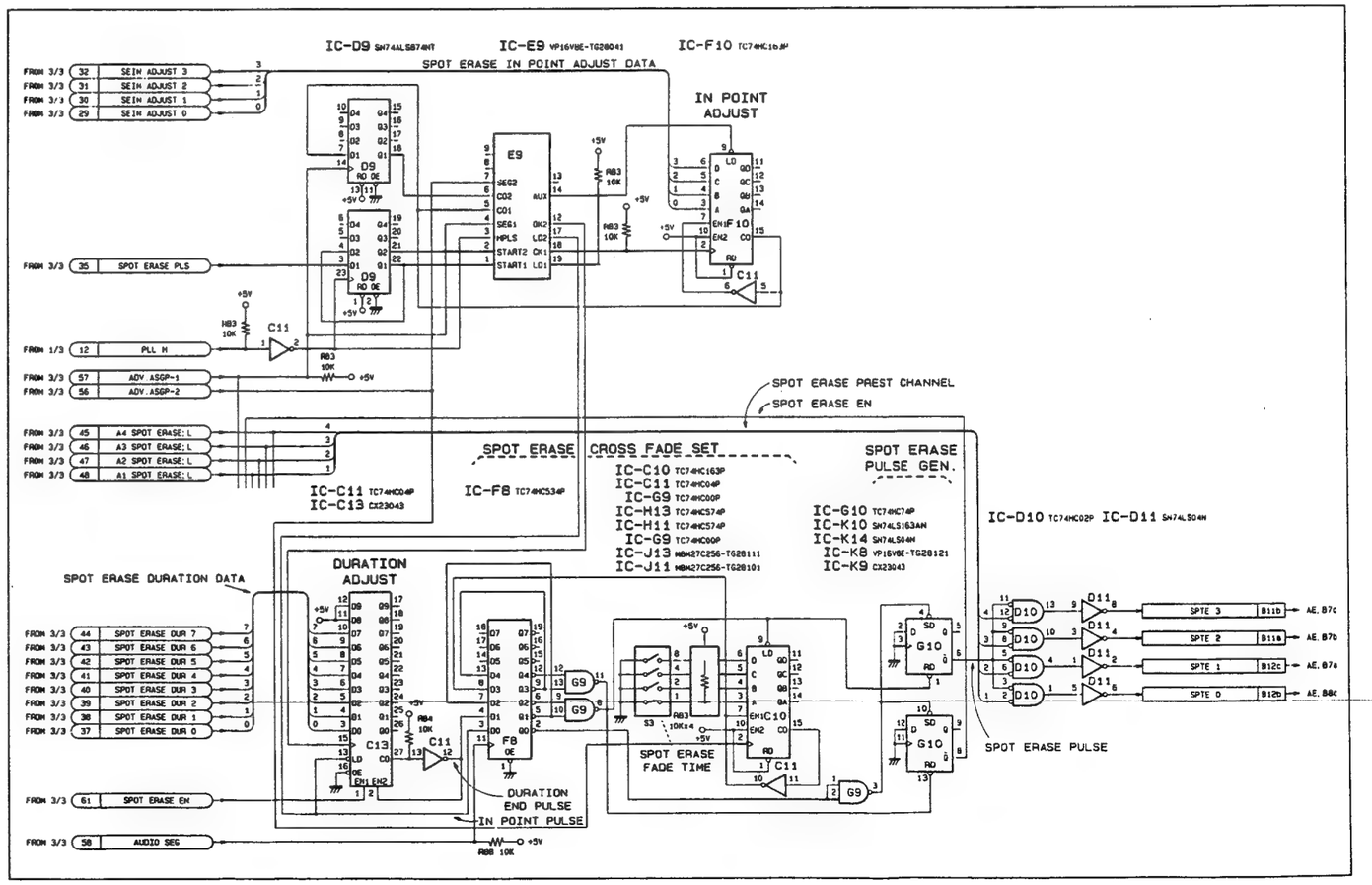



**Fig. 7-1-21. Audio Spot Erase Command Generator (TG-28 Board)**

### 10. REC/EE command generator (TG-28 board)

The audio REC1 pulses which are supplied from the UPI are output to the AE-06 board as the "EDIT PLS 0-3" edit commands during editing or previewing, and the audio REC2 pulses, video REC1 pulse and audio spot erase pulses are output from ICE11 and E12 as the EE or REC commands, depending on whether the editing, REC, preview or EE mode has been established.

The audio REC/EE commands are delayed by 2 audio segments by ICF11 and F12, and output. The video REC/EE commands is output by ICF9 at the timing provided by the EDIT/EE timing pulses. The above signals are gated by the REC/EE gate signals supplied from the REC/EE gate signal generator and the resulting signals are output from ICH3, H6, H9 and H12 as the "REC CD A-D" REC commands and "SRE A-D" EE command signals corresponding to each of the heads.

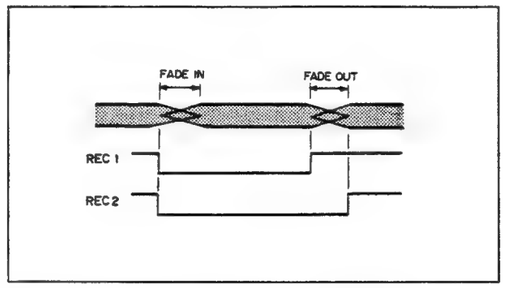



Fig. 7-1-23. REC/EE Commands (TG-28 Board)

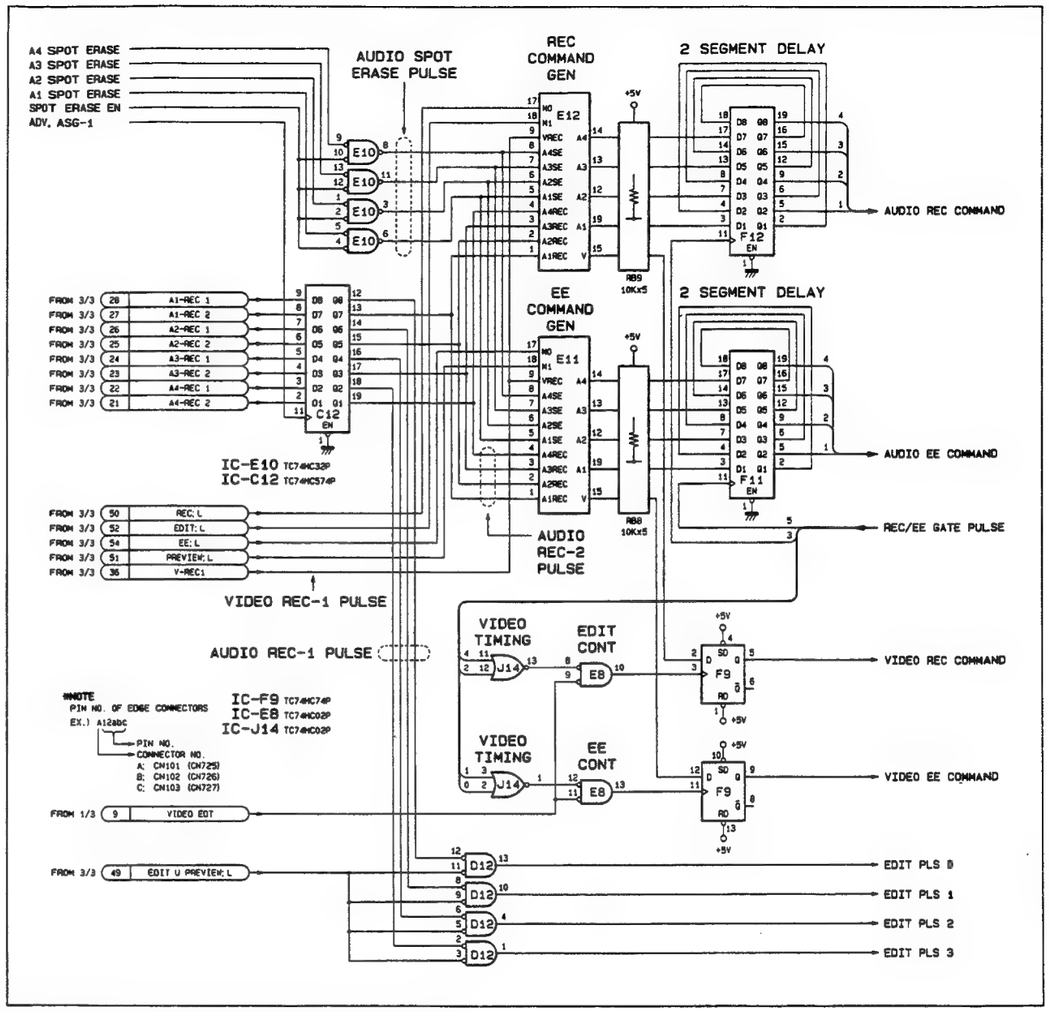



Fig. 7-1-22. REC/EE Command Generator (TG-28 Board)

## 11. TG-28 board input/output signals

### (1) Input signals

- **525/625 (IF-139 board)**
  System select signal. It is set high with a 525/60 system and low with a 625/50 system.

- **AFT (DVR-1000)**
  Playback audio frame pulse. This coincides with the video 5-frame pulse with a 525/60 system and with the video frame pulse with a 625/50 system.

- **BA0, BA6-BA3, BD7-BD0, BD T/R, BDEN, BDRD, BDWR, BRST (IF-139 board)**
  Control bus and data bus signals for interfacing between UPI ICF21 on TG-28 board and IF-139 board.

- **CFIN**
  Color frame pulse which is supplied to the CF PULSE INPUT connector

- **CFT (DVR-1000)**
  Playback color frame pulse

- **IN SYF, IN SYH (VE-12 board)**
  Frame pulse and H pulse which are extracted from the digital video input signal

- **INSYNC (IV-14/IV-20 board)**
  TTL level composite sync signal which is separated from the analog video input signal

- **REFSY (IV-14/IV-20 board)**
  Composite sync signal or black burst signal which is supplied to the ANALOG REFERENCE INPUT connector

- **REFV7-REFV0, REFCK**
  Digital video signals which are based on the SMPTE RP-125/EBU TECH3246-E format and which are supplied to the DIGITAL REFERENCE INPUT connector

### (2) Output signals

- **27MI (VA-45 board)**
  27 MHz clock signal which is generated by the PLL circuit from the input H pulse. It is used for the video sampling clock and interface encoder clock pulses.

- **5FRM (AE-06 board, AU-86 board)**
  Recording system 5-frame pulse. For the 625/50 system, however, the frame pulse is output.

- **AAFRM (AP-14 board)**
  ADVANCE head playback system frame pulse. For the 525/60 system, however, the 5-frame pulse is output.

- **AB TOP, CD TOP (SY-70 board)**
  Head output timing pulses for A/B channels and C/D channels. On the SY-70 board, these pulses are used to initialize the TBC memory.

- **AFMP (AE-06 board, AU-86 board)**
  Frame pulse for audio signal processing

- **AFP (DVR-1000)**
  Audio frame pulse. This is sent to the DVR-1000 and recorded onto the CTL track.

- **ASEG (AU-86 board, AE-06 board, AP-14 board)**
  Audio segment pulse. It is output at the same timing as the recording start line of the first video field and it is subsequently output with each audio segment.
  With the 625/50 system, it is output every 320 audio samples; with the 525/60 system, it is output every 320 or every 321 audio samples (depending on the audio segment).

- **ASH A/C (IE-17 board)**
  Audio shuffling start pulse. Its fall is the start point of the A/B channels; its rise is the start point of the C/D channels.

- **CAFRM (AP-14 board)**
  CONFI head playback system frame pulse. With the 525/60 system, however, the 5-frame pulse is output.

- **CF OUT**
  Color frame pulse. It is output externally through the CF PULSE OUTPUT connector.

- **CFP (DVR-1000)**
  Color frame pulse. It is sent to the DVR-1000 and recorded onto the CTL track.

- **CK135 (VE-12 board)**
  13.5 MHz clock signal of recording system. The digital video signal supplied to the VE-12 board is exchanged with this clock signal and processed.

- **CK27 (VN-01 board)**
  Data clock pulse of the digital video signal conforming to the SMPTE RP-125/EBU TECH3246-E format which is output from the VN-01 board. Its frequency is 27 MHz.

- **EDT PLS0-EDT PLS3 (AE-06 board)**
  Edit start pulses corresponding to each of the 4 digital audio channels. On the AE-06 board, cross fading is operated at the fall and rise of these pulses.

- **FAS (IE-17 board, AE-06 board, AU-86 board, PG-13 board, IF-139 board)**
  Audio sampling clock pulses of recording system. Their frequency is 48 kHz.

- **FAS12 (PG-13 board)**
  DMIX sampling clock pulse. Its frequency is 576 kHz (12 × 48 kHz). The frequency of this signal is not precisely 12 times 48 kHz but a scaled-down version of the 256 × 48 kHz clock pulse when required.

- **FAS256 (SY-70 board, IE-17 board, AE-06 board, AU-86 board, PG-13 board, IF-139 board)**
  Clock pulse which is 256 times the recording system audio sampling clock pulse

- **LSAD (CI-01 board)**
  ADVANCE head playback system LIP sync memory read start pulse. In actual fact, it is finely adjusted inside the CI-01 board.

- **LSCF (CI-01 board)**
  CONFI head playback system LIP sync memory read start pulse. In actual fact, it is finely adjusted inside the CI-01 board.

- **MON H, MON V (IF-139 board)**
  H pulse and V pulse for superimposing characters onto the picture monitor output

- **MUTE (AN-01 board)**
  Audio digital muting command. It is output when something is wrong with the playback audio frame pulse which is supplied from the DVR-1000 and when the lock status of the PLL circuitry inside the TG-28 board is released.

- **PB CK135 (VN-01 board, FM-09 board)**
  Playback system 13.5 MHz clock

- **PB FAS (AN-01 board, AP-14 board, CI-01 board, PG-13 board, IF-139 board)**
  Playback system audio sampling clock pulse. Its frequency is 48 kHz. In actual fact, it is the same as the "FAS" recording system clock signal.

- **PB FAS256 (AN-01 board, AP-14 board, CI-01 board, PG-13 board, IF-139 board)**
  Clock pulse which is 256 times the playback system audio sampling clock pulse. In actual fact, it is the same as the "FAS256" recording system clock signal.

- **REC CDA-REC CDD (IE-17 board)**
  REC command pulses corresponding to recording channels. While these pulses are low, recording data is differentially output from the IE-17 board. While they are high, both differential outputs from the IE-17 board are set low.

- **REF O/E, V START, H START (FM-09 board)**
  Read start pulses for frame memory on FM-09 board

- **SFID (VE-12 board)**
  Video shuffling sequence ID pulse. Video shuffling is characterized by a 4-field sequence, and this pulse indicates the first field. Its phase is locked with the phase of the playback color frame pulse.

- **SHSA, SHSC (VE-12 board, IE-17 board)**
  Video shuffling memory read start pulses. SHSA is for the A/B channels; SHSC is for the C/D channels.

- **SPTE0-SPTE3 (AE-06 board)**
  Spot erase pulses corresponding to digital audio channels. On the AE-06 board, the sound is faded out at the fall of these pulses and faded in at their rise.

- **SRE A-ARE D (SY-70 board)**
  EE command pulses corresponding to playback channels. During preview, these commands are for outputting the EE pictures for the edit preset channels.

- **SYNC (VA-45 board)**
  Sync signal which is inserted into the analog output Y signal

- **SYNC OUT (IV-14/IV-20 board)**
  This is converted on the IV-14 (IV-20) board to a composite sync signal between 0 and -4V and it is output externally through the ANALOG VIDEO OUTPUT connector.

- **SYSCK (VE-12 board, IE-17 board, CI-01 board, SY-70 board, FM-09 board)**
  Recording system signal processing clock pulse. Its frequency is 9.83682 MHz. The recording signal rate (78.69456 Mbits/sec) is 8 times this clock frequency.

- **SYS FR (IF-139 board)**
  Servo reference frame pulse
  This is sent to the IF-139 board and is then sent to the DVR-1000 once it has been processed to deal with the PLL activation after power-on.

- **VAF (VA-45 board, PG-13 board)**
- **VAH (VA-45 board)**
  Frame pulse and H pulse. They are used as the interface encoder frame pulse and clamp pulse.

- **VBV (VE-12 board)**
  VIDEO-BLACK-VIDEO command pulse during preview. While this pulse is low, the output video signal is set to black.

## 4-7-2. TG-28 Board (Board Number Suffix: −14)

The description below deals only with the differences between TG-28 boards with the "−14" suffix and those with the "−11/12/13" suffix. Otherwise, the circuitry configuration is vritually identical although the reference numbers given to the parts differ.

The main differences are listed below:

- Frame pulse/H pulse separator circuit
- Digital input reference sync signal phase
- PLL circuit configuration
- Output sync signal phase adjustment
- Audio frame pulse generator

### 1. Frame pulse/H pulse generator (TG-28 board)

This circuit serves to separate the frame pulse and H pulse from the input composite pulse.

Monostable multivibrator ICB16 detects the trailing edge of the input sync signal. Also, monostable multivibrator ICA22 has time constants which are set at 43 μsec and 19 μsec, and the equalizing pulse is masked by the former to provide the H pulse. This is the H pulse from which the fall of the pulse output from pin 4 of ICA22 is separated.

The frame pulse is produced by latching the H pulse at the rise of the V blanking pulse from ICA21 pin 8.

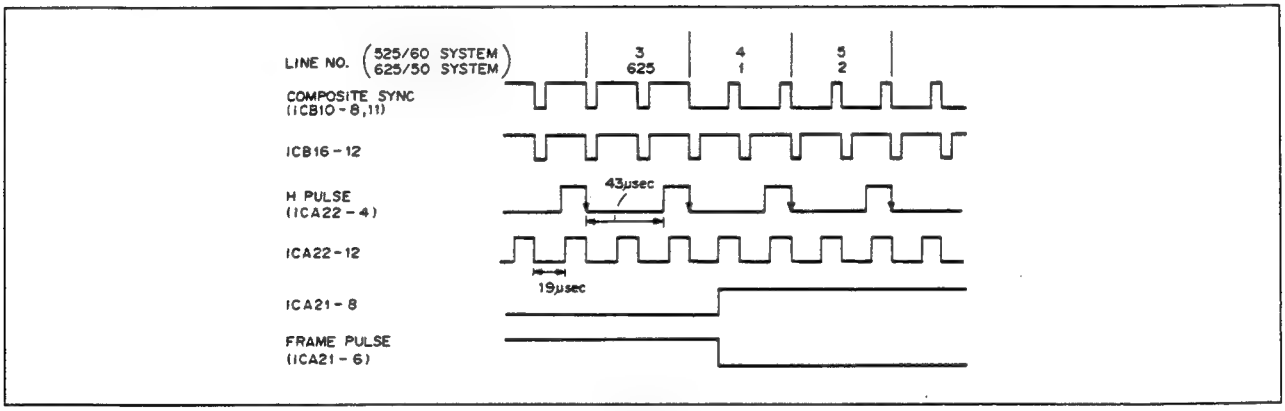



**Fig. 7-2-1. Frame Pulse/H Pulse Separation Timing (TG-28 Board)**

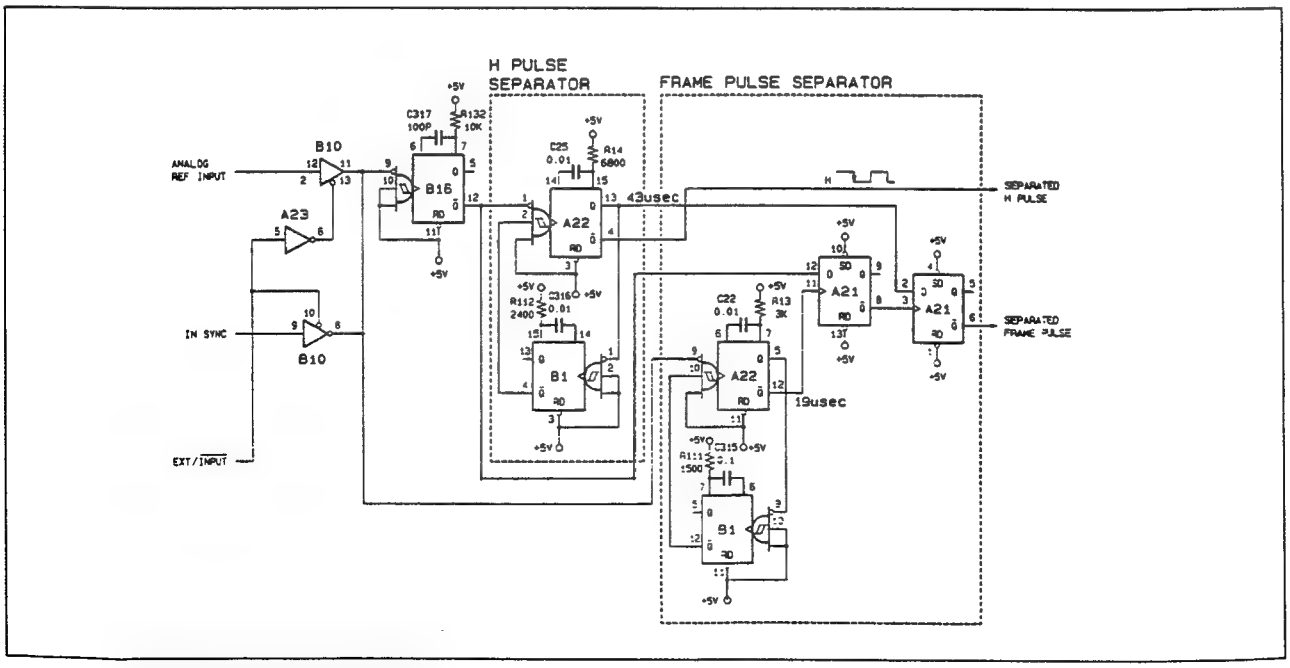



**Fig. 7-2-2. Frame Pulse/H Pulse Separator (TG-28 Board)**

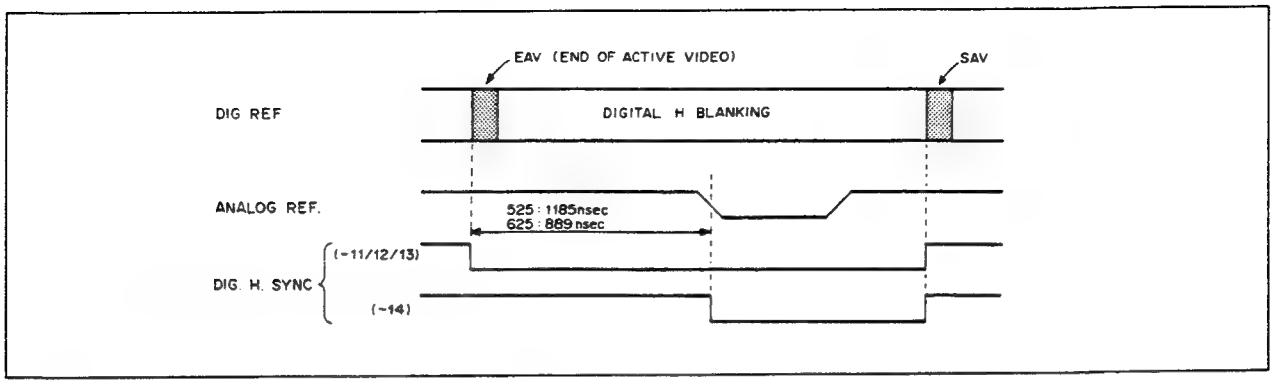



**Fig. 7-2-3. Relationship Between Digital Reference and Analog Reference Phases (TG-28 Board)**

### 2. Change in digital reference sync phase (TG-28 board)

As shown by Fig. 7-2-3, under the SMPTE RP-125/EBU TECH3246-E format an offset of 1185 nanosec is provided for the 525/60 system and 889 nanosec for the 625/50 system between the analog H sync signal and digital H blanking EAV (end of active video).
On a TG-28 board with the "−11/12/13" suffix, this offset simply becomes the difference in the phases of the digital and analog systems, but on a TG-28 board with the "14" suffix it defines the digital H sync signal, as shown by Fig. 7-2-3, and provides phase adjustment.

### 3. PLL circuit (TG-28 board)

Four PLL circuits are used on a TG-28 board with the "−11/12/13" suffix, but on a TG-28 board with the "−14" suffix the recording system PLL (PLL1) and playback system PLL (PLL4) for processing the video signals are combined so that the following 3 circuits are featured.

PLL1: For generating the sync signals
PLL2: For generating the 12.288 MHz clock signal for the audio system
PLL3: For generating the 27 MHz clock signal for the video system

When the reference signals are not supplied, PLL1 starts free-running in the INT mode to generate the sync signals. Fig. 7-2-4 shows the relationship between the various PLL circuits.

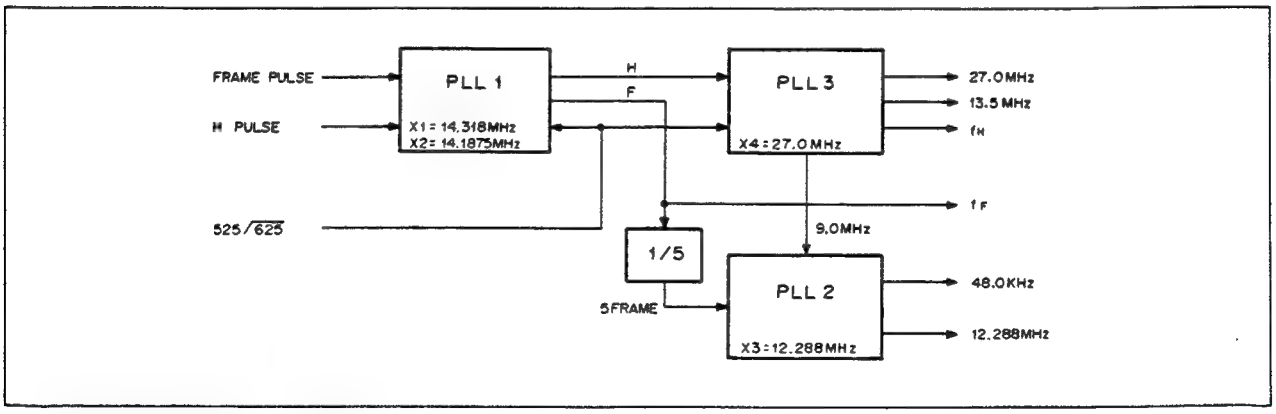



**Fig. 7-2-4. PLL Circuitry Configuration (TG-28 board)**

**(1) PLL1 (TG-28 board)**

This circuit regenerates the output H pulse, frame pulse and other sync signals from the "HPLS" H pulse and "FPLS" frame pulse, it detects the INT/EXT mode, and it generates by free-running the sync signals in the INT mode.

ICA13 is originally an IC designed for generating sync signals but in this PLL circuit it detects the INT/EXT mode from the H pulses that are input continuously, and also compares the phase of the H pulses fed back from ICA15 with the phase of the input pulses.

Sync signal generator ICA15 requires a 14.318 MHz clock signal with the 525/60 system and a 14.1875 MHz clock signal with the 625/50 system. These clock signals are generated by voltage-controlled oscillators X1 and X2, and they are selected in accordance with the mode.

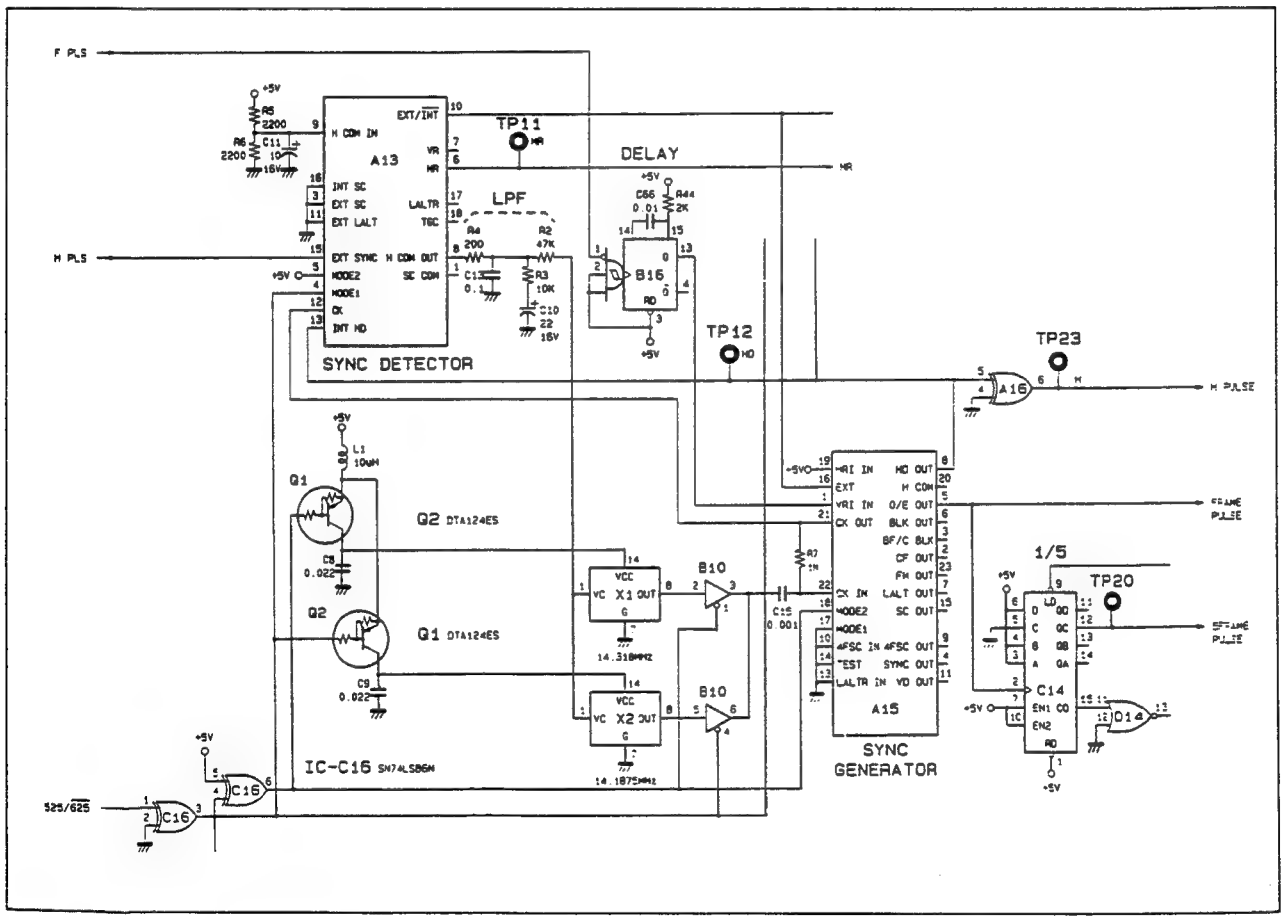



**Fig. 7-2-5. PLL1 (TG-28 Board)**

**(2) PLL3 (TG-28 board)**

Using the H pulses output from PLL1 as the reference signal, PLL3 generates the 13.5 MHz and 27 MHz clock signals for processing the video signals. The multiplication rate is 1716 times for a 525/60 system and 1728 times for a 625/50 system. Since clock signals with a 50% duty ratio are required for video signal processing, the fundamental waves of the VCXO X4 output are extracted, comparated by ICD27 and output. "VAH" H pulses serving as the reference signal for the entire system are output from frequency divider-counter ICD16. In addition, pulses formed by delaying the frame pulses output from the above PLL1 circuit by two lines using the VAH pulse are output for the "VAF" reference frame pulse.

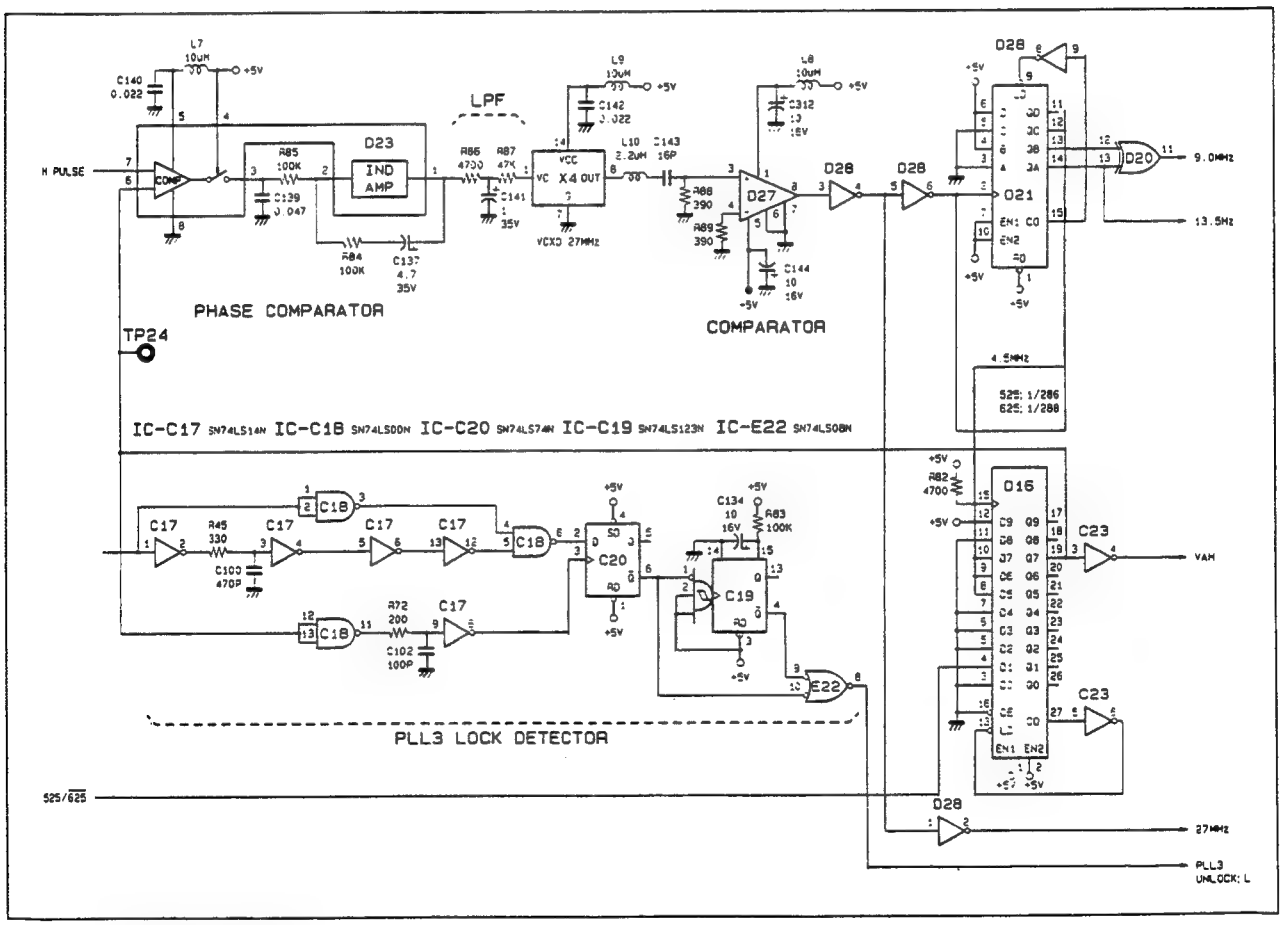



**Fig. 7-2-6. PLL3 (TG-28 Board)**

**(3) PLL2 (TG-28 board)**

From the 9.0 MHz clock pulse which is output from the PLL3 and the 5 FRAME PULSE, PLL2 generates the "FAS(48 kHz)" audio sampling clock pulse whose phase is locked to the 5-FRAME PULSE and also the "256FAS (12.288 MHz)" clock pulse which is 256 times the FAS pulse. The phase comparison frequency of this circuit is 24 kHz which is multiplied by 512 to obtain the 12.288 MHz clock signal.

The reference signal (24.0 kHz), which is produced by dividing down the 9.0 MHz clock pulse from PLL3 by 375, is supplied to pin 7 of phase comparator ICC25. However, without further processing, the FAS clock output (48 kHz) from PLL2 is simply locked to the frequency and not to the 5-frame pulse phase. Therefore, the edge of the "5 FRAME PULSE" (TP20) obtained by dividing the frame pulse frequency by 5 is taken out by the "VAH" reference H pulse which is output from PLL3, the edge is further differentiated by the 9.0 MHz clock signal to form the 5-frame period pulse and the divide-by-375 counter ICD17 is reset using this pulse. This serves to lock the phase of counter ICD17 – in other words, the phase of the 24.0 kHz reference clock signal – to the phase of the 5-frame pulse. Between 5 video frames, ICD17 has 4004 periods with a 525/60 system and 4800 periods with a 625/50 system.

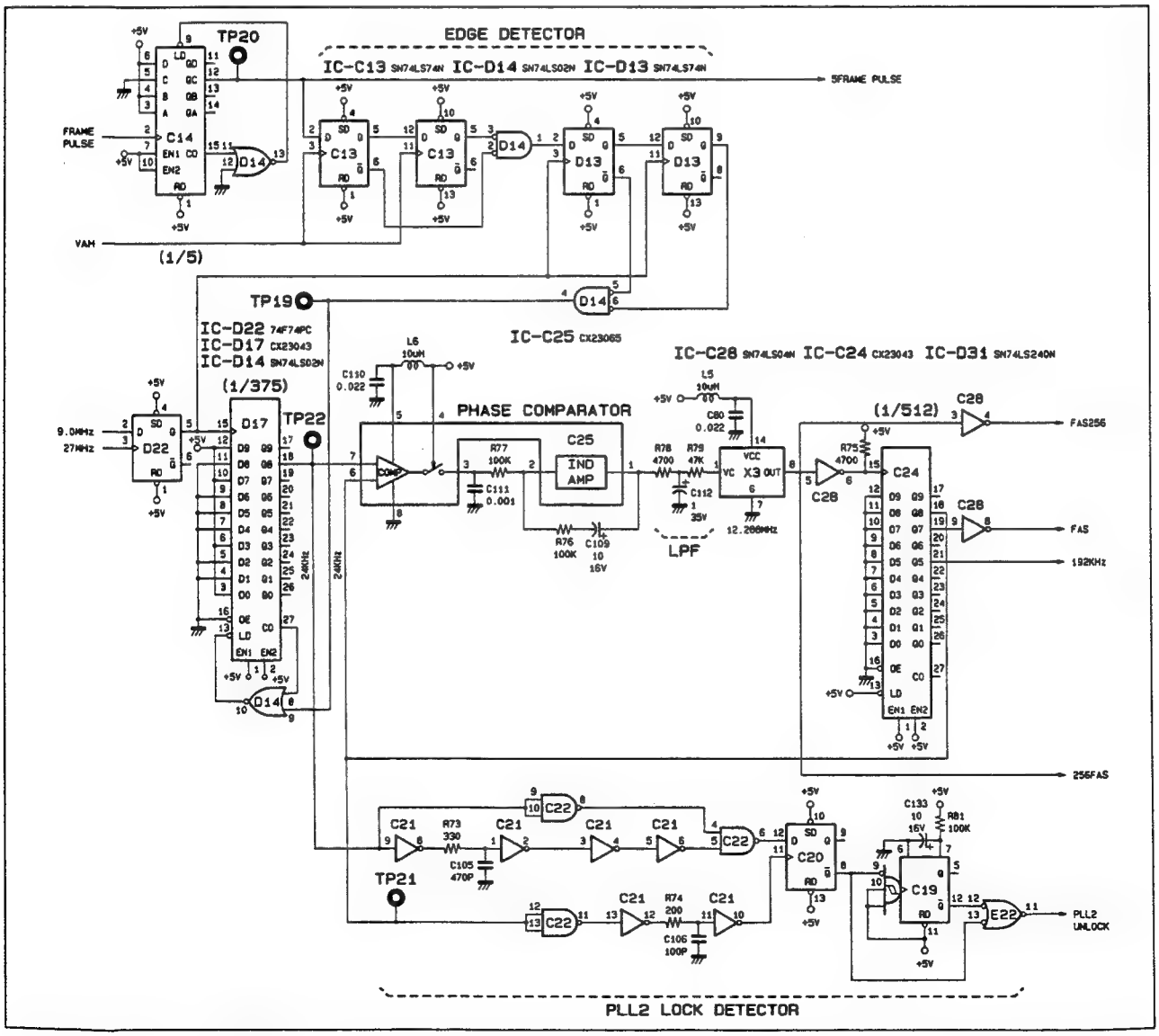



**Fig. 7-2-7. PLL2 (TG-28 Board)**

**4. Sync output circuit (TG-28 board)**

The "MON H" and "MON V" sync signals for superimposing characters as well as the "SYNC" and "SYNC OUT" output sync signals are generated by sync generator ICD28 (CX-773B) on a TG-28 board with the "−11/12/13" board number suffix. However, on a TG-28 board with the "−14" suffix, this circuit has been replaced by a PROM and a counter which operates at a frequency of 13.5 MHz. This makes it possible to adjust the sync signal phase in a single clock unit (13.5 MHz).

The output sync phase is determined by the values of "SYNC PHASE 0-7" supplied from the UPI. This circuit makes it possible to adjust the phase of ±127 clock signals (±9.4 μsec) in a single clock unit, centering on the fall in SYSTEM H.

Since the output sync phase is varied centering on the SYSTEM H fall, the load pulse (pin 13) of sync phase adjustment counter ICC9 must precede the SYSTEM H fall. At PROM ICK14, 128 clock pulses are allowed to go ahead and a load pulse ultimately preceded by 141 clock pulses due to the delay caused by the latch is supplied to ICC9. The ICC9 carry output (CO: pin 27) serves as the reference phase for the output sync signal.

The "MON H," "MON V" and "SYNC" signals are generated by the two PROMs, ICK16 and ICK17.

ICK16 outputs the sync pattern shown by Fig. 7-2-9 in accordance with the output of counter ICL16 which is initialized every H/2 based on the carry output. "MON H" is created from (1) and (2) in the sync pattern; "SYNC" is created from (2) through (5).

Frame counter ICL17 and L18 is initialized every frame by the "SYPHSREF" pulse latched by the ICC9 carry output and it counts the H/2 pulses. Depending on these counter outputs, ICK17 outputs the signal that selects the ICK16 output and "MON V" every H/2.

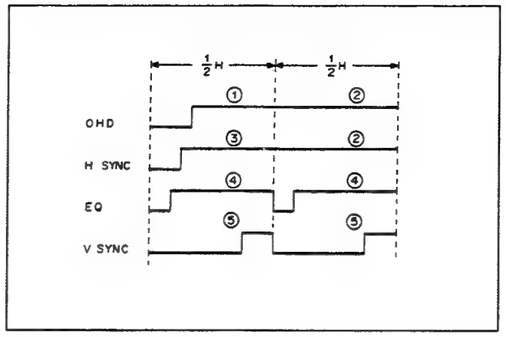



**Fig. 7-2-9. Sync Pattern (TG-28 Board)**

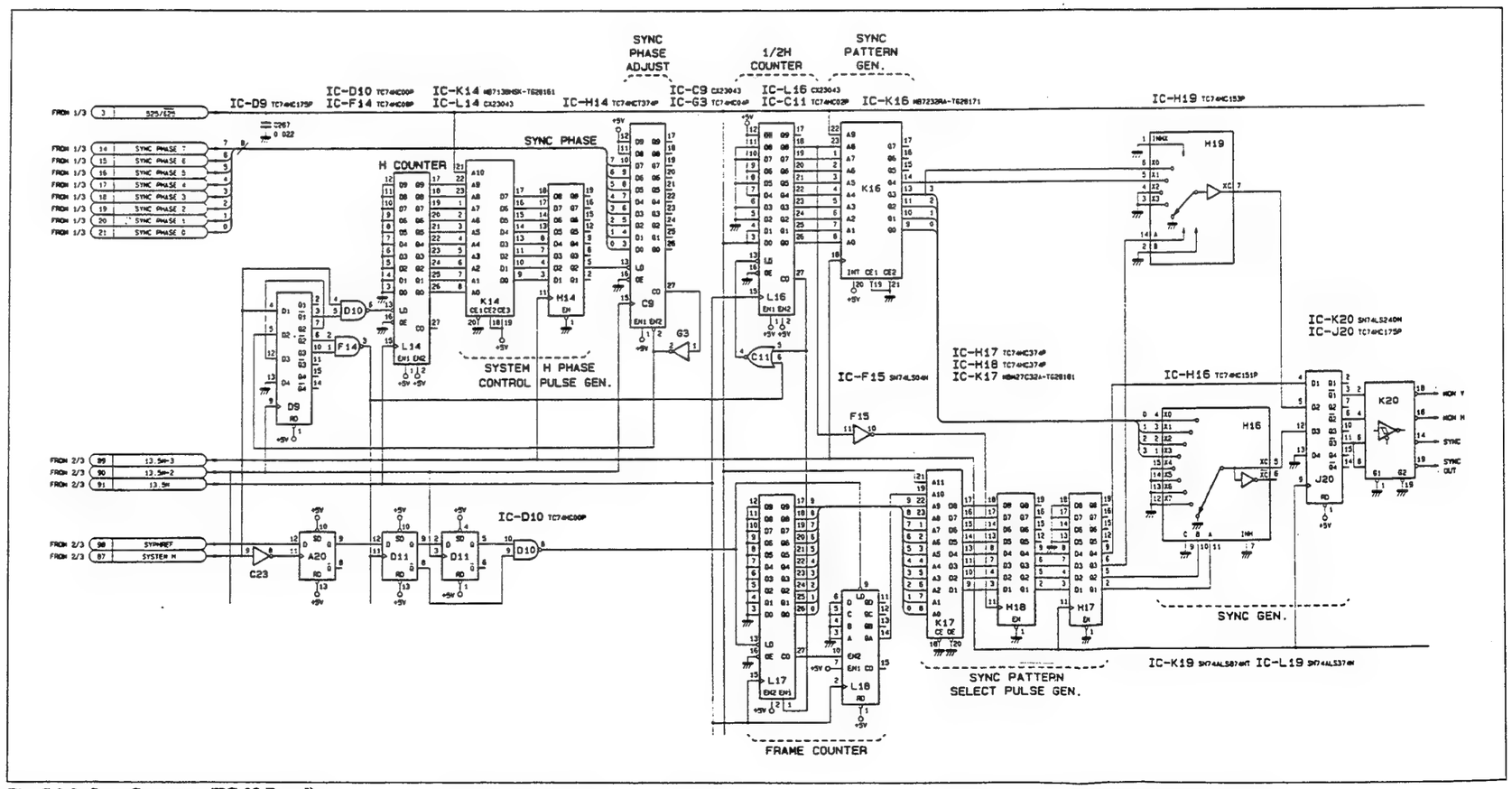



**Fig. 7-2-8. Sync Generator (TG-28 Board)**

### 5. Audio frame pulse generator (TG-28 board)

The playback audio frame pulse is the signal that serves as the reference for the control signals in the digital audio playback system, and it is provided by the playback signal from the CTL track. In a 525/60 system, it coincides with the 5-frame video pulse; in a 625/50 system, it coincides with the video frame pulse. The playback audio frame pulse must satisfy the following conditions:

- It must be compensated properly even when the playback CTL pulse has been lost.
- The correct period pulse must be supplied even when the playback CTL pulse has been thrown into disarray.
- When the CTL pulse with the correct period is supplied, the pulse which accords with this information must be generated immediately.

When the playback CTL pulse has been thrown into disarray or lost, a warning tone may be emitted and so the "MUTE" signal is output to the AN-01 board.
The "AFT" playback CTL pulse has its width increased by monostable multivibrator ICH22. The pulse width is initially expanded since it is reduced depending on the tape speed in a high-speed shuttle mode.

Next, the playback CTL pulse with its width increased is latched by the drum reference signal and a differential pulse is created. The continuity of the playback CTL pulse is detected from this pulse and the pulse formed by delaying the playback CTL pulse with an expanded width by one period, and the control detailed below is exercised in accordance with this state.

- **When the playback CTL pulse is continuously supplied in the proper period:**
  This mode is judged to be normal playback, and the playback audio frame pulse is output at the phase of the playback CTL pulse.
- **When the playback CTL pulse is supplied at a phase which differs from the current phase:**
  The frame pulse is output while the current phase is held. The audio output will be muted.
- **When the playback CTL pulse is not supplied:**
  The frame pulse is output while the current phase is held. The audio output will be muted if the playback CTL pulse is not supplied for 2 or more periods.

In the REC and EE modes, the audio frame pulse is generated from the free-running counter by the "SYSTEM F" system frame pulse.
The "MUTE" signal is also sent via the IF-139 board to the DVR-1000.

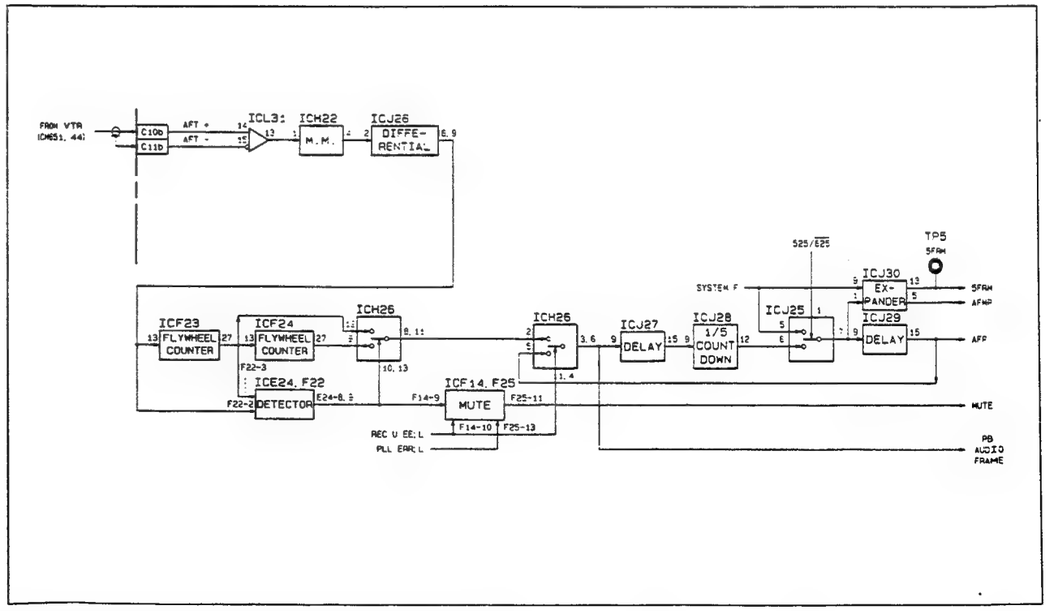



**Fig. 7-2-10. Audio Frame Pulse Generator (TG-28 Board)**

## 4-8. IF-139 BOARD

The DVPC-1000 is configured for the most part by digital and analog signal processing circuitry which is controlled by the IF-139 board via the universal peripheral interface (UPI) provided on each of the boards. The DVPC-1000 is also provided with a number of test mode functions which are also managed by the IF-139 board.

The IF-139 board also functions as the interface with the system control block of the DVR-1000, and for each field it engages in the exchange of the information listed below totaling approximately 150 bytes.

- Operation mode
- Control signal for signal processing system
- Time code data
- Audio level control data
- Error/alarm information

The IF-139 board can be roughly divided into two blocks: one is the microcomputer section which centers on the V20 microprocessor, and the other is the interface circuit and processor for the user data among the audio data.

### 1. Microcomputer (IF-139 board)

The microcomputer is composed of the V20 microprocessor (CPU: ICF2) and peripheral ICs. The V20 operates with a 7.5 MHz clock signal.

Table 8-1 is an address map. Addresses starting with "10000H" are not used.

| ADDRESS | DEVICE |
|---|---|
| 0 - 1FFFH | Main RAM (ICF6) |
| 2000 - 2FFFH | Boards (SY, CI, FM, VN, etc.) |
| 3000 - 3FFFH | WR/RD Port, Display Controller (ICF25) |
| 4000 - 47FFH | Interrupt Controller (ICH9) |
| 4800 - 4FFFH | CTC-1 (ICH6) |
| 5000 - 57FFH | CTC-2 (ICH7) |
| 5800 - 5FFFH | GPIB-1 (ICF11) |
| 6000 - 67FFH | GPIB-2 (ICF12) |
| 6800 - 6FFFH | Recording UCW RAM (ICH19) |
| 7000 - 77FFH | Playback UCW RAM (ICH22) |
| 7800 - 7FFFH | Playback UCW Flag RAM (ICH24) |
| 8000 - FFFFH | ROM (ICF4) |

**Table 8-1. Address Map (IF-139 Board)**



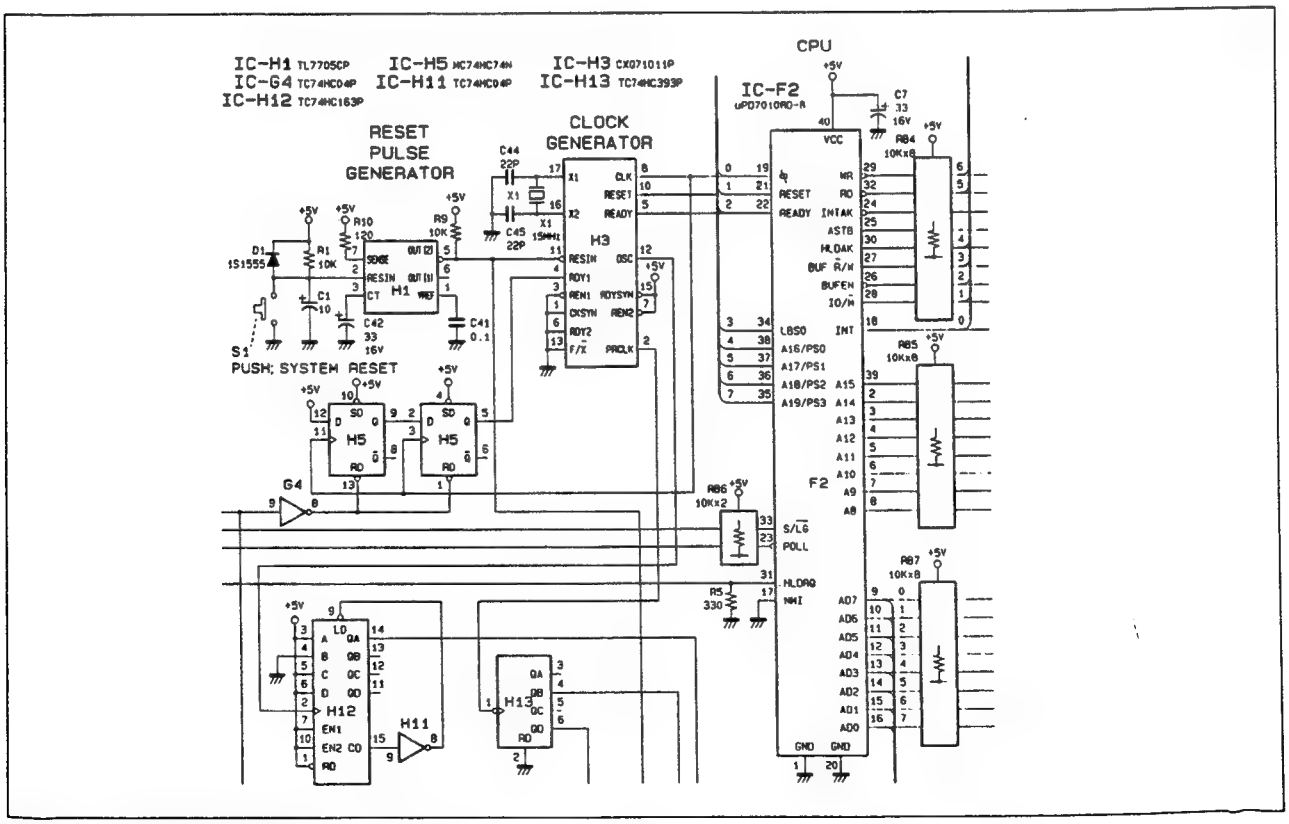



**Fig. 8-1. CPU (IF-139 Board)**

## 2. Clock Generator (IF-139 board)

This generates the clock signal which operates the CPU. This is also divided down to form the CTC count clock and reference frame pulse which are output.
The master oscillation frequency is 15 MHz and this is halved to generate the clock signal (7.5 MHz) which drives the CPU.

## 3. Reset Pulse Generator (IF-139 board)

The supply voltage is monitored by ICH1 and if it falls below the 4.7 V level for a continuous period of 1 microsecond or longer, this generator outputs the reset pulse to the CPU.

## 4. Servo Frame Selector (IF-139)

The reference frame pulse "SYS FR" generated by the TG-28 board is supplied to the DVR-1000 via the IF-139 board.
The servo frame selector monitors the period of the reference frame pulse which is output from the TG-28 board, and when it detects an error in the pulse, it switches over to the reference frame pulse which is provided by dividing down the CPU operating clock signal (7.5 MHz), and it supplies it to the DVR-1000. The results of determining the period of the reference frame pulse are output from pin 5 (high = error) of ICE6, these data are read in from the port and, after the statistics have been recorded, the reference frame pulse is switched by the ICD14 pin 13 output (low = INT mode, high = EXT mode).
This function is used in the case of a malfunction such as when an operating error causes the TG-28 board to generate a reference signal with a clearly different period. It enables the control system and servo system only of the DVR-1000 and DVPC-1000 to operate normally and communicate the malfunction on the DVPC-1000 side to the DVR-1000.

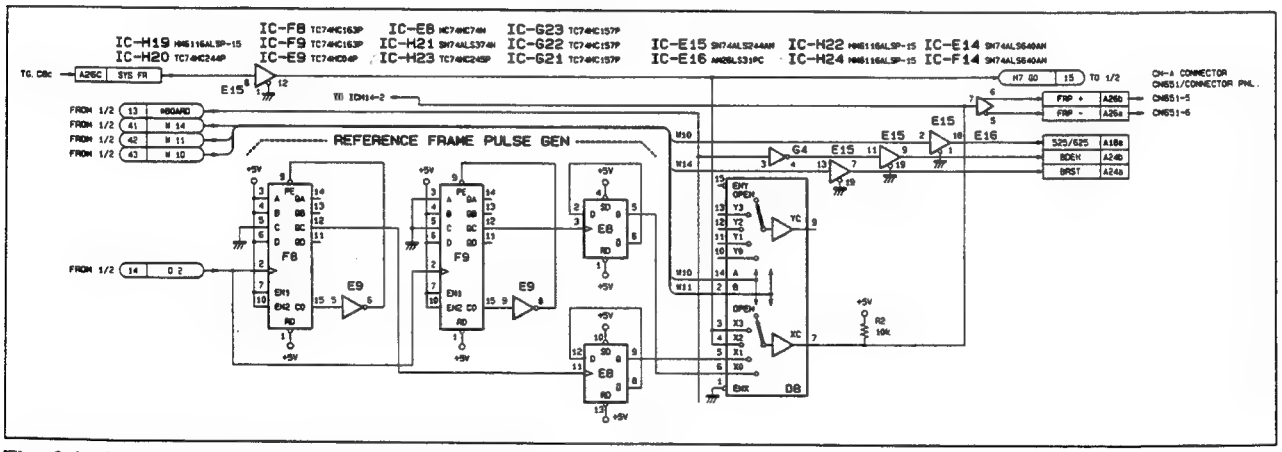


Fig. 8-2. Servo Frame Pulse Selector (IF-139 Board)

### 5. GPIB-1 driver (IF-139 board)

This circuit is provided to transfer data to and from the DVR-1000 via the CN-B connector on the rear panel.

### 6. GPIB-2 driver (IF-139 board)

This circuit provides a connection with the external terminal (microcomputer, etc.) via the GPIB connector on the rear panel.

### 7. I/O Ports (IF-139 board)

The setting statuses of the various switches on the IF-139 board are read at input port ICA1, B1 and C1. The monitor signals are output to the test points at output port ICD3, D4, D5 and D6 where the hardware and also the DP-60 board are controlled.
Communication with the UPI on the boards is provided by I/O port ICE14 and F15.

### 8. Display Control Circuit (IF-139 board)

This circuit generates the time code and other data which are superimposed onto the video signal.



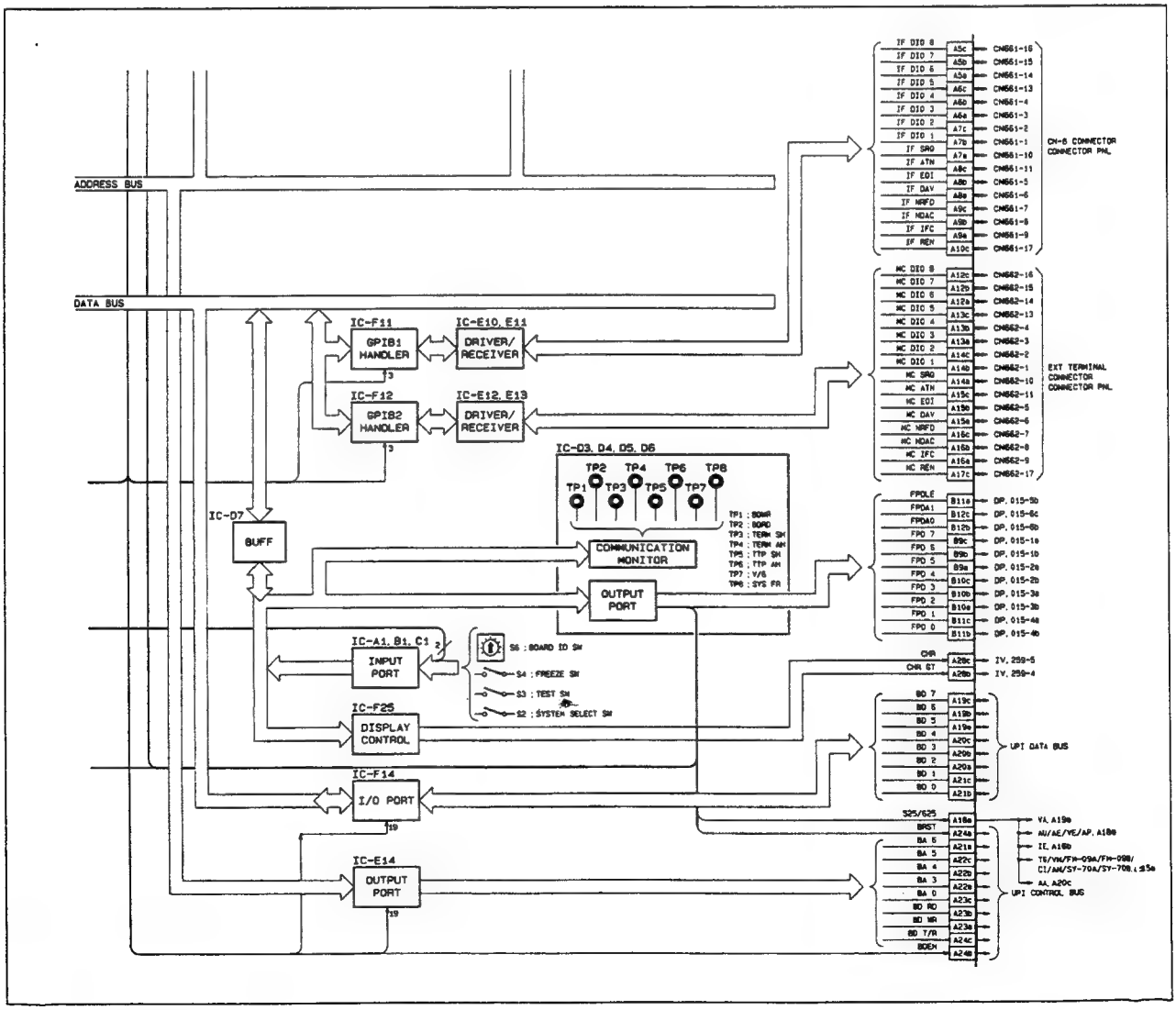



**Fig. 8-3. GPIB Driver/I/O Port (IF-139 Board)**

## 9. User Data Interface Circuit (IF-139 board)

The user data are recorded in the user areas to which 8 bytes are allocated for each audio code block.
The capacity per frame for each channel is 80 bytes for a 525/60 system and 96 bytes for a 625/50 system. Normally, this circuit functions as a peripheral circuit of the microprocessor but it is isolated from the microprocessor once per video frame and it transmits the user data to the audio processing system independently. This transfer sequence is initiated by the load pulse supplied from the port to the memory address counter ICF18 and F21.
This circuit employs the 3 buffer RAMs described below.

- RAM for the recording data (ICH19)
- RAM for the playback data (ICH22)
- RAM for the error flags of the playback data (ICH24)

The data are transferred in 4-bit parallel form by the 64 FAS (64×48 kHz) clock and this occurs once per video frame for both the recording data and playback data.

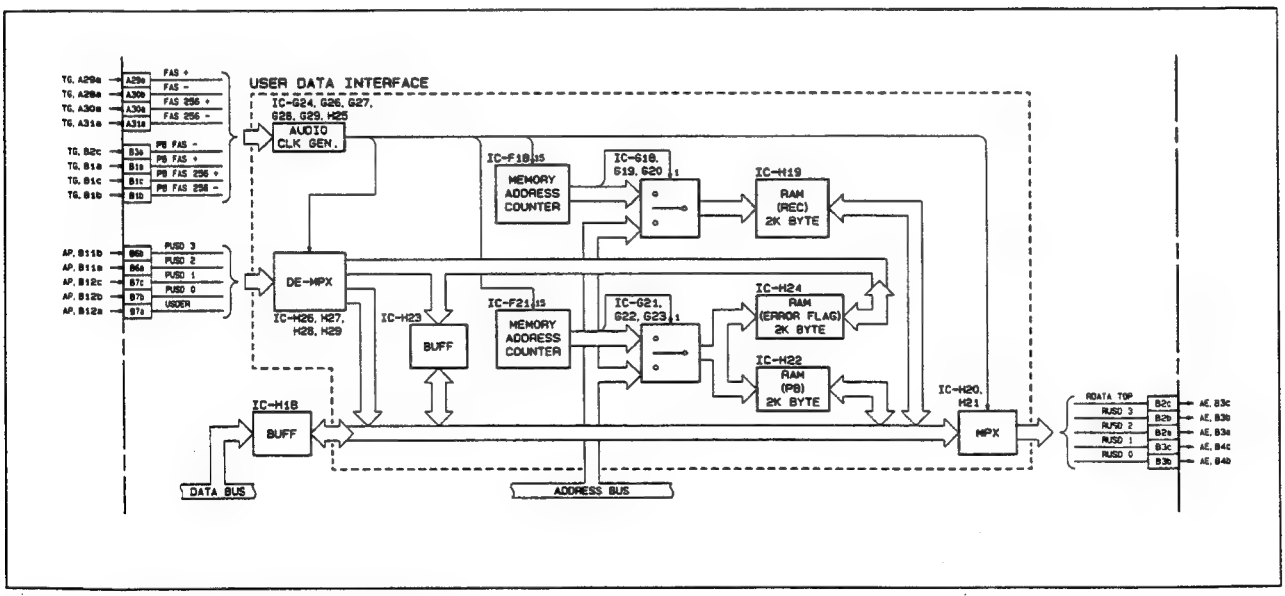



**Fig. 8-4. User Data Interface (IF-139 Board)**

# SECTION 5
# GENERAL INFORMATION FOR ALIGNMENT

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| RV101: | CH-1 LINE OUTPUT LEVEL | 8-5 |
| RV201: | CH-2 LINE OUTPUT LEVEL | 8-5 |
| RV301: | CH-3 LINE OUTPUT LEVEL | 8-5 |
| RV401: | CH-4 LINE OUTPUT LEVEL | 8-5 |
| RV501: | MONITOR 1(L) OUTPUT LEVEL | 8-14 |
| RV601: | MONITOR 2(R) OUTPUT LEVEL | 8-14 |
| RV701: | AUDIO MIX/CUE OUTPUT LEVEL | 8-16 |


### IE-17 BOARD


| | | Section |
|---|---|---|
| L11: | PLL (9.8362MHz REC CLOCK) FREQUENCY CONT | 7-5 |
| RV1: | PLL (9.8362MHz REC CLOCK) FREQUENCY CONT | 7-5 |


### IV-14 BOARD


| | | Section |
|---|---|---|
| RV1: | +12V CURRENT LIMIT | 9-3 |
| RV2: | -12V CURRENT LIMIT | 9-3 |
| RV3: | +12V OUTPUT VOLTAGE | 9-3 |
| RV4: | -12V OUTPUT VOLTAGE | 9-3 |
| RV5: | CHARACTER GAIN | 9-20 |
| RV6: | CHARACTER LEVEL | 9-20 |
| RV7: | ANALOG VIDEO OUTPUT R2 GAIN | 9-13 |
| RV8: | ANALOG VIDEO OUTPUT R1 GAIN | 9-13 |
| RV9: | ANALOG VIDEO OUTPUT B2 GAIN | 9-13 |
| RV10: | ANALOG VIDEO OUTPUT B1 GAIN | 9-13 |
| RV11: | ANALOG VIDEO OUTPUT G2 GAIN | 9-13 |
| RV12: | ANALOG VIDEO OUTPUT G1 GAIN | 9-13 |
| RV13: | BETACAM OUTPUT R-Y GAIN | 9-14 |
| RV14: | BETACAM OUTPUT B-Y GAIN | 9-14 |
| RV15: | BETACAM OUTPUT Y GAIN | 9-14 |
| RV16: | MONITOR OUTPUT G GAIN | 9-15 |
| RV17: | MONITOR OUTPUT B GAIN | 9-15 |
| RV18: | MONITOR OUTPUT R GAIN | 9-15 |
| RV19: | WAVEFORM MONITOR OUTPUT GAIN | 9-15 |
| RV20: | VA-45 OUTPUT G OUTPUT GAIN | 9-5 |
| RV21: | VA-45 OUTPUT B OUTPUT GAIN | 9-5 |
| RV22: | VA-45 OUTPUT R OUTPUT GAIN | 9-5 |
| RV23: | ANALOG VIDEO INPUT-1 G GAIN | 9-4 |
| RV24: | ANALOG VIDEO INPUT-1 G OFFSET | 9-4 |
| RV25: | ANALOG VIDEO INPUT-1 B GAIN | 9-4 |
| RV26: | ANALOG VIDEO INPUT-1 B OFFSET | 9-4 |
| RV27: | ANALOG VIDEO INPUT-1 R GAIN | 9-4 |
| RV28: | ANALOG VIDEO INPUT-1 R OFFSET | 9-4 |
| RV29: | BETACAM INPUT Y GAIN | 9-17 |
| RV30: | BETACAM INPUT Y OFFSET | 9-17 |
| RV31: | BETACAM INPUT B-Y GAIN | 9-17 |
| RV32: | BETACAM INPUT B-Y OFFSET | 9-17 |
| RV33: | BETACAM INPUT R-Y GAIN | 9-17 |
| RV34: | BETACAM INPUT R-Y OFFSET | 9-17 |
| RV35: | CH4 AUDIO INPUT GAIN | 8-6 |
| RV36: | CH3 AUDIO INPUT GAIN | 8-6 |
| RV37: | CH2 AUDIO INPUT GAIN | 8-6 |
| RV38: | CH1 AUDIO INPUT GAIN | 8-6 |
| RV39: | ANALOG VIDEO INPUT-1 SYNC OFFSET | 9-4 |

**PG-13 BOARD**


| | | Section |
|---|---|---|
| RV2: | D-MIX GAIN | 8-15 |


**SY-70 BOARD**


| | | Section |
|---|---|---|
| LV1: | A/C-CH PLL FREQUENCY | 7-4-2 |
| LV2: | B/D-CH PLL FREQUENCY | 7-4-2 |
| RV1: | SPEED INFORMATION OFFSET | 7-4-2 |
| RV2: | A/C-CH SPEED INFORMATION GAIN | 7-4-1<br>7-4-4 |
| RV3: | B/D-CH SPEED INFORMATION GAIN | 7-4-1<br>7-4-4 |
| RV4: | A/C-CH PLL CLOCK BALANCE | 7-4-1<br>7-4-3 |
| RV5: | A/C-CH PLL LOOP GAIN | 7-4-1 |
| RV6: | B/D-CH PLL CLOCK BALANCE | 7-4-1<br>7-4-3 |
| RV7: | B/D-CH PLL LOOP GAIN | 7-4-1 |


**TG-28 BOARD**


| | | Section |
|---|---|---|
| RV1: | 525/625 DETECTION SENSIVITY | 7-2 |
| RV2: | PLL NO.3 (CX773B CLOCK) FREQ.CONT | 7-3-3 |
| RV3: | PLL NO.4 (27MHz CLOCK) FREQ.CONT | 7-3-4 |
| RV4: | PLL NO.2 (12.288MHz CLOCK) FREQ.CONT | 7-3-2 |
| RV5: | PLL NO.1 (27MHz REC CLOCK) FREQ.CONT | 7-3-1 |


**VA-45 BOARD**


| | | Section |
|---|---|---|
| RV101: | R/R-Y INPUT SIGNAL OFFSET | 9-6 |
| RV102: | R/R-Y SIGNAL GAIN | 9-6 |
| RV104: | MATRIX | 9-7 |
| RV105: | R-Y GAIN OFFSET | 9-7 |
| RV106: | R-Y FREQ. RESP | 9-19 |
| RV107: | R-Y GAIN | 9-12 |
| RV108: | R-Y CLAMP | 9-11 |
| RV109: | -2V VOLTAGE CONT | 9-10 |
| RV201: | B/B-Y SIGNAL OFFSET | 9-6 |
| RV202: | B/B-Y SIGNAL GAIN OFFSET | 9-6 |
| RV204: | MATRIX | 9-7 |
| RV205: | B-Y GAIN OFFSET | 9-7 |
| RV206: | B-Y FREQ. RESP | 9-19 |
| RV207: | B-Y GAIN | 9-12 |
| RV208: | B-Y CLAMP | 9-11 |
| RV209: | -2V VOLTAGE CONT | 9-10 |
| RV301: | G/Y SIGNAL OFFSET | 9-6 |
| RV302: | G/Y SIGNAL GAIN OFFSET | 9-6 |
| RV303: | OFFSET | 9-18 |
| RV305: | Y GAIN OFFSET | 9-7 |
| RV306: | Y FREQ. RESP | 9-19 |
| RV307: | Y GAIN | 9-12 |
| RV308: | Y CLAMP | 9-11 |
| RV309: | -2V VOLTAGE CONT | 9-10 |
| RV401: | D/A R-Y GAIN | 9-8 |
| RV403: | D/A OUTPUT R-Y FREQ. RESP | 9-19 |
| RV404: | DEMATRIX | 9-8 |
| RV501: | D/A B-Y GAIN | 9-8 |
| RV503: | D/A OUTPUT B-Y FREQ. RESP | 9-19 |
| RV504: | DEMATRIX | 9-8 |
| RV601: | D/A Y GAIN | 9-8 |
| RV603: | D/A OUTPUT Y FREQ. RESP | 9-19 |
| RV604: | DEMATRIX | 9-8 |
| RV605: | G LEVEL | 9-8 |
| RV606: | OFFSET | 9-9 |
| RV702: | Y ADD SYNC LEVEL | 9-9 |
| RV703: | Y ADD OFFSET | 9-9 |
| RV704: | SYNC ADDITION LEVEL | 9-9 |
| RV704: | BETACAM OUT Y LEVEL | 9-9 |
| RV801: | +12V OVER CURRENT | 9-2 |
| RV802: | +12V VOLTAGE CONT | 9-2 |
| RV831: | -12V OVER CURRENT | 9-2 |
| RV832: | -12V VOLTAGE CONT | 9-2 |
| RV861: | -5V OVER CURRENT | 9-2 |
| RV862: | -5V VOLTAGE CONT | 9-2 |

## 5-2. EQUIPMENT REQUIRED

1. **Component Test Signal Generator**
   TEKTRONIX Type TSG-300 or Equivalent

2. **Waveform Monitor**
   TEKTRONIX Type WFM-300 or Equivalent

3. **Oscilloscope**
   TEKTRONIX Type 2465A or Equivalent

4. **Frequency Counter**

5. **Audio Distortion Analyzer**
   TEKTRONIX Type AA5001 or Equivalent

6. **Audio Oscillator**
   TEKTRONIX Type SG5010 or Equivalent

7. **Digital Voltmeter**
   Effective digits; more than 5 digits
   Accuracy; less than 0.02% ±1 count

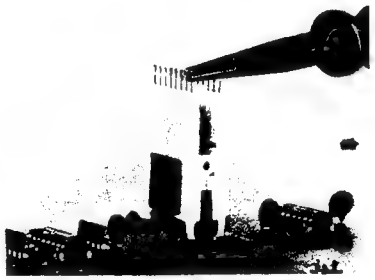
8. **Picture Monitor**

9. **Digital Cassette VTR**
   SONY DVR-1000

10. **Extender; EX-131 (Supplied with DVPC-1000)**
    SONY Part No. A-6001-008-A

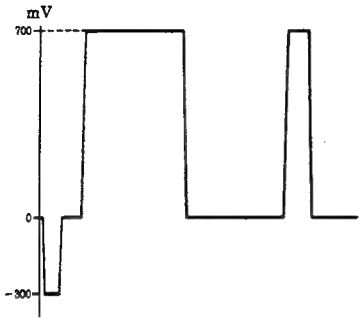
11. **Alignment Tape** — **SONY Part No.**
    525/60 System; BR-5-1A 8-960-070-01
    625/50 System; BR-5-1B 8-960-070-51

12. **IC Test Clip**
    Type TC-16: SONY Part No. J-6041-770-A
    Type TC-20: SONY Part No. J-6041-780-A
    Manufacture:
    AP PRODUCTS INCORPORATED
    P.O.Box 697, 72 Corwin Drive
    Peinesville, Ohio 44077, U.S.A
    Tel: (216) 354-2101
    When connection the test probe to the terminal of DIP integrated circuit, these clips are convenient. Type TP-16 is for DIP 14-pin or 16-pin IC and Type TC-20 is for 18-pin or 20-pin IC.

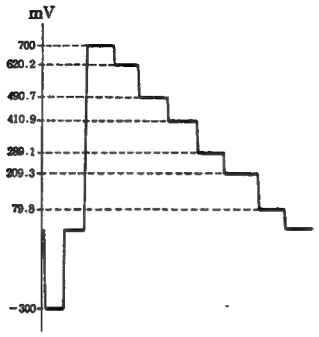


## 5-3. TEST SIGNAL

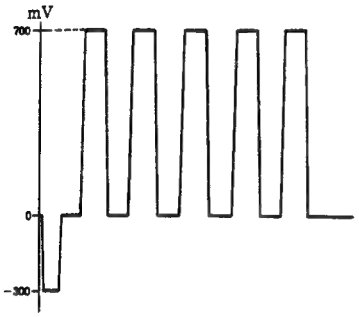
COLOR BARS



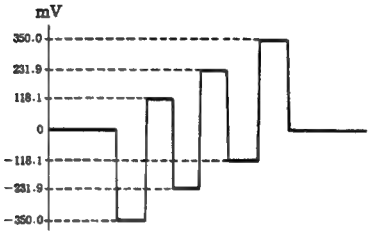

G Channel



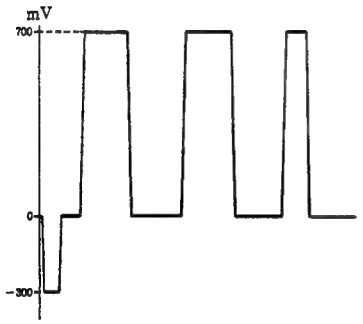

Y Channel



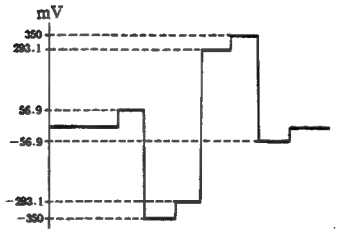

B Channel




B-Y Channel

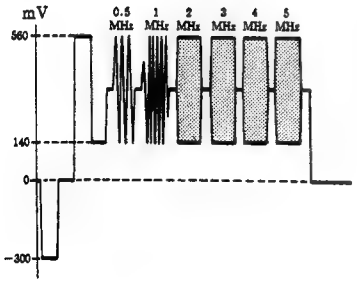



R Channels

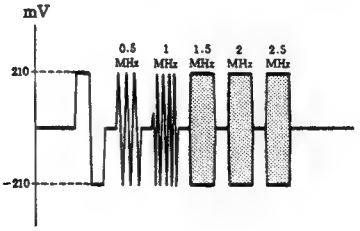



R-Y Channels

MULTI BURST



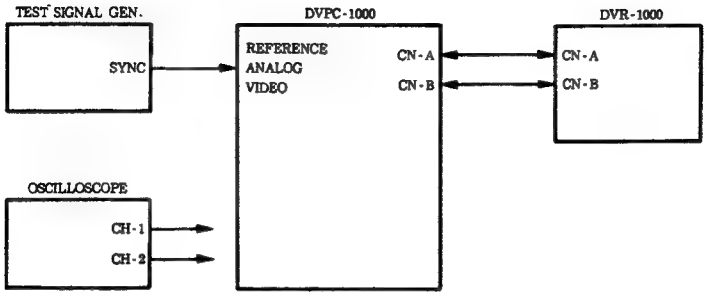

Y Channel



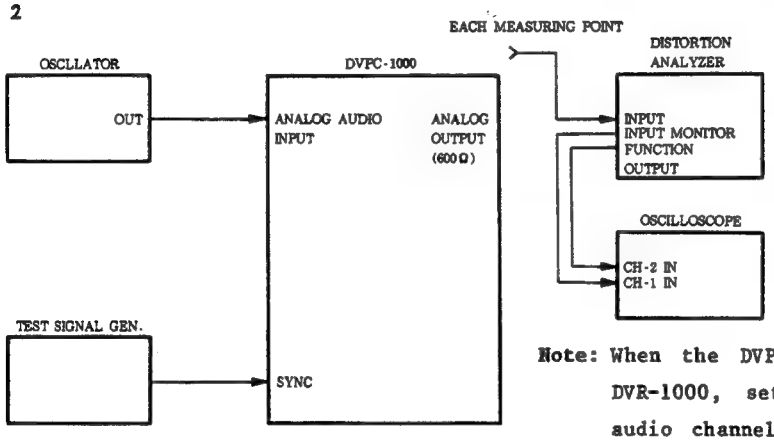

B-Y and R-Y Channels

## 5-4. CONNECTION OF THE EQUIPMENT

**Connection 1**

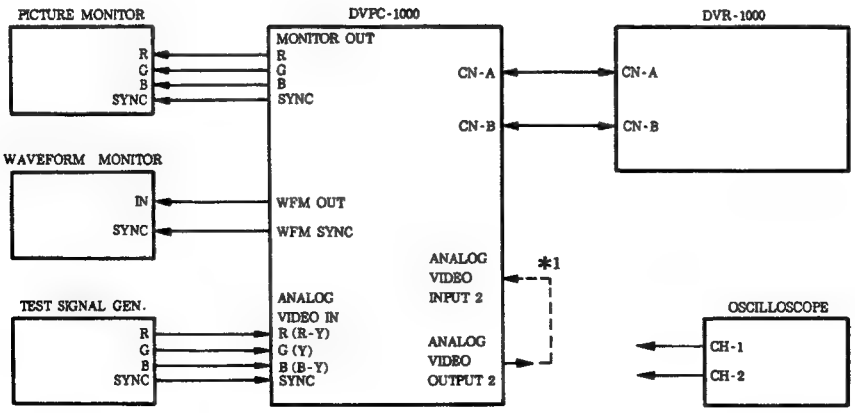



**Connection 2**




**Note:** When the DVPC-1000 is connected with the DVR-1000, set the audio emphasis of all audio channels to the OFF position before aligning the audio signal system. The emphasis ON/OFF switch can be set by the DIGITAL AUDIO RECORDING SETUP sub menu. When the DVR-1000 is not connected, the emphasis ON/OFF switch is automatically set to the OFF position.

**Connection 3**




*1: Connect the ANALOG VIDEO INPUT2 connector and the ANALOG VIDEO OUTPUT2 connector only for adjustments in section 9-17 and 9-18.

## 5-5. INITIAL SETTING OF THE SWITCHES/JUMPERS

**AA-29 BOARD**

```
S101:  CH-1 ANALOG AUDIO INPUT LEVEL
       PRE/VAR SW.....PRESET
S201:  CH-2 ANALOG AUDIO INPUT LEVEL
       PRE/VAR SW.....PRESET
S301:  CH-3 ANALOG AUDIO INPUT LEVEL
       PRE/VAR SW.....PRESET
S401:  CH-4 ANALOG AUDIO INPUT LEVEL
       PRE/VAR SW.....PRESET
S501:  CH-1 ANALOG AUDIO OUTPUT LEVEL
       PRE/VAR SW.....PRESET
S601:  CH-2 ANALOG AUDIO OUTPUT LEVEL
       PRE/VAR SW.....PRESET
S701:  CH-3 ANALOG AUDIO OUTPUT LEVEL
       PRE/VAR SW.....PRESET
S801:  CH-4 ANALOG AUDIO OUTPUT LEVEL
       PRE/VAR SW.....PRESET

CN111/112(JP101/102):
       CH-1 FEEDBACK ON/OFF.....CN111(JP101)
CN211/212(JP201/202):
       CH-2 FEEDBACK ON/OFF.....CN211(JP201)
CN311/312(JP301/302):
       CH-3 FEEDBACK ON/OFF.....CN311(JP301)
CN411/412(JP401/402):
       CH-4 FEEDBACK ON/OFF.....CN411(JP401)
```

**AE-06 BOARD**

```
CN1(JP1):
       UPI TEST.....OPEN
CN2:   VERSION SELECT.....*1
```

**AN-01 BOARD**

```
S1-1:  CONCEALMENT OFF SW.....OFF
S1-2:  MUTE INHIBIT SW.....OFF
S1-3:  BYPASS;DIGITAL AUDIO BYPASS SW..OFF
S1-4:  Always set to off.
S1-5:  Always set to off.
S1-6:  Always set to off.
S1-7:  Always set to off.
S1-8:  Always set to off.
S2:    MUTING TIME SW.....7
S3:    MUTING DELAY SELECT SW.....B
S4:    DIGITAL AUDIO OUTPUT DELAY SW
       (LSD).....1
S5:    DIGITAL AUDIO OUTPUT DELAY SW
       (MSD).....2
S6:    ADVANCE AUDIO DELAY SW (LSB)....7
S7:    ADVANCE AUDIO DELAY SW (MSB)....C
S8:    ADVANCE RETURN DELAY SW (LSB)...F
S9:    ADVANCE RETURN DELAY SW (MSB)...F
S10:   Not used.

JP1:   UPI TEST.....OPEN
JP2:   ADVANCE AUDO MONITOR ON SW.....OPEN
JP3:   Always open.
```

**AP-14 BOARD**

```
S1:    ADVANCE RETURN DELAY(MSB).....2
S2:    ADVANCE RETURN DELAY(LSB).....0
S3:    PB AUDIO DELAY (MSB).....6(625)/7(525)
S4:    PB AUDIO DELAY (LSB).....6(625)/5(525)

CN1(JP1):
       UPI TEST .....OPEN
```

*1; Set as follows depending on the software version of ROM (ICF4) on the IF-139 board.
ICF4; IF1390127 and later versions.....OPEN
IF1390126 and earlier versions...SHORT

**AT-45 BOARD**

```
JP101/102:
       CH-1 ANALOG AUDIO OUTPUT LEVEL..JP102
JP201/202:
       CH-2 ANALOG AUDIO OUTPUT LEVEL..JP202
JP301/302:
       CH-3 ANALOG AUDIO OUTPUT LEVEL..JP302
JP401/402:
       CH-4 ANALOG AUDIO OUTPUT LEVEL..JP402
```

**AU-86 BOARD**

```
S1:    AUDIO TEST SIGNAL SELECT SW.....0
S2:    AUDIO INPUT SELECT XLR/DSUB SW..DSUB
S3:    AUDIO INPUT SELECT DIG/ANA SW...ANA
S4-1:  TEST SIGNAL ENABLE SW.....OFF
S4-2:  Not used.
S4-3:  CH-4 RECORD DATA SELECT SW.....OFF
S4-4:  CH-3 RECORD DATA SELECT SW.....OFF
S4-5:  CH-2 RECORD DATA SELECT SW.....OFF
S4-6:  CH-1 RECORD DATA SELECT SW.....OFF
S4-7:  CH-1/2 INPUT MODE SELECT MONO/
       STEREO SW.....OFF
S4-8:  CH-3/4 INPUT MODE SELECT MONO/
       STEREO SW.....OFF

CN1(JP1):
       UPI TEST.....OPEN
CN2:   VERSION SELECT.....*1
```

**CI-01 BOARD**

```
SW101-1: INNER CORECTION OFF SW.....ON
SW101-2: AUDIO OUTER CORRECTION OFF SW.OFF
SW101-3: BYPASS-3 SW.....OFF
SW101-4: INTER CHANGE ON SW.....OFF
SW101-5: INNER DECODER BYPASS TEST SW..OFF
SW101-6: SWAP TEST DIRECTION SW.....OFF
SW101-7: Not used.
SW101-8: Not used.

CN5:     BOARD VERSION.....*2
CN6:     UPI TEST.....OPEN
CN7:     SWAP TEST.....OPEN
```

**FM-09A,B BOARD**

```
S1-1:  DE-SHUFFLING THROUGH SW.....OFF
S1-2:  BYPASS-4 SW.....OFF
S1-3:  TEMPORAL CONCEALMENT OFF SW.....ON
S1-4:  Not used.
S1-5:  OUTER CORRECTION OFF.....ON
S1-6:  Not used.
S1-7:  Not used.
S1-8:  Not used.

S2-1:  Always set to off.
S2-2:  Always set to off.
S2-3:  Always set to off.
S2-4:  Always set to off.
S2-5:  Always set to off.
S2-6:  Always set to off.
S2-7:  Always set to off.
S2-8:  INHIBIT CH SELECT SW.....OFF

S3-1:  Always set to off.
S3-2:  FRAME MEMORY TEST SW.....OFF
S3-3:  Always set to off.
S3-4:  1H DE-SHUFFLE MEMORY TEST SW....OFF
S3-5:  Always set to off.
S3-6:  Always set to off.
S3-7:  OUTPUT DATA INHIBIT SW.....OFF
S3-8:  Always set to off.
```

*2; Set as follows depending on the last two digits of the CI-01 board number.
The boards with the last two-digit number of 11; OPEN
The boards with the last two-digit number of 12 or greater; SHORT

S4 to S9:
Not used.

CN5: UPI TEST.....OPEN
CN6: TEST ENABLE.....OPEN
CN7: Always open.
CN8: Always open.
CN9: Always open.
CN10: HEAD DE-INTERLEAVE FLAG TEST....OPEN
CN11: Always open.
CN12: A/C-CH FRAME MEMORY READ INHIBIT.....OPEN
CN13: BYPASS-4:A/C-CH DATA INPUT INHIBIT.....OPEN
CN21: Always open.
CN22: B/D-CH FRAME MEMORY READ INHIBIT.....OPEN
CN23: BYPASS 4:B/D-CH INPUT DATA INHIBIT.....OPEN

**IE-17 BOARD**

*1 S1-1: B/D-CH DELAY SW.....ON
S1-2: B/D-CH DELAY SW.....OFF
S1-3: B/D-CH DELAY SW.....ON
S1-4: B/D-CH DELAY SW.....OFF
S1-5: B/D-CH DELAY SW.....OFF
S1-6: B/D-CH DELAY SW.....ON
S1-7: B/D-CH DELAY SW.....OFF
S1-8: B/D-CH DELAY SW.....OFF

*1 S2-1: EE DELAY SW (525/60 SYSTEM).....ON
S2-2: EE DELAY SW (525/60 SYSTEM).....OFF
S2-3: EE DELAY SW (525/60 SYSTEM).....OFF
S2-4: EE DELAY SW (525/60 SYSTEM).....ON
S2-5: EE DELAY SW (525/60 SYSTEM).....OFF
S2-6: EE DELAY SW (525/60 SYSTEM).....ON
S2-7: EE DELAY SW (525/60 SYSTEM).....OFF
S2-8: EE DELAY SW (525/60 SYSTEM).....ON

*1 S3-1: EE DELAY SW (625/50 SYSTEM).....ON
S3-2: EE DELAY SW (625/50 SYSTEM).....ON
S3-3: EE DELAY SW (625/50 SYSTEM).....OFF
S3-4: EE DELAY SW (625/50 SYSTEM).....OFF
S3-5: EE DELAY SW (625/50 SYSTEM).....OFF
S3-6: EE DELAY SW (625/50 SYSTEM).....ON
S3-7: EE DELAY SW (625/50 SYSTEM).....OFF
S3-8: EE DELAY SW (625/50 SYSTEM).....ON

CN1: SCRAMBLE INHIBIT.....OPEN
CN2: COMPULSORY REC.....OPEN
CN3: Always open.

*1; Do not change these setting conditions because they are determined by the mechanical dimensions.

**IF-139 BOARD**

S1: SYSTEM RESET SW .....OFF
S2: SYSTEM SELECT:525/625 SW.....Depend on usage.
S3: TEST ON/OFF SW.....OFF
S4: FREEZE SW.....OFF
S5: GPIB SET ADDRESS.....0
S6: BOARD ID SW.....0

**IV-14 BOARD**

JP1/2: ANALOG AUDIO INPUT IMPEDANCE CH-4.....JP1
JP3/4/5/6: ANALOG AUDIO INPUT LEVEL CH-4...JP4/5
JP7/8: ANALOG AUDIO INPUT IMPEDANCE CH-3.....JP7
JP9/10/11/12: ANALOG AUDIO INPUT LEVEL CH-3...JP10/11
JP13/14: ANALOG AUDIO INPUT IMPEDANCE CH-2.....JP13
JP15/16/17/18: ANALOG AUDIO INPUT LEVEL CH-2...JP16/17
JP19/20: ANALOG AUDIO INPUT IMPEDANCE CH-1.....JP19
JP21/22/23/24: ANALOG AUDIO INPUT LEVEL CH-1...JP22/23

**PG-13 BOARD**

S1: AUDIO TEST SIGNAL SELECT SW.....0
S2-1: AUDIO MONITOR SELECT 1 SW.....OFF
S2-2: AUDIO MONITOR SELECT 2 SW.....OFF
S2-3: AUDIO EMPHASIS ON/OFF SW.....OFF
S2-4: AUDIO DE-EMPHASIS ON/OFF SW.....OFF
S2-5: AUDIO DIGITAL MIX CH-1 ON/OFF SW.....OFF
S2-6: AUDIO DIGITAL MIX CH-2 ON/OFF SW.....OFF
S2-7: AUDIO DIGITAL MIX CH-3 ON/OFF SW.....OFF
S2-8: AUDIO DIGITAL MIX CH-4 ON/OFF SW.....OFF
S3-1: BYPASS-6 SW.....OFF
S3-2: TEST-6:VIDEO TEST SIGNAL OUTPUT SW.....OFF
S3-3: BYPASS-7 SW.....OFF
S3-4: TEST-7:AUDIO TEST SIGNAL OUTPUT.OFF
S3-5: ANALOG VIDEO OUTPUT SELECT: RGB Y/R-Y/B-Y SW.....OFF
S3-6: PB BYPASS:INPUT CHECK SW.....OFF
S3-7: Not used.
S3-8: Not used.
S4: VIDEO INPUT SELECT :RGB/Y,R-Y, B-Y SW.....RGB
S5: VIDEO INPUT CONNECTOR SELECT BNC/MULTI SW.....BNC

JP1/2: UPI TEST.....OPEN

**SY-70A,B BOARD**

S1-1: A/C-CH DATA INHIBIT SW.....OFF
S1-2: B/D-CH DATA INHIBIT SW.....OFF
S1-3: BYPASS-1;SERIAL EE SW.....OFF
S1-4: BYPASS-2;PARALLEL EE SW.....OFF
S1-5: SWAP1 TEST SW(TBC IN).....OFF
S1-6: SWAP1 TEST DIRECTION SW.....OFF
S1-7: SWAP2 TEST SW(TBC OUT).....OFF
S1-8: SWAP2 TEST DIRECTION/ERROR ADD CH SELECT.....OFF
S2: ERROR ADD SIZE SW(LSB).....Used on testing.
S3: ERROR ADD SIZE SW(MSB).....Used on testing.
S4: ERROR ADD POSITION SW(LSB).....Used on testing.
S5: ERROR ADD POSITION SW(MSB).....Used on testing.
S6: ERROR ADD SIZE SW(SAMPLE).....Used on testing.
S7: ERROR ADD TEST MODE SELECT SW...Used on testing.

CN5: TBC MEMORY TEST1.....OPEN
CN6: UPI TEST.....OPEN
CN7: TBC MEMORY TEST2.....OPEN
CN8: DE-SCRAMBLE INHIBIT.....OPEN
CN9: ERROR ADD TEST.....OPEN
CN10: SWAP TEST ENABLE.....OPEN
CN11: JUMP TEST ENABLE.....OPEN
CN12: TEST SIGNAL OUTPUT.....OPEN

**TG-28 BOARD**

S1: ADVANCE AUDIO DELAY CONT (625/50).....4
S2: ADVANCE AUDIO DELAY CONT (525/60).....6
S3: SPOT ERASE FADE TIME CONT .....2
S4: CONFI AUDIO DELAY(625/50).....3
S5: CONFI AUDIO DELAY(525/60).....E
S6-1: TEST SW.....OFF
S6-2: TEST SW.....OFF
S6-3: TEST SW.....OFF
S6-4: TEST SW.....OFF
S6-5: TEST SW.....OFF
S6-6: TEST SW.....OFF
S6-7: TEST SW.....OFF
S6-8: TEST SW.....OFF
S7: REFERENCE INPUT SELECT DIG/ANA SW.....ANA

CN1: UPI TEST .....OPEN

**VA-45 BOARD**

S1-1: TEST SIGNAL SELECT SW.....OFF
S1-2: OFFSET ON/OFF SW.....OFF
S1-3: Not used.
S1-4: Not used.
S1-5: Not used.
S1-6: Not used.
S1-7: Not used.
S1-8: Not used.

S2-1: Not used.
S2-2: V BLANKING SELECT SW.....OFF
S2-3: V BLANKING SELECT SW.....OFF
S2-4: V BLANKING SELECT SW.....OFF
S2-5: V BLANKING SELECT SW.....OFF
S2-6: V BLANKING SELECT SW.....OFF
S2-7: V BLANKING SELECT SW.....OFF
S2-8: V BLANKING SELECT SW.....OFF

S3-1: V BLANKING SELECT SW.....OFF
S3-2: V BLANKING SELECT SW.....OFF
S3-3: V BLANKING SELECT SW.....OFF
S3-4: V BLANKING SELECT SW.....OFF
S3-5: V BLANKING SELECT SW.....OFF
S3-6: Not used.
S3-7: Not used.
S3-8: Not used.

S101: ANALOG VIDEO INPUT LEVEL PRE/VAR SW.....PRESET
S701: ANALOG VIDEO OUTPUT LEVEL PRE/VAR SW.....PRESET

CN5/6(JP5/6):
Y DIGITAL DELAY.....CN6(JP6)
CN7/8(JP7/8):
R-Y DIGITAL DELAY.....CN8(JP8)
CN9/10(JP9/10):
B-Y DIGITAL DELAY.....CN10(JP10)
CN11/12(JP11/12):
Y DIGITAL DELAY.....CN11(JP11)
CN13/14/15/16/17(JP13/14/15/16/17):
D/A C CLOCK.....*2
CN18/19/20/21/22(JP18/19/20/21/22):
D/A Y CLOCK.....*2
CN23/24(JP23/24):
D/A CLOCK.....*2
CN25/26/27/28/29(JP25/26/27/28/29):
A/D Y CLOCK.....*2
CN30/31(JP30/31):
A/D CLOCK.....*2
CN32/33/34/35/36(JP32/33/34/35/36):
A/D C CLOCK.....*2
CN37/38(JP37/38):
SETUP DELETE ON/OFF.....CN38(JP38)
CN39/40(JP39/40):
INPUT BETACAM MASK.....CN39(JP39)

*2: These jumpers are used for clock adjustment of the A/D and D/A converters. Do not change the settings of jumper plugs.

**VE-12 BOARD**

S1-1: MAPPING OFF SW.....OFF
S1-2: SHUFFLING OFF SW.....OFF
S1-3: BYPASS-3 SW.....OFF
S1-4: BYPASS-4 SW.....OFF
S1-5: BYPASS-5 SW.....OFF
S1-6: Not used.
S1-7: Not used.
S1-8: Not used.
S2: VIDEO INPUT SELECT DIG/ANA SW...ANA

CN1: UPI TEST.....OPEN

**VN-01 BOARD**

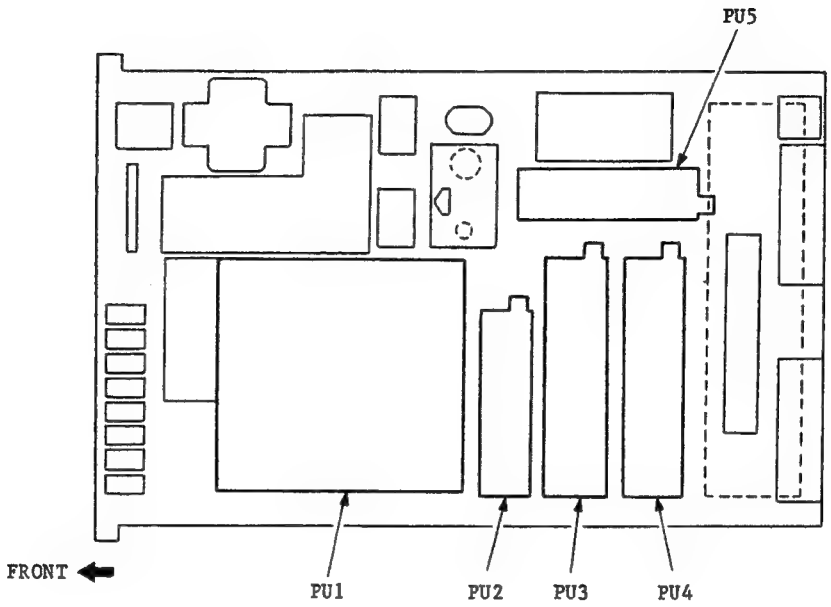
S1-1: DE-MAPPING OFF SW.....OFF
S1-2: CONCEALMENT OFF SW.....OFF
S1-3: BYPASS-5 SW.....OFF
S1-4: Always set to off.
S1-5: Always set to off.
S1-6: Always set to off.
S1-7: PINK DISPLAY ON/OFF SW.....OFF
S1-8: Not used.
S2-1: ERROR ADD TEST SW.....OFF
S2-2: CONCEALMENT ALGORITHM CONTROL...OFF
S2-3: CONCEALMENT ALGORITHM CONTROL...OFF
S2-4: CONCEALMENT ALGORITHM CONTROL...OFF
S2-5: CONCEALMENT ALGORITHM CONTROL...OFF
S2-6: IDEAL DIR DISPLAY SW.....OFF
S2-7: DISPLAY CONT 1.....OFF
S2-8: DISPLAY CONT 2.....OFF
S3: Not used.
S4/5: DIGITAL DELAY SW.....*3

CN1: ERROR PATTERN SELECT (ERV).....OPEN
CN2: ERROR PATTERN SELECT (ERV).....OPEN
CN3: ERROR PATTERN SELECT (ERV).....OPEN
CN4: ERROR PATTERN SELECT (ERH).....OPEN
CN5: ERROR PATTERN SELECT (ERH).....OPEN
CN6: ERROR PATTERN SELECT (ERH).....OPEN
CN7: ERROR PATTERN MODE SELECT.....OPEN
CN8: ERROR PATTERN MODE SELECT.....OPEN
CN9: CONCEALMENT RATE DISPLAY MODE...OPEN
CN10: CONCEALMENT RATE DISPLAY MODE...OPEN
CN11: CONCEALMENT RATE DISPLAY MODE...OPEN
CN12: CONCEALMENT RATE DISPLAY MODE...SHORT
CN14: UPI TEST.....OPEN

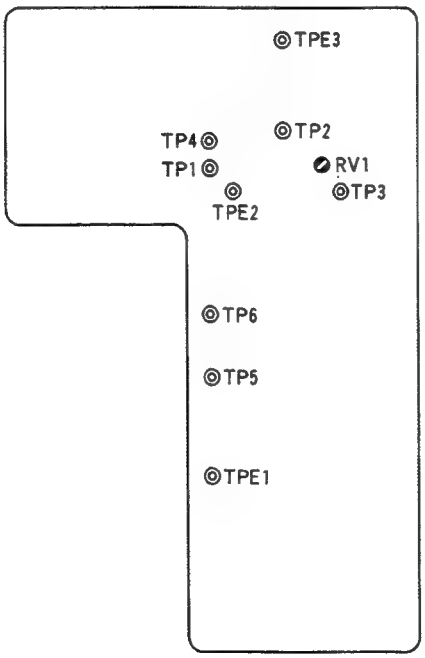
*3: Do not chang the settings. They have already been adjusted.

# SECTION 6
# POWER SUPPLY ALIGNMENT

**Power supply unit**




**AC-69 board (component side)**



## 6-1. VOLTAGE ADJUSTMENT

Equipment; Digital voltmeter
Setting of Switches & Controls;
Same as section 5-5

**Step 1.**
Check that the breaker is on.

**Step 2.**
Turn the power switch on and check that the AC input voltage is within ±10% of the specified voltage.

**Step 3.**
Set RV1 ( on the AC-69 board ) to the mechanical center position.

**Step 4. Adjustment**
Check the following voltages on the MB-132 board.

**Note:** All the voltages are measured by regarding SYSTEM GND CN041 on the MB-132 board as the reference voltage.

① +5 V voltage check
CN034/MB-132 = +5.00 ± 0.25 Vdc
Switching regulator PU1(+5 V)
Output level control on the front side

② -5 V voltage check
PIN1/CN043/MB-132 = -5.1 ± 0.1 Vdc
Switching regulator PU2(-5 V)
Output level control on the front side

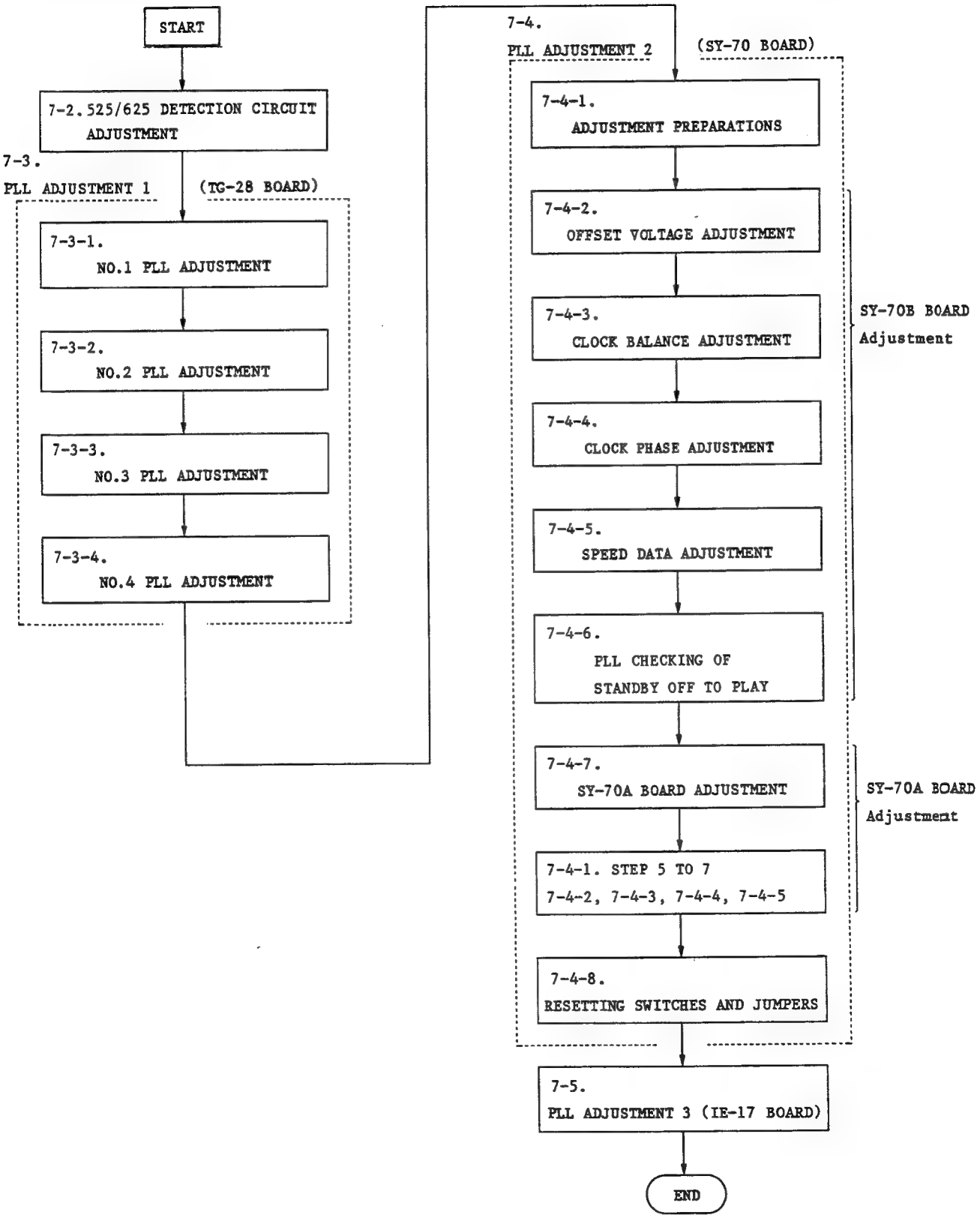
③ -18 V voltage check
PIN1/CN045/MB-132 = -18.00 ± 0.36 Vdc
Switching regulator PU3(-18 V)
Output level control on the front side

④ +18 V voltage check
PIN4/CN045/MB-132 = +18.00 ± 0.36 Vdc
Switching regulator PU4(+18 V)
Output level control on the front side

⑤ +12 V voltage check
PIN6/CN043/MB-132 = +12.00 ± 0.24 Vdc
Switching regulator PU4(+12 V)
Output level control on the front side

# SECTION 7
# CLOCK AND CONTROL SIGNAL SYSTEM ALIGNMENT

## 7-1. ALIGNMENT SEQUENCE

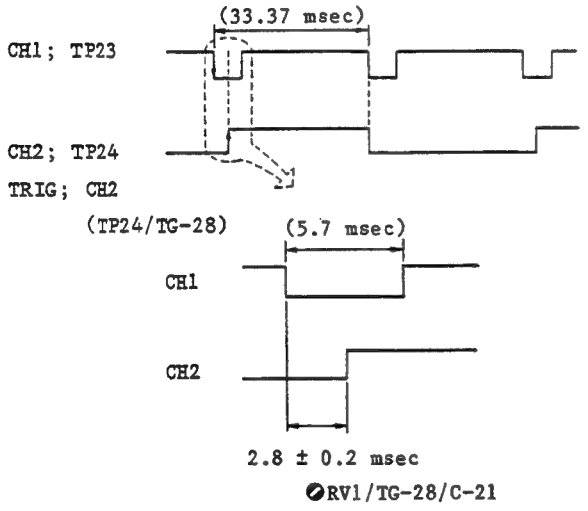


## 7-2. 525/625 DETECTION CIRCUIT ADJUSTMENT

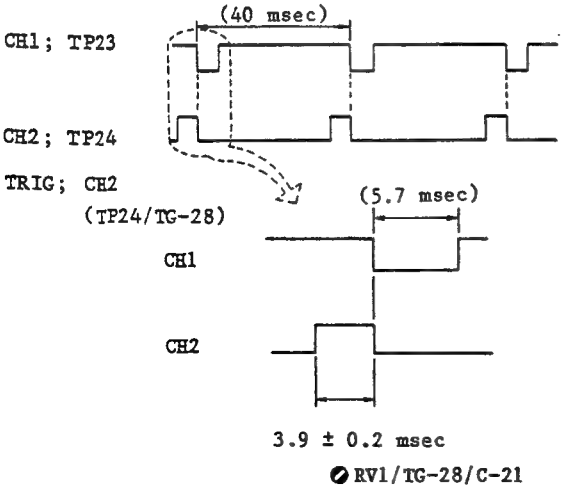
Connection: See connection 1, section 5-4
Equipment: Component video signal generator
Oscilloscope
Mode of DVR/DVPC-1000:
EE
Setting of Switches & Controls:
SERVO REFERENCE/SERVO SETUP SUB MENU:
EXT (ANALOG)
Other settings are same as section 5-5
Input Signal (REFERENCE ANALOG VIDEO):
COMPOSITE SYNC (75 ohms terminate)

**Adjustment: TG-28 Board**

1) For 525/60 system Numbers in parenthesis are reference values.




2) For 625/50 system Numbers in parenthesis are reference values.



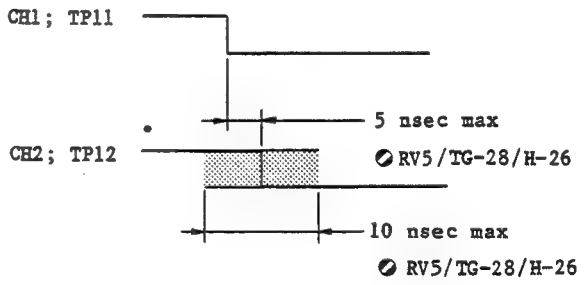

## 7-3. PLL ADJUSTMENT (TG-28 BOARD)

### 7-3-1. No.1 PLL Adjustment

Connection: See connection 3, section 5-4
Equipment: Component video signal generator
Oscilloscope
Mode of DVR/DVPC-1000:
EE
Setting of Switches & Controls:
SERVO REFERENCE/SERVO SETUP SUB MENU:
EXT (ANALOG)
Other settings are same as section 5-5
Input signal (REFERENCE ANALOG VIDEO):
COMPOSITE SYNC (75 ohms terminate)

**Step 1.**
Connect CH-1 of the oscilloscope to TP11/TG-28, and CH-2 to TP12/TG-28. Apply the trigger of the oscilloscope at the falling edge of the CH-1 waveform.

**Step 2. Adjustment: TG-28 Board**
Adjust RV5 so that the jitter of CH-2 is within 10 nsec, and also the center of the jitter at the falling edge of the CH-2 waveform is within 5 nsec with respect to CH-1.



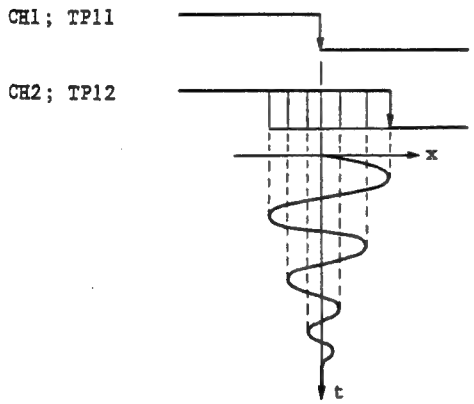
(7-3-1. No.1 PLL Adjustment)

**Step 3. Ringing Adjustment: TG-28 Board**

Turn the power OFF ⟶ ON several times.

Confirm that when the power is switched ON, the falling edge of the CH-2 waveform with respect to the falling edge of CH-1 decays while left-right symmetrical ringing takes place.

If the falling edge does not decay in this way, turn RV5 slightly so that the specification of Step 2 is satisfied, then check the falling edge decay process again.




**7-3-2. No.2 PLL Adjustment**

Connection: See connection 3, section 5-4

Equipment: Component video signal generator
Oscilloscope

Mode of DVR/DVPC-1000:
EE

Setting of Switches & Controls:
SERVO REFERENCE/SERVO SETUP SUB MENU:
EXT (ANALOG)
Other settings are same as section 5-5

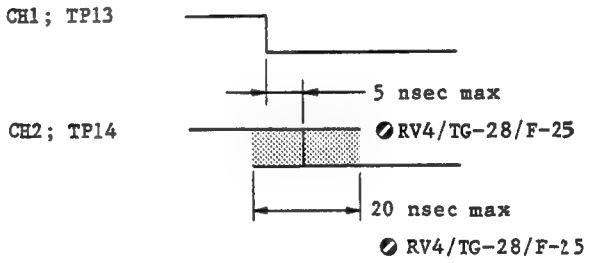
Input signal (REFERENCE ANALOG VIDEO):
COMPOSITE SYNC (75 ohms terminate)

**Step 1.**

Connect CH-1 of the oscilloscope to TP13/TG-28, and CH-2 to TP14/TG-28. Apply the trigger of the oscilloscope to the falling edge of the CH-1 waveform.

**Step 2. Adjustment: TG-28 Board**

Adjust RV4 so that the jitter of CH-2 is within 20 nsec, and also the center of the jitter at the falling edge of the CH-2 waveform is within 5 nsec with respect to CH-1.




**Step 3. Ringing Adjustment: TG-28 Board**

Like Step 3 of 7-3-1, turn the power OFF ⟶ ON several times and check the decay of the falling edge of the CH-2 waveform.

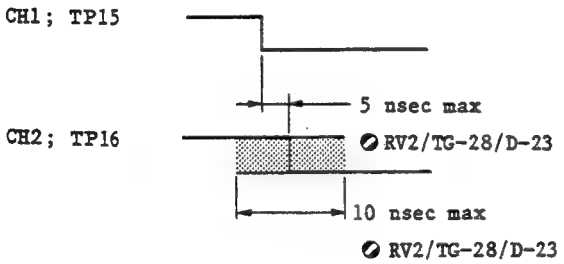
If the decay process is not correct, turn RV4 slightly so that the specification of Step 2 is satisfied, then check it once again.

### 7-3-3. No.3 PLL Adjustment

Connection: See connection 3, section 5-4
Equipment: Component video signal generator
Oscilloscope
Mode of DVR/DVPC-1000:
EE
Setting of Switches & Controls:
SERVO REFERENCE/SERVO SETUP SUB MENU:
EXT (ANALOG)
Other settings are same as section 5-5
Input signal (REFERENCE ANALOG VIDEO):
COMPOSITE SYNC (75 ohms terminate)

**Step 1.**
Connect CH-1 of the oscilloscope to TP15/TG-28, and CH-2 to TP16/TG-28. Apply the trigger of the oscilloscope to the falling edge of the CH-1 waveform.

**Step 2. Adjustment: TG-28 Board**
Adjust RV2 so that the jitter of CH-2 is within 10 nsec, and also the center of the jitter at the falling edge of the CH-2 waveform is within 5 nsec with respect to CH-1.



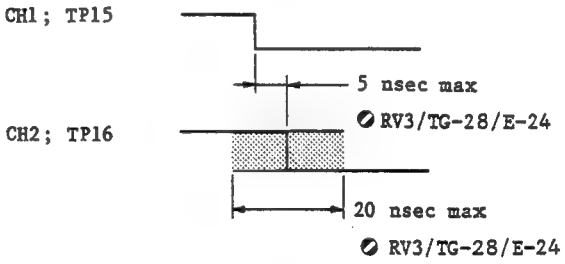

**Step 3. Ringing Adjustment TG-28 Board**
Like Step 3 of 7-3-1, turn the power OFF → ON several times and check the decay of the falling edge of the CH-2 waveform.
If the decay process is not correct, turn RV2 slightly so that the specification of Step 2 is satisfied, then check it once again.

### 7-3-4. No.4 PLL Adjustment

Connection: See connection 3, section 5-4
Equipment: Component video signal generator
Oscilloscope
Mode of DVR/DVPC-1000:
EE
Setting of Switches & Controls:
SERVO REFERENCE/SERVO SETUP SUB MENU:
EXT (ANALOG)
Other settings are same as section 5-5
Input signal (REFERENCE ANALOG VIDEO):
COMPOSITE SYNC (75 ohms terminate)

**Step 1.**
Connect CH-1 of the oscilloscope to TP17/TG-28, and CH-2 to TP18/TG-28. Apply the trigger of the oscilloscope to the falling edge of the CH-1 waveform.

**Step 2. Adjustment: TG-28 Board**
Adjust RV2 so that the jitter of CH-2 is within 20 nsec, and also the center of the jitter at the falling edge of the CH-2 waveform is within 5 nsec with respect to CH-1.




**Step 3. Ringing Adjustment: TG-28 Board**
Like Step 3 of 7-3-1, turn the power OFF → ON several times and check the decay of the falling edge of the CH-2 waveform.
If the decay process is not correct, turn RV3 slightly so that the specification of Step 2 is satisfied, then check it once again.

## 7-4. PLL ADJUSTMENT 2 (SY-70 BOARD)

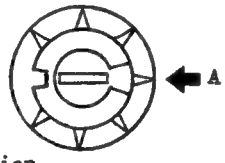
### 7-4-1. Adjustment Preparations

**Step 1. Setting Controls**

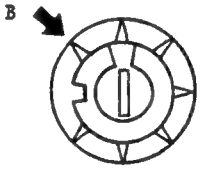
After replacing the following controls, set them to the positions shown in the illustration at right, then start adjustment.

SY-70 Board

RV2, 3, 4, 6: Position A in illustration RV5 and 7 can be set at any position because they are not used.




RV8,9: Position B in illustration
Turn the control fully counterclockwise.




**Step 2.**

Obtain a playback L cassette tape. Use a tape on which is recorded a changing scene, such as a movie.

**Step 3. Setting oscilloscope**

Set the oscilloscope as shown below.

CH-1: 500 mV/DIV, 1 msec/DIV, DC
CH-2: 500 mV/DIV, 1 msec/DIV, DC
TRIG:TP1/SY-70B (ABTOP)

Set the 0 V position for each channel to a point 1 graduation division below the center of the screen.

**Step 4. Setting Control Panel**

(Setting VIDEO STATE/MONITOR menu)

Press the [MON] (MONITOR) button on the control panel. When the display screen changes, press the [F8] (STATE) key. The entire STATE of the VIDEO OUTPUT will change to PB. For details of the method of changing the state, refer to the "DVR-1000 OPERATION MANUAL".

**Step 5.**

Set the switches on the boards as follows.

. IF-139 S3; TEST ON/OFF SW.....ON
. SY-70A S1-1; A/C-CH DATA INH SW.....ON(*1)
S1-2; B/D-CH DATA INH SW.....ON(*1)
. SY-70B S1-1; A/C-CH DATA INH SW.....OFF(*1)
S1-2; B/D-CH DATA INH SW.....OFF(*1)
. FM-09A S1-5; VIDEO OUTER CORRECTION
OFF SW.....ON
. FM-09B S1-5; VIDEO OUTER CORRECTION
OFF SW.....ON
. VN-01 S1-2; CONCEALMENT OFF SW.....ON
. PG-13 S3-2; VIDEO TEST SIGNAL OUTPUT
SW (COLOR BAR).....ON

Check that D1 and D2 on the FM-09A board light up at this time.

*1: This setting is for making adjustments of the SY-70B board.
With this operation, transferring data of slot #16 (C-CH, D-CH) is inhibited. Turn S1-1 and S1-2 ON when making adjustments of the SY-70A board. D1 and D2 on the FM-09B board light up at this time.

**Step 6. Checking the Setting of the Switches**

S1-1/SY-70B: ON
S1-2/SY-70B: ON

With this setting, perform the SHUTTLE playback at a speed other than +1.0 times the normal speed. Verify that the picture is frozen at this time. If it is not, there is a mistake in the setting of the switches. Perform Step 5 again.

**Step 7. Resetting of the Switches**

S1-1/SY-70B: OFF
S1-2/SY-70B: OFF

Set the switches as shown above, as they were in Step 5.

### 7-4-2. Offset Voltage Adjustment

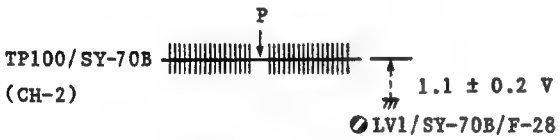
Connection: See connection 1, section 5-4
Equipment: Oscilloscope
Mode of DVR/DVPC-1000:
PLAY
Setting of Switches & Controls:
Refer to Step 5 of Section 7-4-1.
Other settings are same as section 5-5.

**Note:** Set the oscilloscope in the same way as section 7-4-1, Step 3.

**Step 1. A-CH Adjustment**

Connect CH-1 of the oscilloscope to TP103/SY-70B, and CH-2 to TP100/SY-70B.

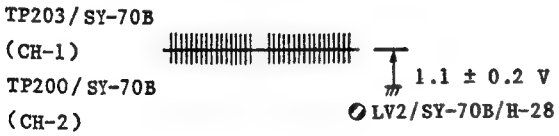
If the preset portion P of the tracking control is not flat and the D.C. voltage is not 1.1 V, slightly turn RV4 (RV6).




Perform adjustment so that waveforms of CH-1 and CH-2 overlap as much as possible.

**Step 2. B-CH Adjustment**

Connect CH-1 of the oscilloscope to TP203/SY-70B, and CH-2 to TP200/SY-70B.



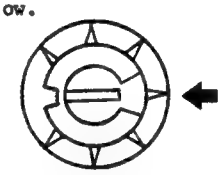

Perform adjustment so that waveforms of CH-1 and CH-2 overlap as much as possible.

### 7-4-3. Clock Balance Adjustment

Connection: See connection 1, section 5-4
Equipment: Oscilloscope
Mode of DVR/DVPC-1000:
PLAY
Setting of Switches & Controls:
Refer to Step 5 of Section 7-4-1.
Other settings are same as section 5-5.

**Step 1. Initial Setting of the Clock Balance**

Set RV4 and RV6 on the SY-70B board as shown in the illustration below.




**Step 2. B-CH Clock Balance Adjustment**

Connect CH-1 of the oscilloscope to TP203/SY-70B, and CH-2 to TP200/SY-70B. The settings of the oscilloscope are the same as those of section 7-4-1, Step 3.

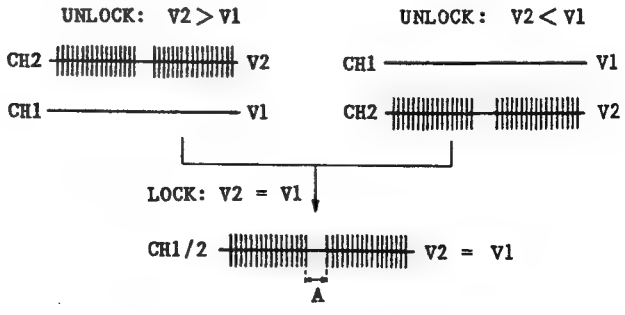
**Step 3. Setting of the Tracking Control**

Pull forward the tracking control on the front of DVR-1000 to the VARIABLE position. Rotate the tracking control so that CH-1 and CH-2 are in the UNLOCK position.

Turn the tracking control so that CH-1 and CH-2 are unlocked (V2 > V1, V2 < V1) as much as possible when RV6 is turned. If one of the channels is not set to UNLOCK state, just go on to the next Step.

**Step 4. Adjustment: SY-70B Board, B-CH**

Adjust RV6 so that CH-1 and CH-2 become locked and the waveform of portion A of CH-2 becomes flat.




Spec.: V2 = V1 RV6/SY-70B/G-32

(7-4-3. Clock Balance Adjustment)

**Step 5. Checking**
Slowly rotate the tracking control of DVR-1000 left and right and confirm that CH-1 and CH-2 remain in a LOCK status. If they go into an UNLOCK status, return to Step 3 and repeat the adjustment procedure.

**Step 6. A-CH Clock Balance Adjustment**
Set CH-1 of the oscilloscope to TP103/SY-70B, and CH-2 to TP100/SY-70B.

**Step 7. Adjustment: SY-70B Board, A-CH**
Place CH-1 and CH-2 in the unlocked status as in Step 3, then adjust RV4/SY-70B so that CH-1 and CH-2 become locked as in Step 4 and the waveform of portion A of CH-2 becomes flat.

**Step 8. Checking**
Slowly turn the tracking control of DVR-1000 left and right, and confirm that CH-1 and CH-2 remain in a LOCK status. If they go into an UNLOCK status, return to Step 7 and repeat the adjustment procedure.

**7-4-4. Clock Phase Adjustment**

Connection: See Connection 1, section 5-4
Equipment: Oscilloscope
Mode of DVR/DVPC-1000: PLAY
Setting of Switchs & Controls:
Refer to Step 3 of Section 7-4-1.
Other Settings are same as Section 5-5.

**Step 1.**
Press the tracking control of DVR-1000 to set it to PRESET.

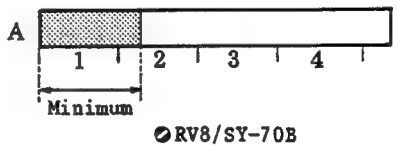
**Step 2. Selection of the RF menu**
Perform the following operations from the control panel.

[TEST], [RF], [F1] (CONTINUE)

When the RF menu is displayed, press the [F11] key twice to set ERRCORR to off.

**Step 3. Adjusting the A-CH on the SY-70B board**
Adjust RV8 on the SY-70B board so that the error rate display (Channel Condition) on the control panel becomes minimum. Check that D1 on the FM-09B board becomes the darkest level at this time.

**Adjustment:** Channel Condition



RV8/SY-70B

**Note:** As it takes a little time before the error rate appears on the display, turn the control slowly.

**Step 4. Adjusting the B-CH on the SY-70B board**
Adjust RV9 on the SY-70B board so that the error rate of B-CH becomes minimum in the same way.

**Step 5.**
Press the [HOME] key to display the HOME menu.

### 7-4-5. SPEED Data Adjustment

Connection: See connection 1, section 5-4
Equipment: Oscilloscope
Mode of DVR/DVPC-1000:
SHUTTLE mode
Setting of Switches & Controls:
Refer to Step 3 of Section 7-4-1.
Other settings are same as Section 5-5.

**Step 1. Setting Oscilloscope**

Connect CH-1 of the oscilloscope to TP1/CI-01, and CH-2 to TP100/SY-70B.

CH-1: 2V/DIV, 1 msec/DIV AC
CH-2: 1V/DIV, 1 msec/DIV DC
TRIG: TP1/SY-70B

**Step 2.**

Set the switches on the SY-70B board as follows.

S1-1/SY-70B A-CH DATA INH SW.....OFF
S1-2/SY-70B B-CH DATA INH SW.....ON

**Step 3.**

Use the playback tape obtained in section 7-4-1, and play it at a speed of -40 times normal speed. After the DC level stabilizes, perform the following adjustment.

**Step 4. CH-A SPEED Data Adjustment**

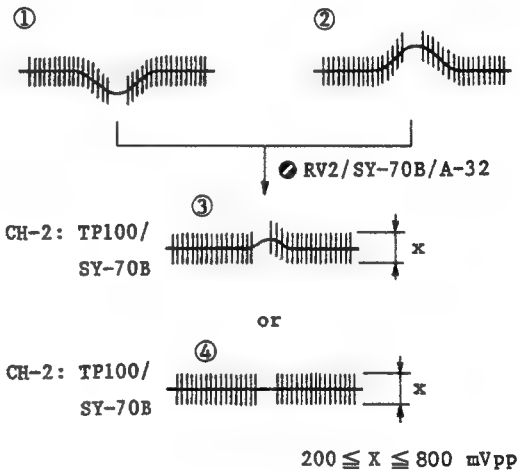
CH-1: TP1/CI-01


Adjust ⊘RV2/SY-70B/AU-32 so that the "L" portion is as large as possible and also the DC level of the waveform maximum. At this time, the picture reproduced on the monitor will vary by the maximum extent. If adjustment is not correct, data write to the frame memory will not take place, but instead the same data will be read repetitively. As a result, the same screen (mozaic pattern) will remain displayed on the monitor, just as in the FREEZE mode.

**Step 5.**

Check the waveform on CH-2 of the oscilloscope. If the waveform shown in ③ or ④ of the illustration below is not obtained, adjust ⊘ RV2/SY-70B/A-32.

**Note:** Ideally, the waveform of ④ should be obtained. If, however, the specification at Step 4 is not satisfied, priority must be given to satisfying the specification of Step 4 in which case waveform ③ at Step 5 is acceptable.




**Step 6.**

Press the F1 (OUTPUT) key on the DVR-1000 control panel. While this key is pressed, the EE picture will be output, and when the F1 key is released, the playback picture will be output.

Press the F1 key ON/OFF repetitively, and confirm that the output playback picture changes.

If the playback picture does not change, repeat adjustment from Step 4.

If it is quite impossible to satisfy all specification, maximum priority must be given to the change of the playback picture by the F1 key ON/OFF in which case the adjustment criteria of Steps 4 and 5 may be degraded slightly.

(7-4-5. Speed Data Adjustment)

**Step 7.**

Play back the tape at a speed of +40 times normal speed.

Press key [F1] ON/OFF and confirm that the playback picture changes. If it does not change, repeat adjustment from Step 3.

**Step 8.**

Confirm that the waveform of CH-2 (TP100/SY-70B) when the tape is played back at a speed of +40 times normal speed is ③ or ④ of Step 5. If it does not meet the specification adjust ⊘RV2/SY-70B/A-32. After adjustment, set the playback speed to -40 times normal speed, and recheck Step 5. If it is quite impossible to satisfy all standards, give priority to the specification which is applicable to a playback speed of -40 times normal speed.

**Step 9. Final Checking of SHUTTLE ⟷ E/E**

Check the changes of the played back images by turning the [F1] key on and off at speeds of ±40, ±32, and ±16 times the normal speed. If the played back image is completely frozen at a certain speed, change the setting of the DIP switches and repeat the adjustments from step 6.

S1-6/SY-70B SPEED INF. CONTROL SW.....OFF

With this operation, the speed information is sent when no data is received in High Speed Shuttle mode (±24 times the normal speed or faster).

**Step 10.**

Play back the tape at speed other than +1.0 times the normal speed in Shuttle mode. Verify that the picture is frozen when the DIP switch is set as follows.

S1-1/SY-70B A-CH DATA INH SW..... ON

S1-2/SY-70B B-CH DATA INH SW..... ON

If it is not, there is a mistake in the setting of the switches. Verify the switch of 7-4-1 Step 5 and repeat the beginning 7-4-5 Speed Data Adjustment.

(7-4-5. Speed Data Adjustment)

**Step 11. B-CH SPEED Data Adjustment**

Set DIP switch S1 on the front of SY-70B board as follows.

S1-1/SY-70B A-CH DATA INH SW..... ON

S1-2/SY-70B B-CH DATA INH SW..... OFF

S1-6/SY-70B SPEED INF. CONTROL SW.... ON

**Step 12.**

Connect CH1 of the oscilloscope with TP2/CI-01 and CH2 with TP200/SY-70B.

**Step 13. CH-B SPEED Data Adjustment**

Change the setting of the adjustment control from RV2/SY-70B to RV3/SY-70B and make adjustments from Step 3.

### 7-4-6. PLL Checking of STANDBY OFF → PLAY

**Step 1.**
Set all the DIP switches (S1) on the SY-70B board to off.

**Step 2.**
Play back the tape.

**Step 3.**
Pull the tracking volume control toward you to set to VARIABLE, and then set it to the position where the picture is frozen.

**Step 4.**
Set the oscilloscope as follows.
CH1: TP100/SY-70B, 500 mV/DIV
CH2: TP200/SY-70B, 500 mV/DIV

**Step 5.**
Set TTP to STANDBY OFF.

**Step 6.**
Verify that PLL is not set to UNLOCK state (7-4-3. Step 4) when the PLAY key is pressed in STANDBY OFF mode.

**Step 7.**
Perform the above-mentioned STANDBY OFF → PLAY test (Step 5 and 6) 10 times. If PLL is set to UNLOCK state, repeat the adjustments from Section 7-4-3, "Clock Balance Adjustment."
(Only the channel which is set to UNLOCK state)
When PLL is set to UNLOCK state even after the readjustment, press the tracking volume control to preset it and perform the STANDBY OFF → PLAY test 20 times.
If PLL is set to UNLOCK state even once in this test,

① Check the modification.
If the modification is done correctly,

② Then check the error voltage of TP100 (or TP200).
(X in Step 5 of Section 7-4-5)
When X < 300 mVpp:
(The band of the oscilloscope should not be restricted.)
Perform the following steps 1) or 2) for the channel which is still set to UNLOCK state and repeat the adjustments from Section 7-4-3.

1) Replace MC5400 of ICE31 (A/C CH) and ICG31 (B/D CH). (MC5400: 8-749-900-72)
2) Add an approx. 10k (5-15kohm) resistor between PIN1 and PIN3 of MC5400 so that X = approx. 400 mVpp.

### 7-4-7. SY-70A Board Adjustment

**Step 1.**

After completing adjustment of the SY-70B board, set the switches as follows.

. SY-70B S1-1; A/C-CH DATA INH SW..... ON
S1-2; B/D-CH DATA INH SW..... ON

. SY-70A S1-1; A/C-CH DATA INH SW..... OFF
S1-2; B/D-CH DATA INH SW..... OFF

Verify that D1 and D2 of FM-09B light up at this time. With this operation, transferring data of slot #17 (A-CH, B-CH) is inhibited.

**Step 2.**

Make adjustments in Steps 5 to 7 of Section 7-4-1 and in Sections 7-4-2 to 7-4-6 similarly to the SY-70B board.

At this time, read over again as follows.

| | | |
|---|---|---|
| SY-70B | ⟶ | SY-70A |
| CH-A | ⟶ | CH-C |
| CH-B | ⟶ | CH-D |
| TP1/CI-01 | ⟶ | TP3/CI-01 |
| TP2/CI-01 | ⟶ | TP4/CI-01 |

Connect the TRIG terminal of the oscilloscope with TP1/SY-70A (AB Top).

### 7-4-8. Resetting Switches and Jumpers

**Step 1. Setting control panel**

Return the system from the VIDEO STATE which was activated in Step 4 of section 7-1-1, to the initial state.

**Step 2. Resetting Switches**

| | |
|---|---|
| S3/IF-139 | ; OFF (TEST SW) |
| S1/SY-70A/B | ; ALL OFF |
| S1/VN-01 | ; ALL OFF |
| S3/PG-13 | ; ALL OFF |
| S1-3,5/FM-09A/B | ; ON |

(Those other than S1-3 and 5 FM-09 are all off.)

Verify that the LED TEST MODE green lamp on the front panel of the DVPC-1000 lights up.

## 7-5. PLL ADJUSTMENT 3 (IE-17 BOARD)

Connection: See connection 1, section 5-4
Equipment: Digital voltmeter
Frequency counter,
Oscilloscope
Mode of DVR/DVPC-1000:
STOP
Setting of Switches & Controls:
Same as section 5-5

**Step 1.**

Short circuit pins 5 and 7 of IC-B25 on the IE-17 board using jumper wire.

**Step 2. VCO Input Voltage Setting**

TP9/IE-17 = -6.20 ± 0.05 Vdc
◐RV1/IE-17/A-26

**Step 3. REC CLOCK Frequency Adjustment**

TP8/IE-17 = 9.8 ± 1.0 MHz
◐L11/IE-17/B-28

**Step 4.**

Remove the jumper wire installed in Step 1.

**Step 5. REC CLOCK Adjustment**

Using the oscilloscope, observe the waveforms at TP7 and TP8 of the IE-17 board.

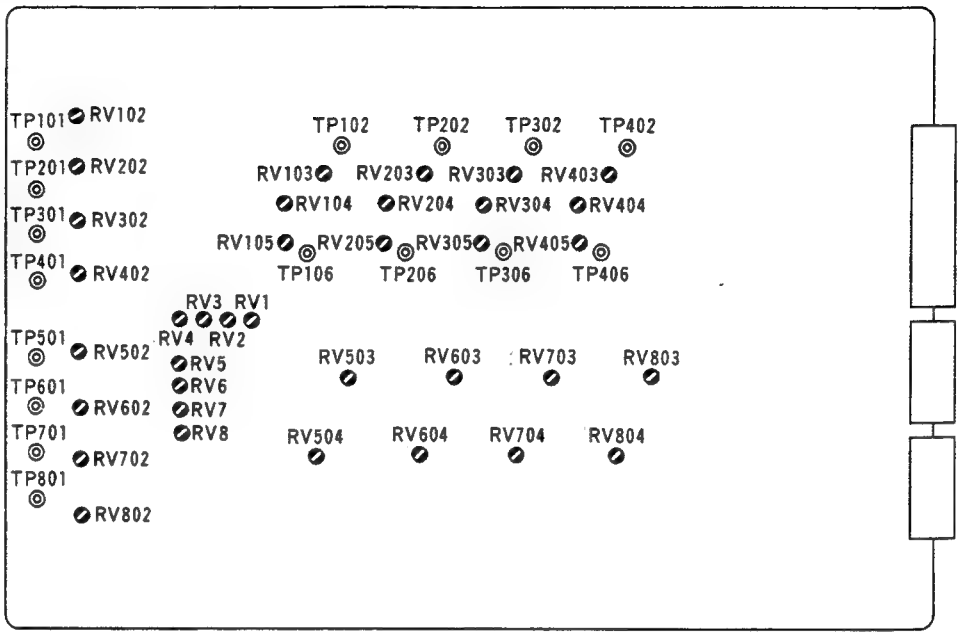
Adjust ◐RV1/IE-17/A-26 so that the signal at TP8 locks onto the signal at TP7, and also jitter becomes minimum.

At this time, confirm that the voltage at TP8/IE-17 is within the following range.

$-6.3\ \text{Vdc} \leqq \text{TP9/IE-17} \leqq -5.7\ \text{Vdc}$

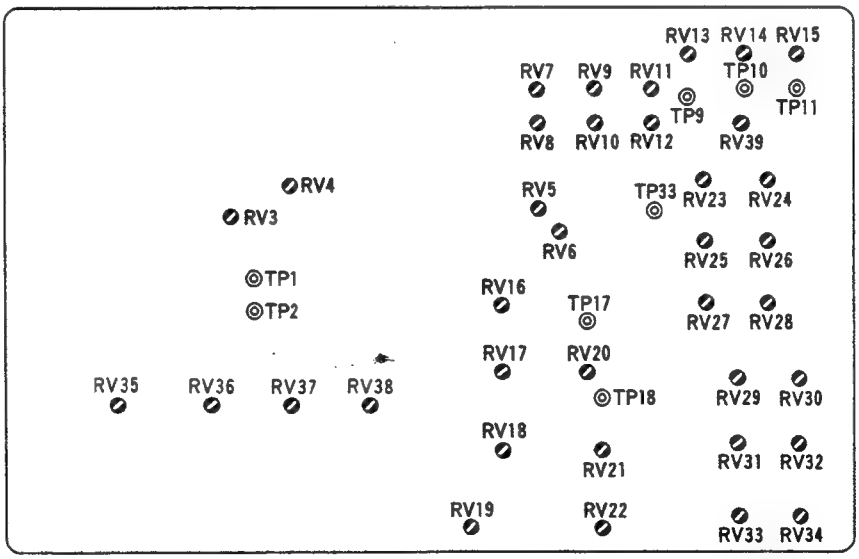
# SECTION 8
# ANALOG AUDIO SIGNAL SYSTEM ALIGNMENT

**AA-29 board (component side)**



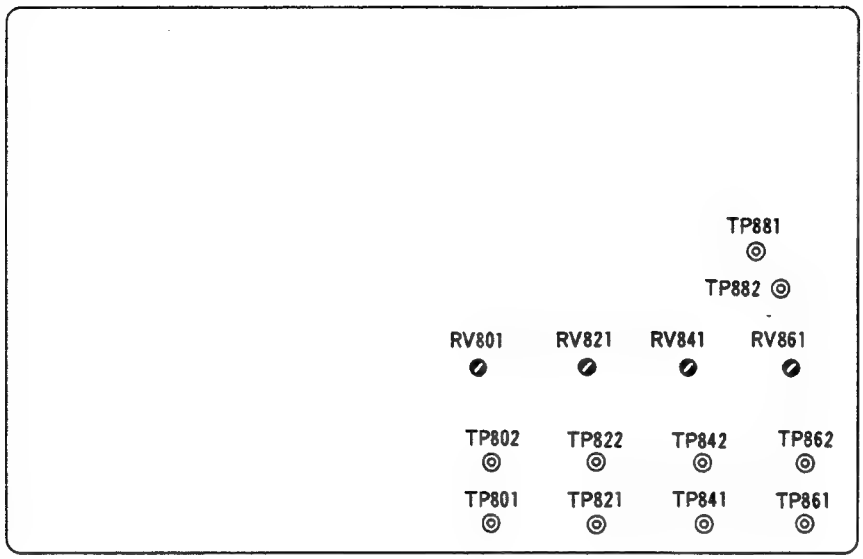

**IV-14 board (component side)**

| Serial No: Up to 20999 (UC) |
|---|
| Serial No: Up to 11199 (EK) |

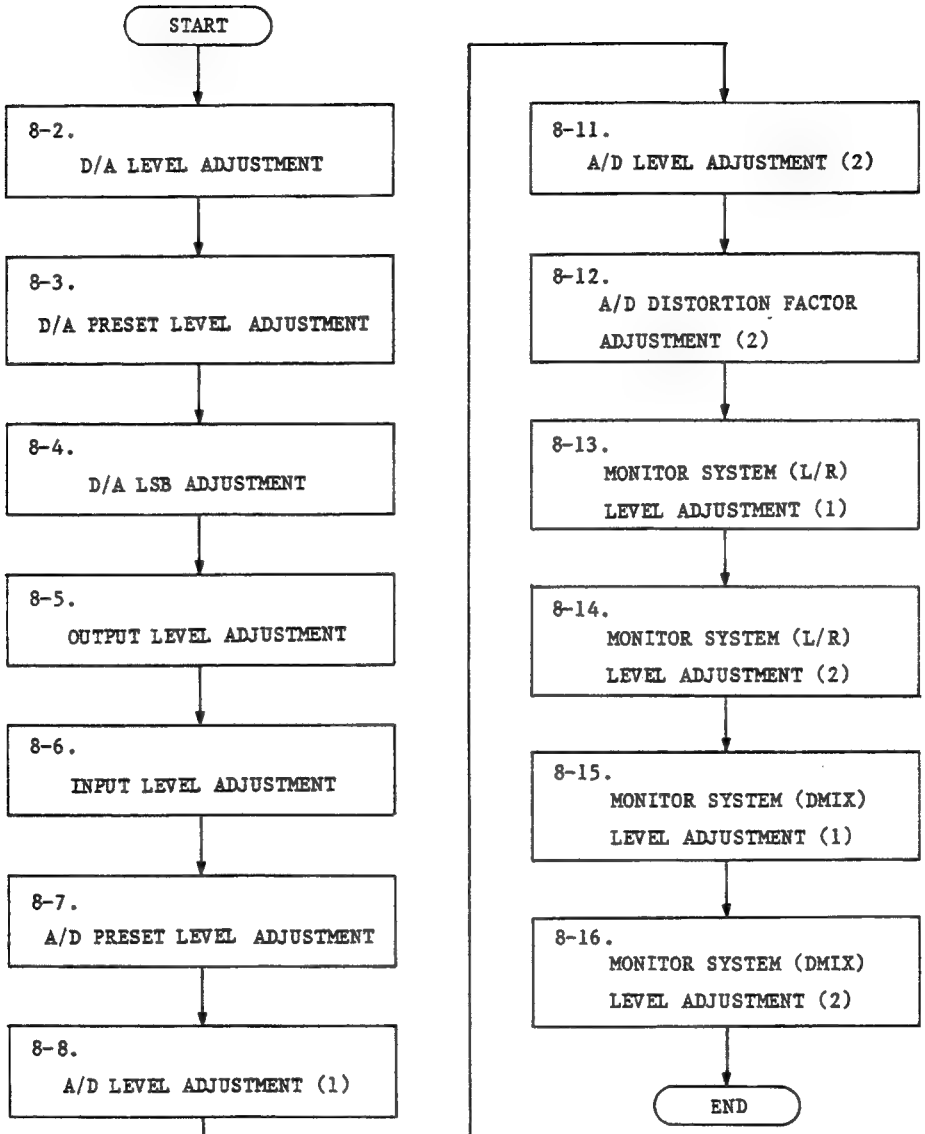


IV-21 board (component side)

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)



## 8-1. ALIGNMENT SEQUENCE




Note: When the DVPC-1000 is connected with the DVR-1000, set the audio emphasis of all audio channels to the OFF position before aligning the audio signal system. The emphasis ON/OFF switch can be set by the DIGITAL AUDIO RECORDING SETUP sub menu. When the DVR-1000 is not connected, the emphasis ON/OFF switch is automatically set to the OFF position.

## 8-2. D/A LEVEL ADJUSTMENT

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(Input impedance 100 kΩ, 80 kHz LPF
ON, level measurement)
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
TEST SW (S3/IF-139); ON
AUDIO TEST SIGNAL SELECT SW
(S1/PG-13); 0
AUDIO TEST SIGNAL OUTPUT SW
(S3-4/PG-13); ON
ANALOG AUDIO OUTPUT LEVEL PRE/VAR SW
(S501, 601, 701, 801/AA-29); VAR
(lower side)
ANALOG AUDIO OUTPUT LEVEL CONT.
(RV501, 502, 503, 504/AA-29);
fully clockwise
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
Free

**Adjustment AA-29 board**

CH-1; TP501/AA-29 = +6.0 ± 0.1 dBs
⊘RV504/AA-29
CH-2; TP601/AA-29 = +6.0 ± 0.1 dBs
⊘RV604/AA-29
CH-3; TP701/AA-29 = +6.0 ± 0.1 dBs
⊘RV704/AA-29
CH-4; TP801/AA-29 = +6.0 ± 0.1 dBs
⊘RV804/AA-29

## 8-3. D/A PRESET LEVEL ADJUSTMENT

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(Input impedance 100 kΩ, 80 kHz LPF
ON, level measurement)
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
TEST SW (S3/IF-139); ON
AUDIO TEST SIGNAL SELECT SW
(S1/PG-13); 0
AUDIO TEST SIGNAL OUTPUT SW
(S3-4/PG-13); ON
ANALOG AUDIO OUTPUT LEVEL PRE/VAR SW
(S501, 601, 701, 801/AA-29); PRE
(upper side)
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
Free

**Adjustment AA-29 board**

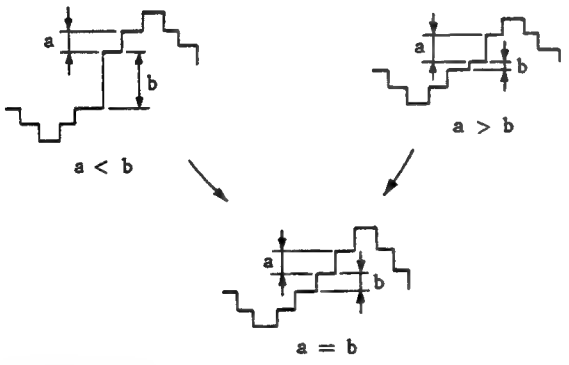
CH-1; TP501/AA-29 = -6.0 ± 0.1 dBs
⊘RV502/AA-29
CH-2; TP601/AA-29 = -6.0 ± 0.1 dBs
⊘RV602/AA-29
CH-3; TP701/AA-29 = -6.0 ± 0.1 dBs
⊘RV702/AA-29
CH-4; TP801/AA-29 = -6.0 ± 0.1 dBs
⊘RV802/AA-29

## 8-4. D/A LSB ADJUSTMENT

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(Input impedance 100 kΩ, 80 kHz LPF ON, level measurement)
Oscilloscope
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
TEST SW (S3/IF-139); ON
AUDIO TEST SIGNAL SELECT SW (S1/PG-13); 7
AUDIO TEST SIGNAL OUTPUT SW (S3-4/PG-13); ON
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
Free

**Adjustment AA-29 board**

Connect the audio distortion meter to TP501 on the AA-29 board. Adjust RV503 on the AA-29 board so that a = b as observed on an oscilloscope connected to the input monitor of the audio distortion meter. Adjust CH-2 (TP601, RV603), CH-3 (TP701, RV703), and CH-4 (TP801, RV803) in the same manner.




INPUT MONITOR
CH-1; TP501/AA-29 CH-1; ⊘RV503/AA-29
CH-2; TP601/AA-29 CH-2; ⊘RV603/AA-29
CH-3; TP701/AA-29 CH-3; ⊘RV703/AA-29
CH-4; TP801/AA-29 CH-4; ⊘RV803/AA-29

## 8-5. OUTPUT LEVEL ADJUSTMENT

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(600Ω termination, 80 kHz LPF ON, level measurement)
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
TEST SW (S3/IF-139); ON
AUDIO TEST SIGNAL SELECT SW (S1/PG-13); 0
AUDIO TEST SIGNAL OUTPUT SW (S3-4/PG-13); ON
ANALOG AUDIO OUTPUT LEVEL PRE/VAR SW (S501, 601, 701, 801/AA-29); PRE (upper side)
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
Free

**Adjustment AT-45 board**

CH-1; ANALOG AUDIO OUT = +8.0 ± 0.1 dBm /CONNECTOR PNL. ⊘RV101/AT-45
CH-2; ANALOG AUDIO OUT = +8.0 ± 0.1 dBm /CONNECTOR PNL. ⊘RV201/AT-45
CH-3; ANALOG AUDIO OUT = +8.0 ± 0.1 dBm /CONNECTOR PNL. ⊘RV301/AT-45
CH-4; ANALOG AUDIO OUT = +8.0 ± 0.1 dBm /CONNECTOR PNL. ⊘RV401/AT-45

## 8-6. INPUT LEVEL ADJUSTMENT

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(Input impedance 100 k , 80 kHz LPF
ON, level measurement)
Audio oscillator
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
ANALOG AUDIO INPUT LEVEL PRE/VAR SW
(S101, 201, 301, 401/AA-29); VAR
(lower side)
A/D PRESET LEVEL CONT.
(RV101, 201, 301, 401/AA-29);
fully clockwise
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
1 kHz/+8 dBm

**Adjustment AA-29 board**

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

CH-1; TP101/AA-29 = +6.0 ± 0.1 dBs
⊘RV38/IV-14
CH-2; TP201/AA-29 = +6.0 ± 0.1 dBs
⊘RV37/IV-14
CH-3; TP301/AA-29 = +6.0 ± 0.1 dBs
⊘RV36/IV-14
CH-4; TP401/AA-29 = +6.0 ± 0.1 dBs
⊘RV35/IV-14

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

CH-1; TP101/AA-29 = +6.0 ± 0.1 dBs
⊘RV801/IV-21
CH-2; TP201/AA-29 = +6.0 ± 0.1 dBs
⊘RV821/IV-21
CH-3; TP301/AA-29 = +6.0 ± 0.1 dBs
⊘RV841/IV-21
CH-4; TP401/AA-29 = +6.0 ± 0.1 dBs
⊘RV861/IV-21

## 8-7. A/D PRESET LEVEL ADJUSTMENT

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(Input impedance 100 kΩ, 80 kHz LPF
ON, level measurement)
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
ANALOG AUDIO OUTPUT LEVEL PRE/VAR SW
(S501, 601, 701, 801/AA-29); PRESET
(upper side)
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
1 kHz/+8 dBm

**Adjustment AA-29 board**

CH-1; TP101/AA-29 = -6.0 ± 0.1 dBs
⊘RV102/AA-29
CH-2; TP201/AA-29 = -6.0 ± 0.1 dBs
⊘RV202/AA-29
CH-3; TP301/AA-29 = -6.0 ± 0.1 dBs
⊘RV302/AA-29
CH-4; TP401/AA-29 = -6.0 ± 0.1 dBs
⊘RV402/AA-29

## 8-8. A/D LEVEL ADJUSTMENT (1)

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(Input impedance 100 kΩ, 80 kHz LPF ON, level measurement)
Audio oscillator
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
ANALOG AUDIO INPUT LEVEL PRE/VAR SW (S101, 201, 301, 401/AA-29); PRESET (upper side)
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
1 kHz/+8 dBm

**Adjustment AA-29 board**

CH-1; TP102/AA-29 = -6.8 ± 0.1 dBs
⊘RV103/AA-29
CH-2; TP202/AA-29 = -6.8 ± 0.1 dBs
⊘RV203/AA-29
CH-3; TP302/AA-29 = -6.8 ± 0.1 dBs
⊘RV303/AA-29
CH-4; TP402/AA-29 = -6.8 ± 0.1 dBs
⊘RV403/AA-29

## 8-9. A/D DISTORTION FACTOR ADJUSTMENT (1)

Connection; See connection 2, section 5-4.
Equipment; Oscilloscope or Digital voltmeter
Mode of DVR/DVPC-1000;
Free
Setting of Switches & Controls;
Same as section 5-5
Input Signal (ANALOG AUDIO IN);
Free

**Adjustment AA-29 board**

CH-1; TP106(PIN8/IC109) = -1.7 ± 0.1 V
⊘RV105/AA-29
CH-2; TP206(PIN8/IC209) = -1.7 ± 0.1 V
⊘RV205/AA-29
CH-3; TP306(PIN8/IC309) = -1.7 ± 0.1 V
⊘RV305/AA-29
CH-4; TP406(PIN8/IC409) = -1.7 ± 0.1 V
⊘RV405/AA-29

## 8-10. A/D OFFSET ADJUSTMENT

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
Audio oscillator
Oscilloscope
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
ANALOG AUDIO INPUT LEVEL PRE/VAR SW
(S101, 201, 301, 401/AA-29); PRE
(upper side)
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
1 kHz/+28 dBm

**Step 1.**
Connect jumper plugs as shown below.

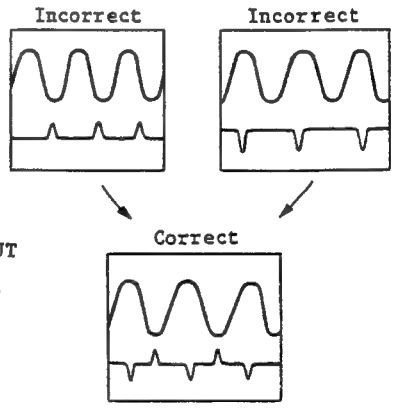
**AA-29 board** (Part No. 1-620-925-11)

CH-1; JP101 → JP102
CH-2; JP201 → JP202
CH-3; JP301 → JP302
CH-4; JP401 → JP402

**AA-29 board** (Part No. 1-620-925-12)

CN111 → CN112
CN211 → CN212
CN311 → CN312
CN411 → CN412

**Step 2. Adjustment**
Adjust RV104, RV204, RV304, and RV404 so that the distorted waveform becomes symmetric with respect to the X-axis as shown in the figure below by observing the analog output with an audio distortion meter.




ANALOG AUDIO OUT
/CONNECTOR PNL.
CH-1
CH-2
CH-3
CH-4

CH-1; ⊘RV104/AA-29
CH-2; ⊘RV204/AA-29
CH-3; ⊘RV304/AA-29
CH-4; ⊘RV404/AA-29

**Step 3.**
Put the jumper plug back in its original position.

## 8-11. A/D LEVEL ADJUSTMENT (2)

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(600Ω termination, 80 kHz LPF ON,
level measurement)
Audio oscillator
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
ANALOG AUDIO INPUT LEVEL PRE/VAR SW
(S101, 201, 301, 401/AA-29); PRE
(upper side)
ANALOG AUDIO OUTPUT LEVEL PRE/VAR SW
(S501, 601, 701, 801/AA-29); PRE
(upper side)
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
1 kHz/+8 dBm

**Adjustment AA-29 board**

CH-1; ANALOG AUDIO OUT = +8.0 ± 0.1 dBm
/CONNECTOR PNL. ⊘RV103
CH-2; ANALOG AUDIO OUT = +8.0 ± 0.1 dBm
/CONNECTOR PNL. ⊘RV203
CH-3; ANALOG AUDIO OUT = +8.0 ± 0.1 dBm
/CONNECTOR PNL. ⊘RV303
CH-4; ANALOG AUDIO OUT = +8.0 ± 0.1 dBm
/CONNECTOR PNL. ⊘RV403

## 8-12. A/D DISTORTION FACTOR ADJUSTMENT (2)

Connection; See connection 2, section 5-4.
Equipment; Audio distortion factor meter
(600Ω termination, 80 kHz LPF ON,
distortion factor measurement)
Audio oscillator
Oscilloscope
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
ANALOG AUDIO INPUT LEVEL PRE/VAR SW
(S101, 201, 301, 401/AA-29); PRE
(upper side)
ANALOG AUDIO OUTPUT LEVEL PRE/VAR SW
(S501, 601, 701, 801/AA-29); PRE
(upper side)
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
1 kHz/+8 dBm, +27.5 dBm

**Step 1. Adjustment AA-29 board**

Input 1 kHz/+27.5 dBm signals into the ANALOG AUDIO IN with an audio oscillator, and adjust RV105, RV205, RV305, and RV405 so that the distortion factor at the ANALOG AUDIO OUTPUT is less than 0.015%.

ANALOG AUDIO OUT; Distortion factor:
/CONNECTOR PNL. less than 0.015%
CH-1; ⊘RV105
CH-2; ⊘RV205
CH-3; ⊘RV305
CH-4; ⊘RV405

**Step 2. Adjustment AA-29 board**

Input 1 kHz/+8.0 dBm signals into the ANALOG AUDIO IN with an audio oscillator, and adjust RV105, RV205, RV305, and RV405 so that the distortion factor at the ANALOG AUDIO OUTPUT is less than 0.05%.

ANALOG AUDIO OUT; Distortion factor:
/CONNECTOR PNL. less than 0.05%
CH-1; ⊘RV105
CH-2; ⊘RV205
CH-3; ⊘RV305
CH-4; ⊘RV405

If it does not meet the specification, repeat step 1 and step 2.

## 8-13. MONITOR SYSTEM (L/R) LEVEL ADJUSTMENT (1)

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(Input impedance 100 kΩ, 80 kHz LPF ON, level measurement)
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
TEST SW (S3/IF-139); ON
UPI TEST JUMPER (JP1/PG-13); SHORT
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
1 kHz/+8 dBm

**Adjustment AA-29 board**

Select the monitor output with the combination of the S3-6, S2-1, and S2-2 ON/OFF switches on the PG-13 board as shown in the table below, and adjust RV1, RV2, RV3, RV4, RV5, RV6, RV7, and RV8 so that the TP1 level on the AA-29 board is -10 dBs.

| S3-6 | S2-1 | S2-2 | Monitor output signal | Adjusting point | Specification |
|---|---|---|---|---|---|
| ON | ON | ON | CH-1 Input signal | RV1 | TP1 = -10 ± 0.1 dBs |
| | | OFF | CH-2 Input signal | RV2 | |
| | OFF | ON | CH-3 Input signal | RV3 | |
| | | OFF | CH-4 Input signal | RV4 | |
| OFF | ON | ON | CH-1 output signal | RV5 | |
| | | OFF | CH-2 output signal | RV6 | |
| | OFF | ON | CH-3 output signal | RV7 | |
| | | OFF | CH-4 output signal | RV8 | |

**Note:** The selected signals are common to L/R.

## 8-14. MONITOR SYSTEM (L/R) LEVEL ADJUSTMENT (2)

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(600Ω termination, 80 kHz LPF ON,
level measurement)
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
TEST SW (S3/IF-139); ON
UPI TEST JUMPER (JP1/PG-13); SHORT
BYPASS INPUT CHECK SW (S3-6/PG-13); ON
AUDIO MONITOR SELECT 1 SW
(S2-1/PG-13); ON
AUDIO MONITOR SELECT 2 SW
(S2-2/PG-13); ON
For other setting same as section 5-5.
Input Signal (ANALOG AUDIO IN);
1 kHz/+8 dBm

**Adjustment AT-45 board**

L-CH output TP502-TP503
(balanced output) = -20.0 ± 0.1 dBm
⊘RV501/AT-45
R-CH output TP602-TP603
(balanced output) = -20.0 ± 0.1 dBm
⊘RV601/AT-45

## 8-15. MONITOR SYSTEM (DMIX) LEVEL ADJUSTMENT (1)

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(Input impedance 100 kΩ, 80 kHz LPF
ON, level measurement)
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
TEST SW (S3/IF-139); ON
AUDIO TEST SIGNAL SELECT SW
(S1/PG-13); 0
AUDIO TEST SIGNAL OUTPUT SW
(S3-4/PG-13); ON
Input Signal (ANALOG AUDIO IN);
Free

**Adjustment PG-13 board**

TP13/PG-13 = -10.0 ± 0.1 dBs
⊘RV2/PG-13/G-4

## 8-16. MONITOR SYSTEM (DMIX) LEVEL ADJUSTMENT (2)

Connection; See connection 2, section 5-4.
Equipment; Audio distortion meter
(600Ω termination, 80 kHz LPF ON,
level measurement)
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
TEST SW (S3/IF-139); ON
AUDIO TEST SIGNAL SELECT SW
(S1/PG-13); 0
AUDIO TEST SIGNAL SELECT SW
(S3-4/PG-13); ON
Input Signal (ANALOG AUDIO IN);
Free

**Adjustment AT-45 board**

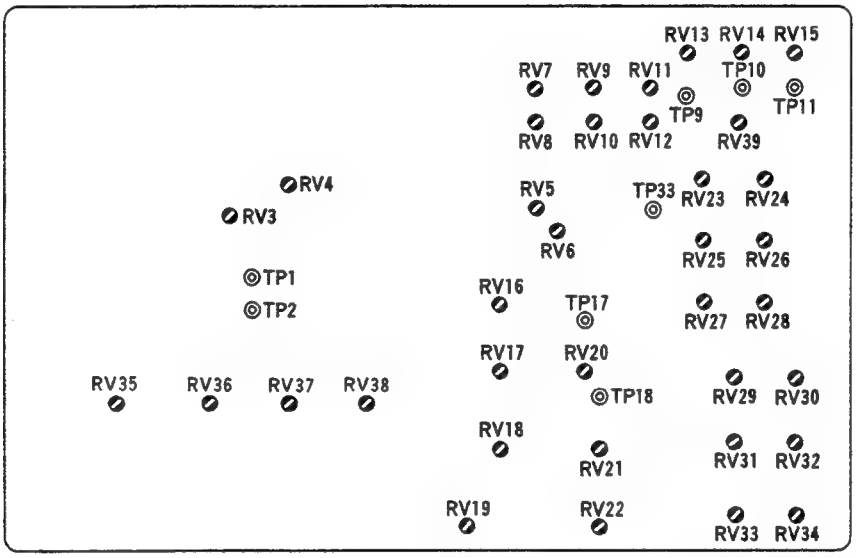
DMIX output TP702-TP703
(balanced output) = -20.0 ± 0.1 dBm
⊘RV701/AT-45

# SECTION 9
# ANALOG VIDEO SIGNAL SYSTEM ALIGNMENT

For users who have a unit (IV-14 board mounted) with Serial No. 20999 (UC), or lower, or Serial No. 11199 (EK), or lower, make adjustments shown on pages 9-1 to 9-17.
For users who have a unit (IV-20/21 board mounted) with Serial No. 20101 (UC), or higher, or Serial No. 11201 (EK), or higher, make adjustments shown on pages 9-18 to 9-35.

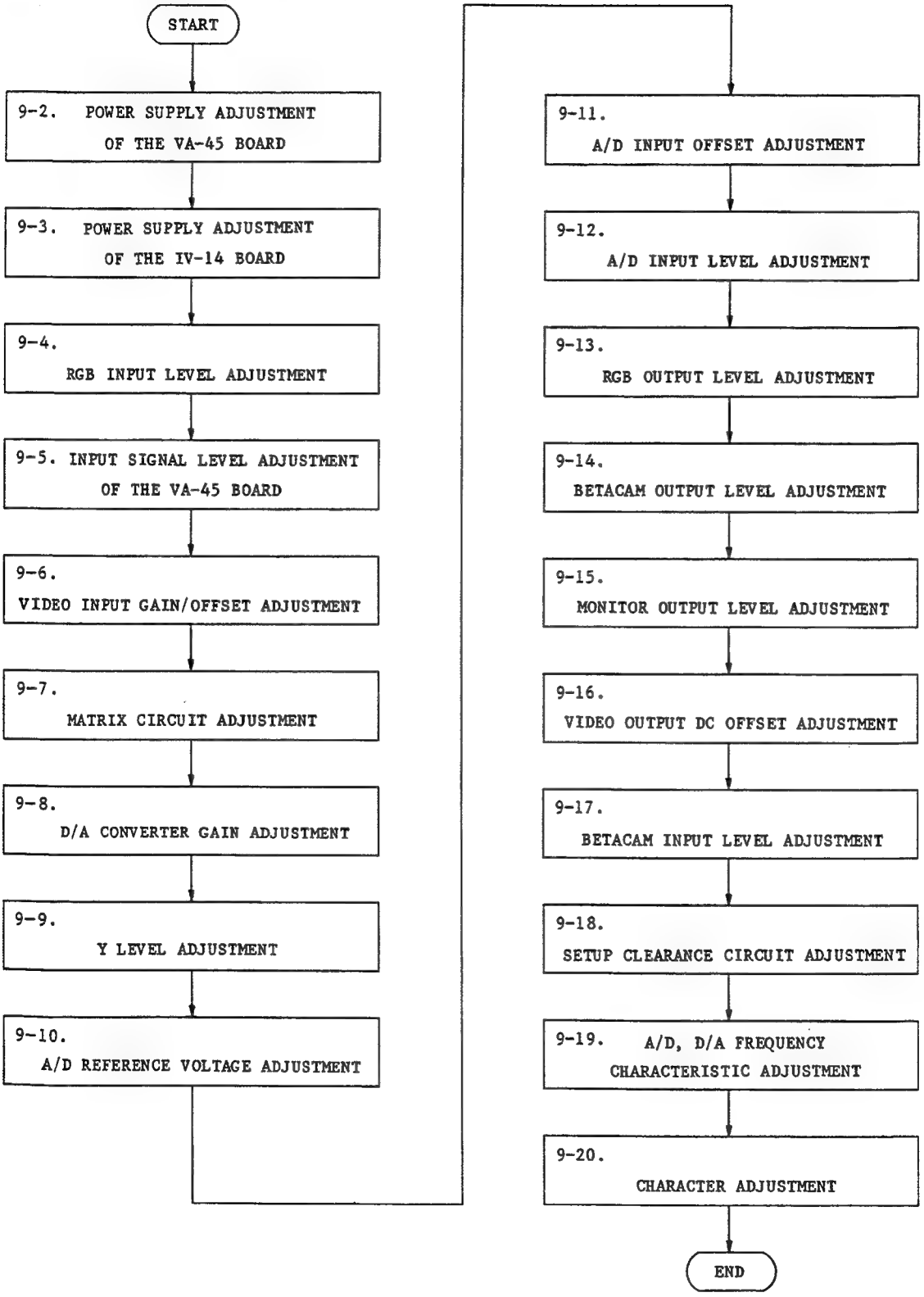
Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

**IV-14 board (component side)**



Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

## 9-1. ALIGNMENT SEQUENCE



Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

## 9-2. POWER SUPPLY ADJUSTMENT OF THE VA-45 BOARD

Equipment; Digital voltmeter
Setting of Switches & Controls;
Same as section 5-5.

Note: When any of the following controls is replaced, set the control to the following position before adjusting it.
VA-45 board
RV801, 831, 861 ..... Fully counterclockwise
RV802, 832, 862 ..... Mechanical center position

**Step 1. +12 V voltage adjustment**
TP801/VA-45 = +12.00 ± 0.05 Vdc
●RV802/VA-45/A-2

**Step 2. +12 V over-current protective circuit adjustment**
Slowly turn RV801/VA-45 clockwise while observing a voltmeter connected across TP801/VA-45. When the output voltage starts to change, turn RV801 counterclockwise by 1 scale division.

**Step 3. -12 V voltage adjustment**
TP802/VA-45 = -12.00 ± 0.05 Vdc
●RV832/VA-45/A-6

**Step 4. -12 V over-current protective circuit adjustment**
Slowly turn RV831/VA-45 clockwise while observing a voltmeter connected across TP802/VA-45. When the output voltage starts to change, turn RV831 counterclockwise by 1 scale division.

**Step 5. -5 V voltage adjustment**
TP803/VA-45 = -5.00 ± 0.05 Vdc
●RV862/VA-45/A-8

**Step 6. -5 V over-current protective circuit adjustment**
Slowly turn RV861/VA-45 clockwise while observing a voltmeter connected across TP803/VA-45. When the output voltage starts to change, turn RV861 counterclockwise by 1 scale division.

## 9-3. POWER SUPPLY ADJUSTMENT OF THE IV-14 BOARD

Equipment; Digital voltmeter
Setting of Switches & Controls;
Same as section 5-5.

Note: When any of the following controls is replaced, set the control to the following position before adjusting it.
IV-14 board
RV1, 2, 3, 4 ..... Mechanical center position

**Step 1. +12 V voltage adjustment**
TP1/IV-14 = +12.00 ± 0.05 Vdc
●RV3/IV-14

**Step 2. +12 V over-current protective circuit adjustment**
Slowly turn RV1/IV-14 clockwise while observing a voltmeter connected across TP1/IV-14. When the output voltage starts to change, turn RV1 counterclockwise by 1 scale division.

**Step 3. -12 V voltage adjustment**
TP2/IV-14 = -12.00 ± 0.05 Vdc
●RV4/IV-14

**Step 4. -12 V over-current protective circuit adjustment**
Slowly turn RV2/IV-14 clockwise while observing a voltmeter connected across TP2/IV-14. When the output voltage starts to change, turn RV2 counterclockwise by 1 scale division.

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

## 9-4. RGB INPUT LEVEL ADJUSTMENT

Connection; See Connection 3, Section 5-4.

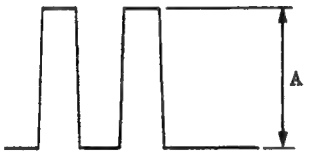
Equipment; Oscilloscope
Component signal generator

Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU : ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): RGB
BYPASS6 SW (S3-1/PG-13): ON
For other setting same as section 5-5

Input Signal (ANALOG VIDEO INPUT 1):
100% COLOR BARS (RGB) ↔ No signal

**Step 1. R gain adjustment**
Input color bars signal.

TP32/IV-14

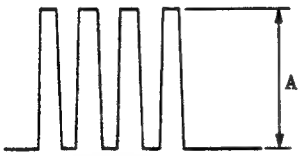



A = 700 ± 10 mVp-p
⊘RV27/IV-14

**Step 2. R offset adjustment**
Remove signal from the input.
TP32/IV-14 = 400 ± 20 mVdc
⊘RV28/IV-14

**Step 3. B gain adjustment**
Input color bars signal.

TP18/IV-14

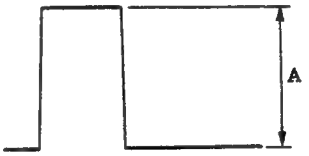



A = 700 ± 10 mVp-p
⊘RV25/IV-14

**Step 4. B offset adjustment**
Remove signal from the input.
TP18/IV-14 = 400 ± 20 mVdc
⊘RV26/IV-14

**Step 5. G gain adjustment**
Input color bars signal.

TP17/IV-14




A = 700 ± 10 mVp-p
⊘RV23/IV-14

**Step 6. G offset adjustment**
Remove signal from the input.
TP17/IV-14 = 400 ± 20 mVdc
⊘RV24/IV-14

**Step 7. SYNC offset adjustment**
Adjust with no signal input.
TP33/IV-14 = 0 ± 20 mVdc
⊘RV39/IV-14

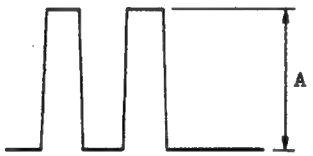
Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

## 9-5. INPUT SIGNAL LEVEL ADJUSTMENT OF THE VA-45 BOARD

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Component signal generator
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU: ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): RGB
BYPASS6 SW (S3-1/PG-13): ON
For other setting same as section 5-5
Input Signal (ANALOG VIDEO INPUT 1):
100% COLOR BARS (RGB)

**Step 1. R level adjustment**

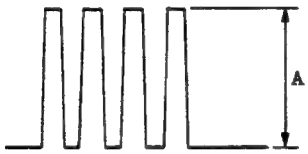
TP101/VA-45




A = 700 ± 10 mVp-p
⊘RV22/IV-14

**Step 2. B level adjustment**

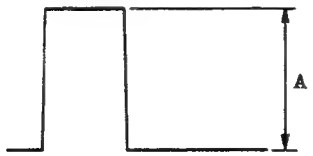
TP201/VA-45




A = 700 ± 10 mVp-p
⊘RV21/IV-14

**Step 3. G level adjustment**

TP301/VA-45




A = 700 ± 10 mVp-p
⊘RV20/IV-14

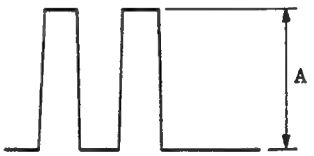
## 9-6. VIDEO INPUT GAIN/OFFSET ADJUSTMENT

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Component video signal generator
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU: ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): RGB
ANALOG VIDEO INPUT SW (S101/VA-45): PRESET
TEST SW (S3/IF-139): ON
For other setting same as section 5-5
Input Signal (ANALOG VIDEO INPUT 1):
100% COLOR BARS (RGB) ↔ No signal

**Step 1. R(R-Y) gain adjustment**

Input color bars signal.

TP102/VA-45




A = 1400 ± 20 mVp-p
⊘RV102/VA-45/A-1

**Step 2. R(R-Y) offset adjustment**

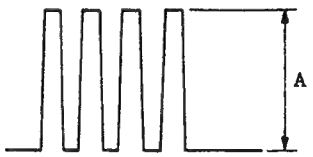
Remove signal from the input.

TP102/VA-45 = 0 ± 40 mVdc
⊘RV101/VA-45/A-1

**Step 3. B(B-Y) gain adjustment**

Input color bars signal.

TP202/VA-45




A = 1400 ± 20 mVp-p
⊘RV202/VA-45/A-1

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

(9-6. VIDEO INPUT GAIN/OFFSET ADJUSTMENT)

**Step 4. B(B-Y) offset adjustment**

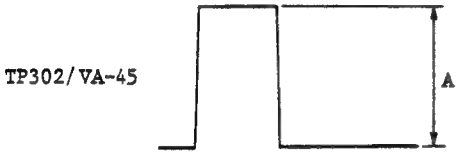
Remove signal from the input.

TP202/VA-45 = 0 ± 40 mVdc

⊘ RV201/VA-45/A-1

**Step 5. G(Y) gain adjustment**

Input color bars signal.




A = 1400 ± 20 mVp-p

⊘RV302/VA-45/B-1

**Step 6. G(Y) offset adjustment**

Remove signal from the input.

TP302/VA-45 = 0 ± 40 mVdc

⊘RV301/VA-45/B-1

**9-7. MATRIX CIRCUIT ADJUSTMENT**

Connection; See Connection 3, Section 5-4.

Equipment; Oscilloscope

Component video signal generator

(GBR output)

Mode of DVR/DVPC-1000;

EE

Setting of Switches & Controls;

ANALOG VIDEO INPUT SW

(S101/VA-45): PRESET

PROCESSOR CONT. MODE/SYSTEM SETUP SUB

MENU: ON

VIDEO SELECT RGB/Y, R-Y, B-Y SW

(S4/PG-13): RGB

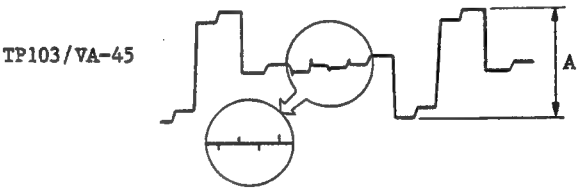
TEST SW (S3/IF-139): ON

For other setting same as section 5-5

Input Signal (ANALOG VIDEO INPUT 1):

100% COLOR BARS (RGB)

**Step 1. R-Y matrix adjustment**



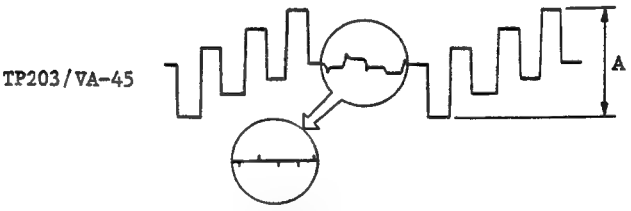

Minimize the difference in level.

⊘RV104/VA-45/A-1

A = 1400 ± 20 mVp-p

⊘RV105/VA-45/A-1

**Step 2. B-Y matrix adjustment**




Minimize the difference in level.

⊘RV204/VA-45/A-1

A = 1400 ± 20 mVp-p

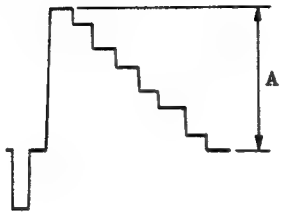
⊘RV205/VA-45/A-1

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

(9-7. MATRIX CIRCUIT ADJUSTMENT)

**Step 3. Y matrix adjustment**

TP303/VA-45



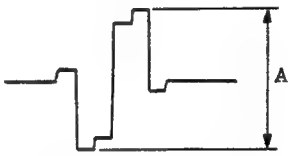

A = 1400 ± 20 mVp-p
⊘RV305/VA-45/B-1

## 9-8. D/A CONVERTER GAIN ADJUSTMENT

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
VIDEO TEST SIGNAL OUTPUT SW
(S3-2/PG-13): ON
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
TEST SIGNAL SELECT SW
(S1-1/VA-45): OFF
For other setting same as section 5-5

**Step 1. R-Y level adjustment**

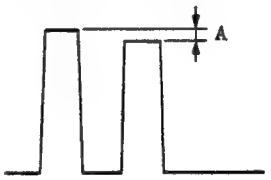
TP403/VA-45




A = 710 ± 10 mVp-p
⊘RV401/VA-45/C-1

**Step 2. R dematrix adjustment**

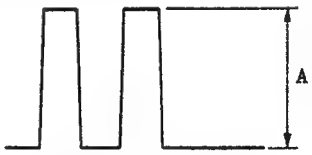
TP402/VA-45




A = Minimum
⊘RV601/VA-45/G-1

**Step 3. R level adjustment**

TP402/VA-45



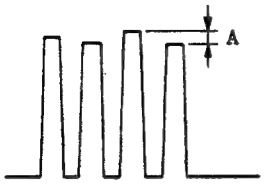

A = 710 ± 10 mVp-p
⊘RV404/VA-45/E-1

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

(9-8. D/A CONVERTER GAIN ADJUSTMENT)

**Step 4. B dematrix adjustment**

TP502/VA-45

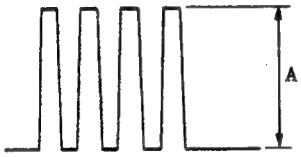



A = Minimum

⊘RV501/VA-45/E-1

**Step 5. B level adjustment**

TP502/VA-45

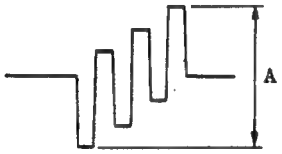



A = 710 ± 10 mVp-p

⊘RV504/VA-45/F-1

**Step 6. B-Y level check**

TP503/VA-45

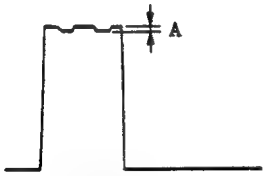



A = 710 ± 10 mVp-p

If it does not meet the specification, repeat adjustments from step 1.

**Step 7. G dematrix adjustment**

TP602/VA-45

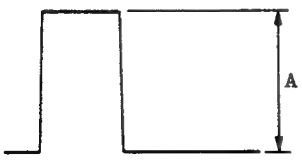



A = Minimum

⊘RV604/VA-45/G-1

**Step 8. G level adjustment**

TP602/VA-45




A = 710 ± 10 mVp-p

⊘RV605/VA-45/H-1

**9-9. Y LEVEL ADJUSTMENT**

Connection; See Connection 3, Section 5-4.

Equipment; Oscilloscope

Setting of Switches & Controls;

TEST SW (S3/IF-139): ON

BYPASS6 SW (S3-1/PG-13): ON

VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13): ON

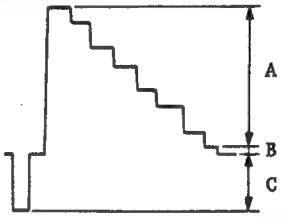
ANALOG VIDEO OUTPUT SW (S701/VA-45): PRESET

TEST SIGNAL SELECT SW (S1-1/VA-45): OFF

For other setting same as section 5-5

**Step 1. BETACAM OUT Y level adjustment (525/60 system)**

TP603/VA-45




A = 660 ± 10 mV ⊘RV606/VA-45/H-1

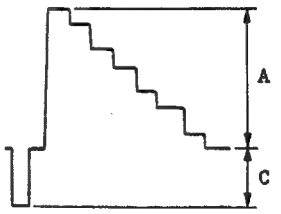
B = 54 ± 7 mV ⊘RV703/VA-45/E-1

C = 286 ± 5 mV ⊘RV705/VA-45/E-1

**Note:** When adjust the VA-45 board with board number 1-620-781-11, observe at edge connector B12c on the VA-45 board. Adjust the portion of C by RV702.

**Step 2. BETACAM OUT Y level adjustment (625/50 system)**

TP603/VA-45




Check; A = 700 ± 10 mV

Adjust; C = 300 ± 5 mV ⊘RV702/VA-45/E-1

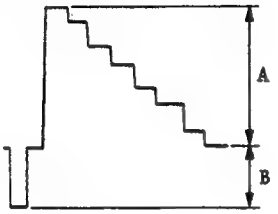
**Note:** When adjust the VA-45 board with board number 1-620-781-11, observe at edge connector B12c on the VA-45 board.

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

(9-9. Y LEVEL ADJUSTMENT)

**Step 3. Y level adjustment/check**

TP604/VA-45




Check: A = 710 ± 10 mV
Adjustment: B = 304 ± 5 mV ●RV704/VA-45/E-1

**Note:** When adjust the VA-45 board with board number 1-620-781-11, observe at TP603 on the VA-45 board.

If it does not meet the specification, repeat adjustment of section 9-7 "D/A converter gain adjustment."

**9-10. A/D REFERENCE VOLTAGE ADJUSTMENT**

Equipment; Digital voltmeter
Setting of Switches & Controls;
Same as section 5-5

**Step 1. R-Y A/D reference voltage adjustment**
TP105/VA-45 = -2.00 ± 0.01 Vdc
●RV109/VA-45/A-1

**Step 2. B-Y A/D reference voltage adjustment**
TP205/VA-45 = -2.00 ± 0.01 Vdc
●RV209/VA-45/A-1

**Step 3. Y A/D reference voltage adjustment**
TP305/VA-45 = -2.00 ± 0.01 Vdc
●RV309/VA-45/B-1

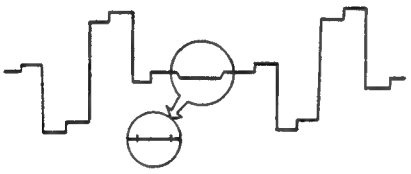
Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

## 9-11. A/D INPUT OFFSET ADJUSTMENT

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Component signal generator
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
For other setting same as section 5-5
Input signal (ANALOG VIDEO INPUT 1):
100% COLOR BARS (Y, R-Y, B-Y)

**Step 1. R-Y offset adjustment**

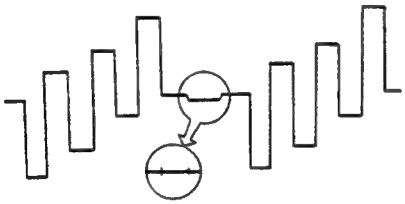
TP401/VA-45



Minimize the difference in level.
● RV108/VA-45/A-1

**Step 2. B-Y offset adjustment**

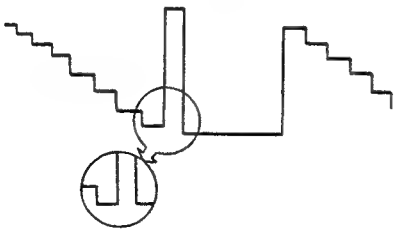
TP501/VA-45



Minimize the difference in level.
● RV208/VA-45/A-1

**Step 3. Y offset adjustment**

TP601/VA-45



Minimize the difference in level.
● RV308/VA-45/B-1

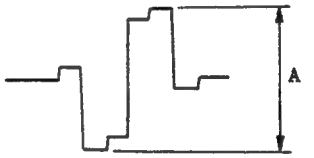
## 9-12. A/D INPUT LEVEL ADJUSTMENT

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Component signal generator
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
TEST SIGNAL SELECT SW
(S1-1/VA-45): OFF
For other setting same as section 5-5
Input Signal (ANALOG VIDEO INPUT 1):
100% COLOR BARS

**Step 1. R-Y input level adjustment**

Adjust RV107 by changing the position of VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13) so that the level with S3-2 = OFF is equal to the level with S3-2 = ON.

TP401/VA-45

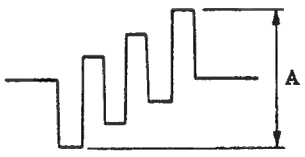



Spec.; The level (A) with S3-2/PG-13 = OFF is equal to the level with S3-2/PG-13 = ON.
● RV107/VA-45/A-1

**Step 2. B-Y input level adjustment**

Adjust RV207 by changing the position of VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13) so that the level with S3-2 = OFF is equal to the level with S3-2 = ON.

TP501/VA-45




Spec.: The level (A) with S3-2/PG-13 = OFF is equal to the level with S3-2/PG-13 = ON.
● RV207/VA-45/A-1

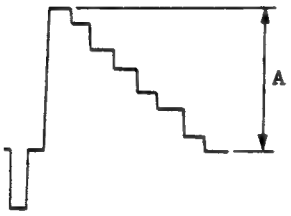
Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

(9-12. A/D INPUT LEVEL ADJUSTMENT)

**Step 3. Y input level adjustment**

Adjust RV307 by changing the position of VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13) so that the level with S3-2 = OFF is equal to the level with S3-2 = ON.

TP601/VA-45



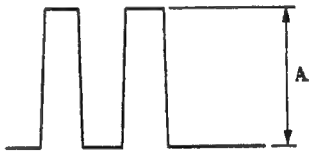

Spec.: The level (A) with S3-2/PG-13 = OFF is equal to the level with S3-2/PG-13 = ON.
● RV307/VA-45/C-1

## 9-13. RGB OUTPUT LEVEL ADJUSTMENT

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13): ON
VIDEO OUTPUT RGB/Y, R-Y, B-Y SW (S3-5/PG-13): OFF (RGB)
TEST SIGNAL SELECT SW (S1-1/VA-45): OFF
ANALOG VIDEO OUTPUT SW (S701/VA-45): PRESET
For other setting same as section 5-5

**Step 1. R output level adjustment**

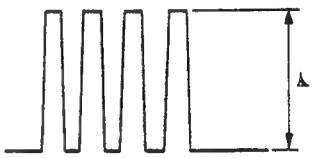
ANALOG VIDEO OUTPUT 1
R1(R-Y1)/CN PNL.
R2(R-Y2)/CN PNL.




A = 700 ± 10 mVp-p
R2(Right side): ●RV7/IV-14
R1(Left side): ●RV8/IV-14

**Step 2. B output level adjustment**

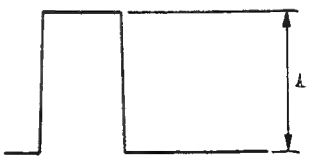
ANALOG VIDEO OUTPUT 1
R1(B-Y1)/CN PNL.
R2(B-Y2)/CN PNL.




A = 700 ± 10 mVp-p
B2(Right side): ●RV9/IV-14
B1(Left side): ●RV10/IV-14

**Step 3. G output level adjustment**

ANALOG VIDEO OUTPUT 1
G1(Y1)/CN PNL.
G2(Y2)/CN PNL.




A = 700 ± 10 mVp-p
G2(Right side): ●RV11/IV-14
G1(Left side): ●RV12/IV-14

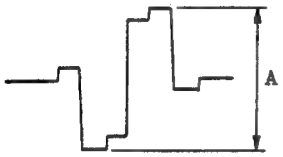
Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

## 9-14. BETACAM OUTPUT LEVEL ADJUSTMENT

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
VIDEO TEST SIGNAL OUTPUT SW
(S3-2/PG-13): ON
TEST SIGNAL SELECT SW
(S1-1/VA-45): OFF
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
For other setting same as section 5-5

**Step 1. R-Y output level adjustment**

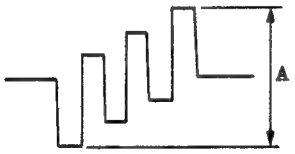
TP9/IV-14




A = 1870 ± 20 mVp-p
⊘RV13/IV-14

**Step 2. B-Y output level adjustment**

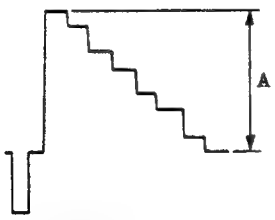
TP10/IV-14




A = 1870 ± 20 mVp-p
⊘RV14/IV-14

**Step 3. Y output level adjustment**

TP11/IV-14



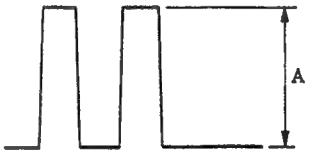

A = 1400 ± 20 mVp-p
⊘RV15/IV-14

## 9-15. MONITOR OUTPUT LEVEL ADJUSTMENT

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
VIDEO TEST SIGNAL OUTPUT SW
(S3-2/PG-13): ON
TEST SIGNAL SELECT SW
(S1-1/VA-45): OFF
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
WFM SIGNAL SELECT/MON MENU/
DVR-1000 CONT. PNL.: VIDEO (RED)
For other setting same as section 5-5

**Step 1. MONITOR OUT R level adjustment**

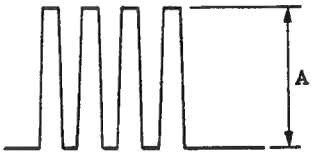
PICTURE MONITOR OUTPUT
R/CN PNL.




A = 700 ± 10 mVp-p
⊘RV18/IV-14

**Step 2. MONITOR OUT B level adjustment**

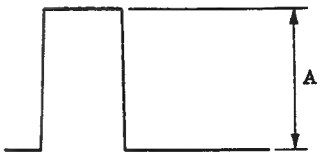
PICTURE MONITOR OUTPUT
B/CN PNL.




A = 700 ± 10 mVp-p
⊘RV17/IV-14

**Step 3. MONITOR OUT G level adjustment**

PICTURE MONITOR OUTPUT
G/CN PNL.



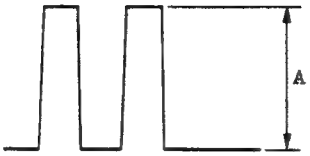

A = 700 ± 10 mVp-p
⊘RV16/IV-14

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

(9-15. MONITOR OUTPUT LEVEL ADJUSTMENT)

**Step 4. WFM output level adjustment**

WFM OUTPUT/CN PNL.



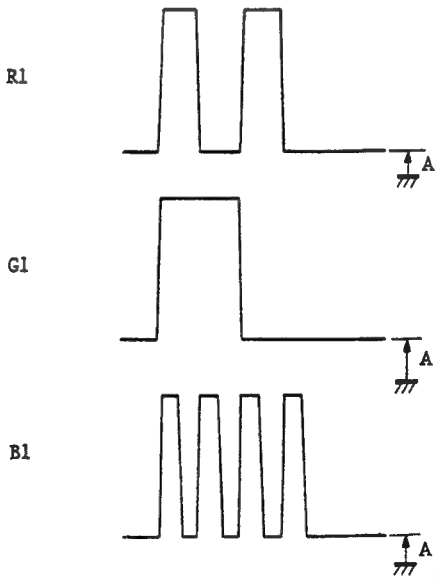

A = 700 ± 10 mVp-p
●RV19/IV-14

## 9-16. VIDEO OUTPUT DC OFFSET ADJUSTMENT

Connection; See Connection 3, Section 5-4.
Equipment; Waveform monitor
Component video signal generator
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU : ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): RGB
BYPASS6 SW (S3-1/PG-13): ON
VIDEO OUTPUT RGB/Y, R-Y, B-Y SW (S3-5/PG-13): OFF (RGB)
ANALOG VIDEO INPUT SW (S101/VA-45): PRESET
ANALOG VIDEO OUTPUT SW (S701/VA-45): PRESET
For other setting same as section 5-5
Input Signal (ANALOG VIDEO INPUT 1):
100% COLOR BARS (RGB)

**Adjustment IV-14 board**

Measure the DC offset voltage of each R/G/B channel at ANALOG VIDEO OUTPUT 1 (R1, G1, B1).




When the difference of offset voltage among three channels is 50 mV or more, mount the following resistors, which is selected according to the difference of voltage, to the channel with the lowest offset voltage.

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

(9-16. VIDEO OUTPUT DC OFFSET ADJUSTMENT)

**Mount position**

In case R1-CH is lower ...
Between pin 1 and pin 3 of IC23
In case B1-CH is lower ...
Between pin 1 and pin 3 of IC28
In case G1-CH is lower ...
Between pin 1 and pin 3 of IC33

**Mount resistor**

| Voltage difference(mV) | Mount resistor | SONY part number |
|---|---|---|
| 15 - 25 | 24 k , METAL, 1/6W | 1-215-454-00 |
| 26 - 40 | 15 k , METAL, 1/6W | 1-215-449-00 |
| 41 - 60 | 10 k , METAL, 1/6W | 1-215-445-00 |
| 61 - 85 | 6.8 k , METAL, 1/6W | 1-215-441-00 |
| 86 - 120 | 5.1 k , METAL, 1/6W | 1-215-438-00 |

Measure the difference of offset voltage between channels at ANALOG VIDEO OUTPUT 1 (R2, G2, B2) and PICTURE MONITOR OUTPUT (R, G, B) in a similar manner, then mount a resistor to the channel with the lower voltage.

**Mount position**

ANALOG VIDEO OUTPUT 1
In case R2-CH is lower ...
Between pin 1 and pin 3 of IC22
In case B2-CH is lower ...
Between pin 1 and pin 3 of IC27
In case G2-CH is lower ...
Between pin 1 and pin 3 of IC32
PICTURE MONITOR OUTPUT
In case R-CH is lower ...
Between pin 1 and pin 3 of IC54
In case B-CH is lower ...
Between pin 1 and pin 3 of IC50
In case G-CH is lower ...
Between pin 1 and pin 3 of IC46

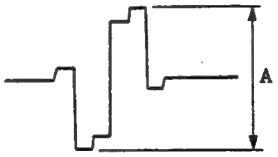
**9-17. BETACAM INPUT LEVEL ADJUSTMENT**

Connection; See Connection 3, Section 5-4.
(Connect the ANALOG VIDEO INPUT-2 connector and the ANALOG VIDEO OUTPUT-2 connector with a cable.)
Equipment; Oscilloscope
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
ANALOG VIDEO INPUT SW (S101/VA-45): PRESET
ANALOG VIDEO OUTPUT SW (S701/VA-45): PRESET
TEST SIGNAL SELECT SW (S1-1/VA-45): OFF
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU : ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): Y, R-Y, B-Y
VIDEO SELECT BNC/MULTI SW (S5/PG-13): MULTI
BYPASS6 SW (S3-1/PG-13): ON
For other setting same as section 5-5
Input Signal (ANALOG VIDEO INPUT 2);
The signal of ANALOG VIDEO OUTPUT-2 connector output (Y, R-Y, B-Y: color bars) is used as an input signal.

**Step 1. R-Y gain adjustment**

Input color bars signal.

TP32/IV-14




A = 700 ± 10 mVp-p
●RV33/IV-14

**Step 2. R-Y offset adjustment**

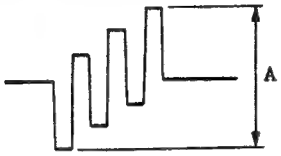
Remove signal from the input.
TP32/IV-14 = 400 ± 20 mVdc
●RV34/IV-14

(9-17. BETACAM INPUT LEVEL ADJUSTMENT)

**Step 3. B-Y gain adjustment**

Input color bars signal.

TP18/IV-14




A = 700 ± 10 mVp-p

●RV31/IV-14

**Step 4. B-Y offset adjustment**

Remove signal from the input.

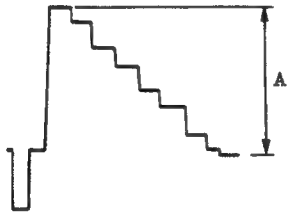
TP18/IV-14 = 400 ± 20 mVdc

●RV32/IV-14

**Step 5. Y gain adjustment**

Input color bars signal.

TP17/IV-14




A = 700 ± 10 mVp-p

●RV29/IV-14

**Step 6. Y offset adjustment**

Remove signal from the input.

TP17/IV-14 = 400 ± 20 mVdc

●RV30/IV-14

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

**9-18. SETUP CLEARANCE CIRCUIT ADJUSTMENT**
**(in case of 525/60 line standard only)**

Connection; See Connection 3, Section 5-4.
(Connect the ANALOG VIDEO INPUT-2 connector and the ANALOG VIDEO OUTPUT-2 connector with a cable.)

Equipment; Oscilloscope
Component signal generator

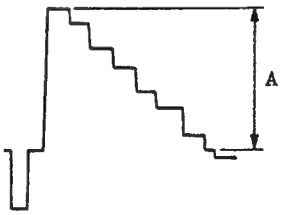
Mode of DVR/DVPC-1000;
EE

Setting of Switches & Controls;
ANALOG VIDEO INPUT SW
(S101/VA-45): PRESET
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
VIDEO TEST SIGNAL OUTPUT SW
(S3-2/PG-13): ON
TEST SIGNAL SELECT SW
(S1-1/VA-45): OFF
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU : ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW
(S4/PG-13): Y, R-Y, B-Y
VIDEO SELECT BNC/MULTI SW
(S5/PG-13): MULTI
TEST SW (S3/IF-139): ON
SYSTEM SELECT SW (S2/IF-139): 525
For other setting same as section 5-5

Input Signal (ANALOG VIDEO INPUT 2);
The signal of ANALOG VIDEO OUTPUT-2 connector output (Y, R-Y, B-Y: color bars) is used as an input signal.

**VA-45 board adjustment**

TP302




A = 1400 ± 20 mVp-p

●RV303/VA-45/A-1

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

## 9-19. A/D, D/A FREQUENCY CHARACTERISTIC ADJUSTMENT

Connection; See Connection 3, Section 5-4.

Equipment; Oscilloscope
Component video signal generator

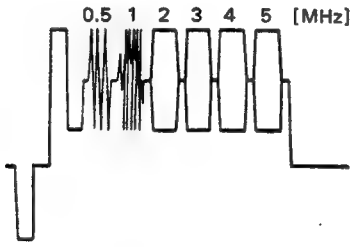
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU : ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): Y, R-Y, B-Y
VIDEO SELECT BNC/MULTI SW (S5/PG-13): BNC
BYPASS6 SW (S3-1/PG-13): ON
VIDEO OUTPUT RGB/Y, R-Y, B-Y SW (S3-5/PG-13): ON (Y, R-Y, B-Y)
TEST SIGNAL SELECT SW (S1-1/VA-45): ON
For other setting same as section 5-5

Input Signal (ANALOG VIDEO INPUT 1);
NARROW BAND MULTIBURST (Y, R-Y, B-Y)

**Step 1.**
Set the VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13) to on.

**Step 2. D/A output Y frequency characteristic adjustment**

ANALOG VIDEO OUT 1
G(Y)/CN PNL.

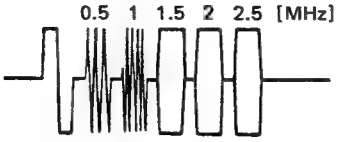



Spec.: 0 - 5 MHz = Flat

●RV603/VA-45/G-1

**Step 3. D/A output B-Y frequency characteristic adjustment**

ANALOG VIDEO OUT 1
B(B-Y)/CN PNL.

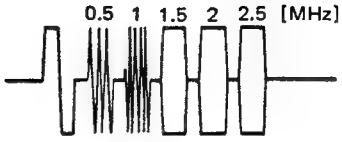



Spec.: 0 - 2.5 MHz = Flat

●RV503/VA-45/E-1

**Step 4. D/A output R-Y frequency characteristic adjustment**

ANALOG VIDEO OUT 1
R(R-Y)/CN PNL.



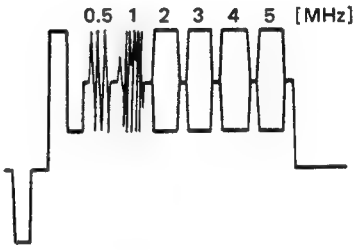

Spec.: 0 - 2.5 MHz = Flat

●RV403/VA-45/C-1

**Step 5.**
Set the VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13) to off. Turn RV106, 206, and 306 on the VA-45 board fully counterclockwise, then check the following section.

**Step 6. A/D output Y frequency characteristic check**

ANALOG VIDEO OUT 1
G(Y)/CN PNL.

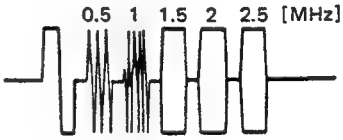



Spec.: 0 - 5 MHz = Flat

If it does not meet the specification, adjust by ●RV306/VA-45/A-1.

**Step 7. A/D output B-Y frequency characteristic adjustment**

ANALOG VIDEO OUT 1
B(B-Y)/CN PNL.




Spec.: 0 - 2.5 MHz = Flat

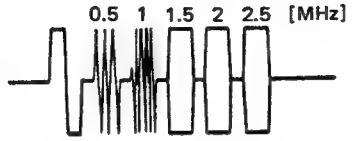
If it does not meet the specification, adjust by ●RV206/VA-45/A-1.

Serial No: Up to 20999 (UC)
Serial No: Up to 11199 (EK)

(9-19. A/D, D/A FREQUENCY CHARACTERISTIC ADJUSTMENT)

**Step 8. A/D output R-Y frequency characteristic adjustment**

ANALOG VIDEO OUT 1
R(R-Y)/CN PNL.




Spec.: 0 - 2.5 MHz = Flat

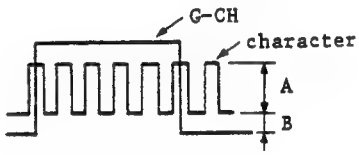
If it does not meet the specification, adjust by ⊘ RV106/VA-45/A-1.

**9-20. CHARACTER ADJUSTMENT**

Connection; See Connection 3, Section 5-4.
Equipment; Waveform monitor
Setting of Switches & Controls;
SUPER (SUPERIMPOSITION)/TC & CHAR
MENU : ON

**Step 1. G-CH character level and offset adjustment**

ANALOG MONITOR OUT
G-CH/CN PNL.




A: 500 ± 15 mV
⊘RV5/IV-14
B: 100 ± 5 mV
⊘RV6/IV-14

**Step 2. R, B-CH check**

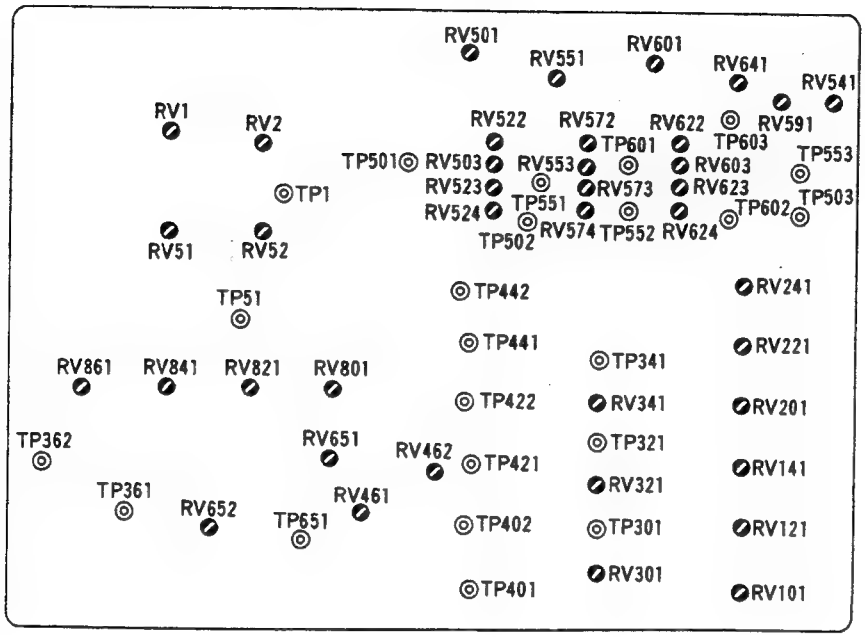
ANALOG MONITOR OUT
R-CH/CN PNL.

B-CH/CN PNL.

Make sure, that the character level is within each signal level.

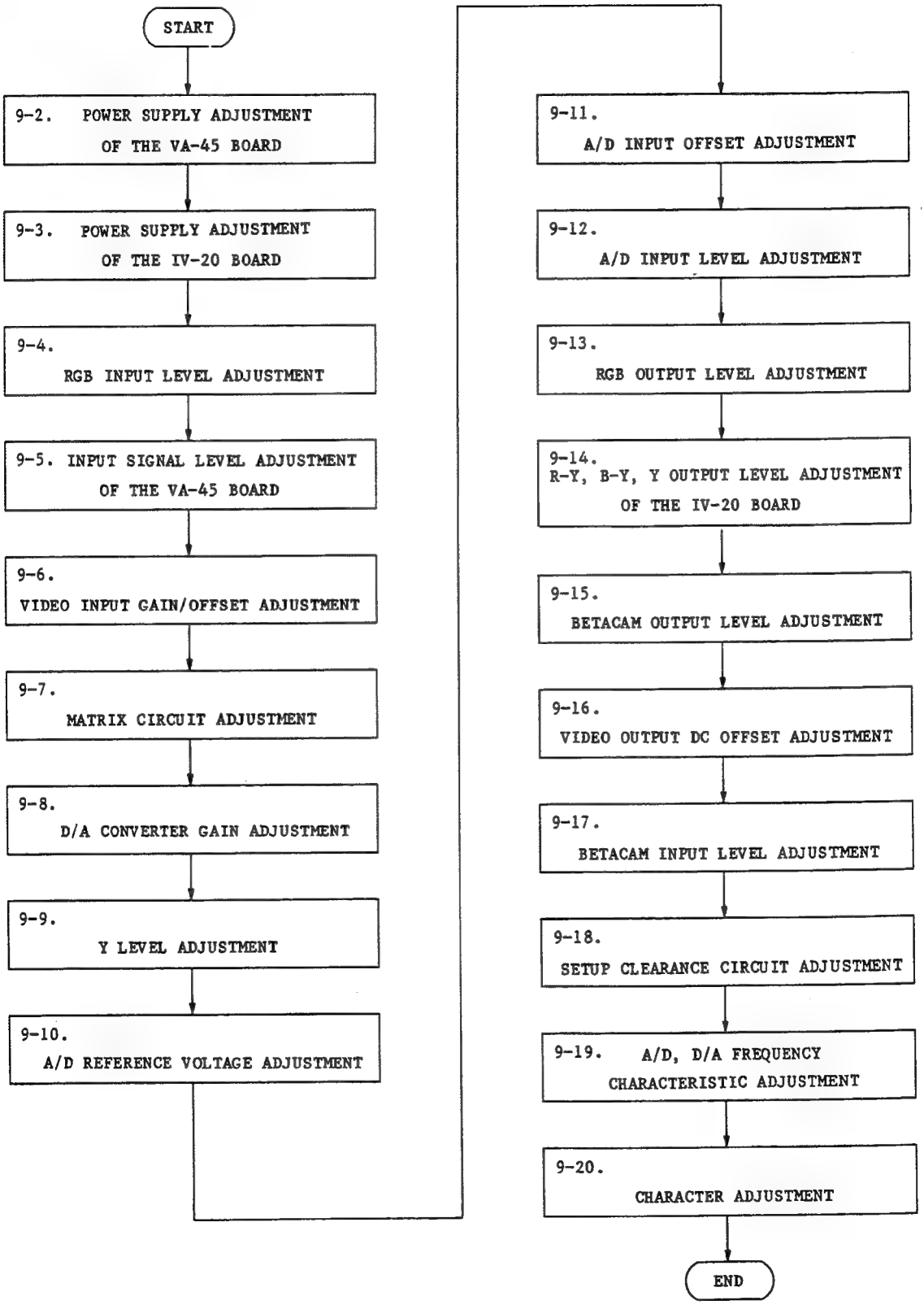
Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

**IV-20 board (component side)**



Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

## 9-1. ALIGNMENT SEQUENCE



Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

## 9-2. POWER SUPPLY ADJUSTMENT OF THE VA-45 BOARD

Equipment; Digital voltmeter
Setting of Switches & Controls;
Same as section 5-5.

**Note:** When any of the following controls is replaced, set the control to the following position before adjusting it.
VA-45 board
RV801, 831, 861 ..... Fully counterclockwise
RV802, 832, 862 ..... Mechanical center position

**Step 1. +12 V voltage adjustment**
TP801/VA-45 = +12.00 ± 0.05 Vdc
⊘RV802/VA-45/A-2

**Step 2. +12 V over-current protective circuit adjustment**
Slowly turn RV801/VA-45 clockwise while observing a voltmeter connected across TP801/VA-45. When the output voltage starts to change, turn RV801 counterclockwise by 1 scale division.

**Step 3. -12 V voltage adjustment**
TP802/VA-45 = -12.00 ± 0.05 Vdc
⊘RV832/VA-45/A-6

**Step 4. -12 V over-current protective circuit adjustment**
Slowly turn RV831/VA-45 clockwise while observing a voltmeter connected across TP802/VA-45. When the output voltage starts to change, turn RV831 counterclockwise by 1 scale division.

**Step 5. -5 V voltage adjustment**
TP803/VA-45 = -5.00 ± 0.05 Vdc
⊘RV862/VA-45/A-8

**Step 6. -5 V over-current protective circuit adjustment**
Slowly turn RV861/VA-45 clockwise while observing a voltmeter connected across TP803/VA-45. When the output voltage starts to change, turn RV861 counterclockwise by 1 scale division.

## 9-3. POWER SUPPLY ADJUSTMENT OF THE IV-20 BOARD

Equipment; Digital voltmeter
Setting of Switches & Controls;
Same as section 5-5.

**Note:** When any of the following controls is replaced, set the control to the following position before adjusting it.
IV-20 board
RV2, 52 ..... Mechanical center position
RV1, 51 ..... Fully counterclockwise

**Step 1. +12 V voltage adjustment**
TP1/IV-20 = +12.00 ± 0.05 Vdc
⊘RV2/IV-20

**Step 2. +12 V over-current protective circuit adjustment**
Slowly turn RV1/IV-20 clockwise while observing a voltmeter connected across TP1/IV-20. When the output voltage starts to change, turn RV1 counterclockwise by 1 scale division.

**Step 3. -12 V voltage adjustment**
TP2/IV-20 = -12.00 ± 0.05 Vdc
⊘RV52/IV-20

**Step 4. -12 V over-current protective circuit adjustment**
Slowly turn RV-51/IV-20 clockwise while observing a voltmeter connected across TP2/IV-20. When the output voltage starts to change, turn RV2 counterclockwise by 1 scale division.

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

## 9-4. RGB INPUT LEVEL ADJUSTMENT

Connection; See Connection 3, Section 5-4.

Equipment; Oscilloscope
Component signal generator

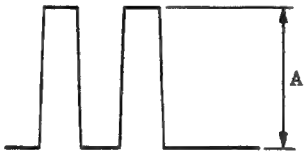
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU/DVR-1000 CONT. PNL.: ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): RGB
Set the short pins of JPI (on the boards with numbers ending with 11) and CN1 (on the boards with numbers ending with 12) to on. (PG-13)
INPUT SW (S3-6/PG-13): ON
BYPASS6 SW (S3-1/PG-13): ON
For other setting same as section 5-5

Input Signal (ANALOG VIDEO INPUT 1):
100% COLOR BARS (RGB) No signal

**Step 1. R gain adjustment**

Input color bars signal.

PICTURE MONITOR OUTPUT
TP32/IV-20

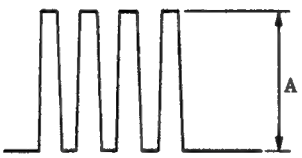



A = 700 ± 10 mVp-p
⊘RV201/IV-20

**Step 2. B gain adjustment**

Input color bar signals.

PICTURE MONITOR OUTPUT
TP18/IV-20

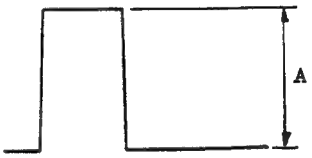



A = 700 ± 10 mVp-p
⊘RV221/IV-20

**Step 3. G gain adjustment**

Input color bars signal.

PICTURE MONITOR OUTPUT
TP17/IV-20




A = 700 ± 10 mVp-p
⊘RV241/IV-20

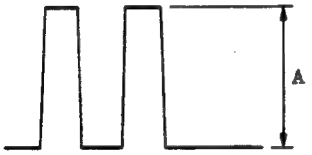
Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

## 9-5. INPUT SIGNAL LEVEL ADJUSTMENT OF THE VA-45 BOARD

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Component signal generator
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU: ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): RGB
BYPASS6 SW (S3-1/PG-13): ON
For other setting same as section 5-5
Input Signal (ANALOG VIDEO INPUT 1):
100% COLOR BARS (RGB)

**Step 1. R level adjustment**

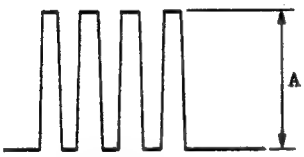
TP101/VA-45




A = 700 ± 10 mVp-p
⊘RV301/IV-20

**Step 2. B level adjustment**

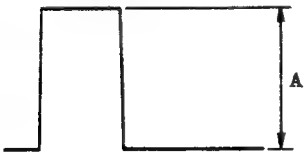
TP201/VA-45




A = 700 ± 10 mVp-p
⊘RV321/IV-20

**Step 3. G level adjustment**

TP301/VA-45




A = 700 ± 10 mVp-p
⊘RV341/IV-20

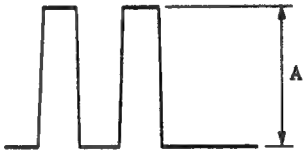
## 9-6. VIDEO INPUT GAIN/OFFSET ADJUSTMENT

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Component video signal generator
Mode of DVR/DVPC-1000;
EE
Setting of Switches & Controls;
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU: ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): RGB
ANALOG VIDEO INPUT SW (S101/VA-45): PRESET
TEST SW (S3/IF-139): ON
For other setting same as section 5-5
Input Signal (ANALOG VIDEO INPUT 1):
100% COLOR BARS (RGB) ↔ No signal

**Step 1. R(R-Y) gain adjustment**

Input color bars signal.

TP102/VA-45




A = 1400 ± 20 mVp-p
⊘RV102/VA-45/A-1

**Step 2. R(R-Y) offset adjustment**

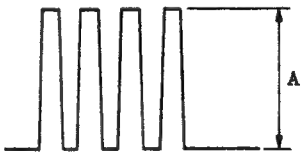
Remove signal from the input.

TP102/VA-45 = 0 ± 40 mVdc
⊘RV101/VA-45/A-1

**Step 3. B(B-Y) gain adjustment**

Input color bars signal.

TP202/VA-45




A = 1400 ± 20 mVp-p
⊘RV202/VA-45/A-1

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

(9-6. VIDEO INPUT GAIN/OFFSET ADJUSTMENT)

**Step 4. B(B-Y) offset adjustment**

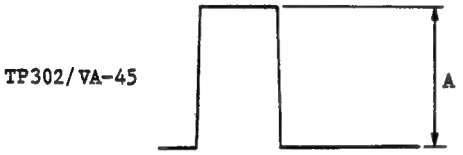
Remove signal from the input.

TP202/VA-45 = 0 ± 40 mVdc

⊘ RV201/VA-45/A-1

**Step 5. G(Y) gain adjustment**

Input color bars signal.




A = 1400 ± 20 mVp-p

⊘RV302/VA-45/B-1

**Step 6. G(Y) offset adjustment**

Remove signal from the input.

TP302/VA-45 = 0 ± 40 mVdc

⊘RV301/VA-45/B-1

## 9-7. MATRIX CIRCUIT ADJUSTMENT

Connection; See Connection 3, Section 5-4.

Equipment; Oscilloscope

Component video signal generator

(GBR output)

Mode of DVR/DVPC-1000;

EE

Setting of Switches & Controls;

ANALOG VIDEO INPUT SW

(S101/VA-45): PRESET

PROCESSOR CONT. MODE/SYSTEM SETUP SUB

MENU: ON

VIDEO SELECT RGB/Y, R-Y, B-Y SW

(S4/PG-13): RGB

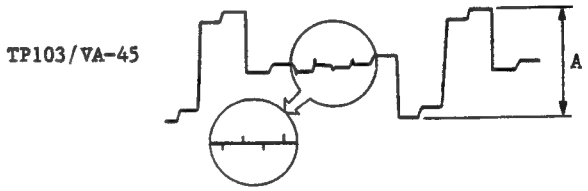
TEST SW (S3/IF-139): ON

For other setting same as section 5-5

Input Signal (ANALOG VIDEO INPUT 1):

100% COLOR BARS (RGB)

**Step 1. R-Y matrix adjustment**



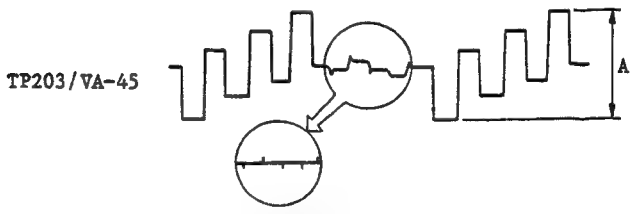

Minimize the difference in level.

⊘RV104/VA-45/A-1

A = 1400 ± 20 mVp-p

⊘RV105/VA-45/A-1

**Step 2. B-Y matrix adjustment**




Minimize the difference in level.

⊘RV204/VA-45/A-1

A = 1400 ± 20 mVp-p

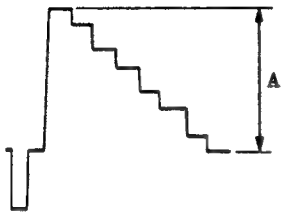
⊘RV205/VA-45/A-1

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

(9-7. MATRIX CIRCUIT ADJUSTMENT)

**Step 3. Y matrix adjustment**

TP303/VA-45




A = 1400 ± 20 mVp-p

⊘RV305/VA-45/B-1

**9-8. D/A CONVERTER GAIN ADJUSTMENT**

Connection; See Connection 3, Section 5-4.

Equipment; Oscilloscope

Setting of Switches & Controls;

TEST SW (S3/IF-139): ON

BYPASS6 SW (S3-1/PG-13): ON

VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13): ON

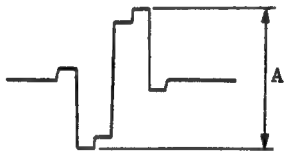
ANALOG VIDEO OUTPUT SW (S701/VA-45): PRESET

TEST SIGNAL SELECT SW (S1-1/VA-45): OFF

For other setting same as section 5-5

**Step 1. R-Y level adjustment**

TP403/VA-45

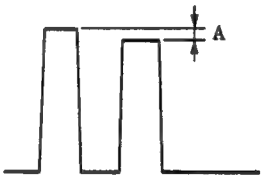



A = 710 ± 10 mVp-p

⊘RV401/VA-45/C-1

**Step 2. R dematrix adjustment**

TP402/VA-45

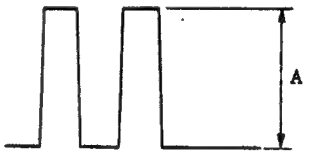



A = Minimum

⊘RV601/VA-45/G-1

**Step 3. R level adjustment**

TP402/VA-45




A = 710 ± 10 mVp-p

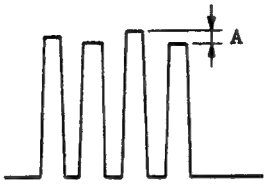
⊘RV404/VA-45/E-1

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

(9-8. D/A CONVERTER GAIN ADJUSTMENT)

**Step 4. B dematrix adjustment**

TP502/VA-45

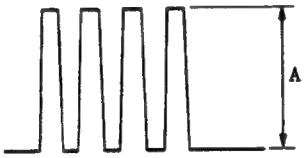



A = Minimum

⊘RV501/VA-45/E-1

**Step 5. B level adjustment**

TP502/VA-45

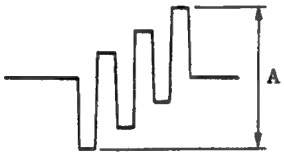



A = 710 ± 10 mVp-p

⊘RV504/VA-45/F-1

**Step 6. B-Y level check**

TP503/VA-45

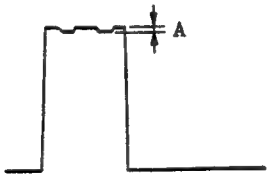



A = 710 ± 10 mVp-p

If it does not meet the specification, repeat adjustments from step 1.

**Step 7. G dematrix adjustment**

TP602/VA-45

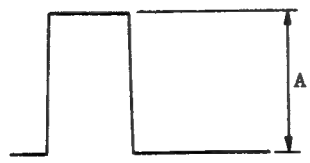



A = Minimum

⊘RV604/VA-45/G-1

**Step 8. G level adjustment**

TP602/VA-45




A = 710 ± 10 mVp-p

⊘RV605/VA-45/H-1

**9-9. Y LEVEL ADJUSTMENT**

Connection; See Connection 3, Section 5-4.

Equipment; Oscilloscope

Setting of Switches & Controls;

TEST SW (S3/IF-139): ON

BYPASS6 SW (S3-1/PG-13): ON

VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13): ON

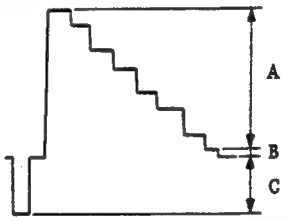
ANALOG VIDEO OUTPUT SW (S701/VA-45): PRESET

TEST SIGNAL SELECT SW (S1-1/VA-45): OFF

For other setting same as section 5-5

**Step 1. BETACAM OUT Y level adjustment (525/60 system)**

TP603/VA-45




A = 660 ± 10 mV ⊘RV606/VA-45/H-1

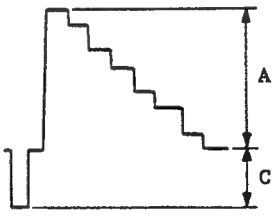
B = 54 ± 7 mV ⊘RV703/VA-45/E-1

C = 286 ± 5 mV ⊘RV705/VA-45/E-1

**Note:** When adjust the VA-45 board with board number 1-620-781-11, observe at edge connector B12c on the VA-45 board. Adjust the portion of C by RV702.

**Step 2. BETACAM OUT Y level adjustment (625/50 system)**

TP603/VA-45




Check; A = 700 ± 10 mV

Adjust; C = 300 ± 5 mV ⊘RV702/VA-45/E-1

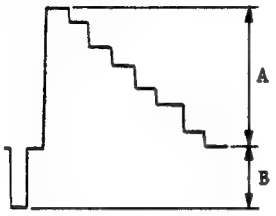
**Note:** When adjust the VA-45 board with board number 1-620-781-11, observe at edge connector B12c on the VA-45 board.

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

(9-9. Y LEVEL ADJUSTMENT)

**Step 3. Y level adjustment/check**

TP604/VA-45




Check: A = 710 ± 10 mV

Adjustment: B = 304 ± 5 mV ●RV704/VA-45/E-1

**Note: When adjust the VA-45 board with board number 1-620-781-11, observe at TP603 on the VA-45 board.**

If it does not meet the specification, repeat adjustment of section 9-7 "D/A converter gain adjustment."

**9-10. A/D REFERENCE VOLTAGE ADJUSTMENT**

Equipment; Digital voltmeter

Setting of Switches & Controls;

Same as section 5-5

**Step 1. R-Y A/D reference voltage adjustment**

TP105/VA-45 = -2.00 ± 0.01 Vdc

●RV109/VA-45/A-1

**Step 2. B-Y A/D reference voltage adjustment**

TP205/VA-45 = -2.00 ± 0.01 Vdc

●RV209/VA-45/A-1

**Step 3. Y A/D reference voltage adjustment**

TP305/VA-45 = -2.00 ± 0.01 Vdc

●RV309/VA-45/B-1

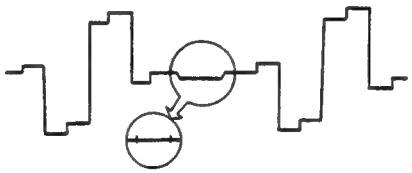
Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

## 9-11. A/D INPUT OFFSET ADJUSTMENT

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Component signal generator
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
For other setting same as section 5-5
Input signal (ANALOG VIDEO INPUT 1):
100% COLOR BARS (Y, R-Y, B-Y)

**Step 1. R-Y offset adjustment**

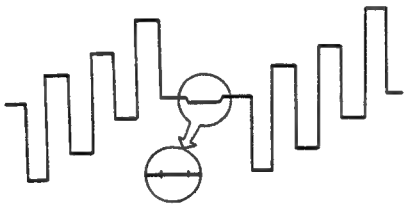
TP401/VA-45



Minimize the difference in level.
⊘RV108/VA-45/A-1

**Step 2. B-Y offset adjustment**

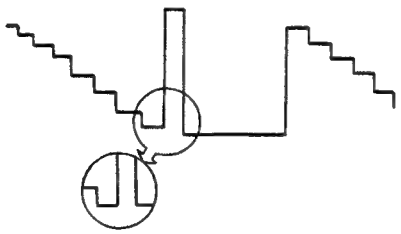
TP501/VA-45



Minimize the difference in level.
⊘RV208/VA-45/A-1

**Step 3. Y offset adjustment**

TP601/VA-45



Minimize the difference in level.
⊘RV308/VA-45/B-1

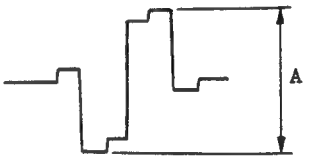
## 9-12. A/D INPUT LEVEL ADJUSTMENT

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Component signal generator
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
TEST SIGNAL SELECT SW
(S1-1/VA-45): OFF
For other setting same as section 5-5
Input Signal (ANALOG VIDEO INPUT 1):
100% COLOR BARS

**Step 1. R-Y input level adjustment**

Adjust RV107 by changing the position of VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13) so that the level with S3-2 = OFF is equal to the level with S3-2 = ON.

TP401/VA-45

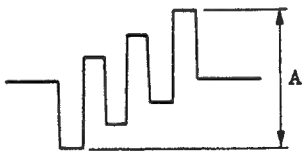



Spec.; The level (A) with S3-2/PG-13 = OFF is equal to the level with S3-2/PG-13 = ON.
⊘RV107/VA-45/A-1

**Step 2. B-Y input level adjustment**

Adjust RV207 by changing the position of VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13) so that the level with S3-2 = OFF is equal to the level with S3-2 = ON.

TP501/VA-45




Spec.: The level (A) with S3-2/PG-13 = OFF is equal to the level with S3-2/PG-13 = ON.
⊘RV207/VA-45/A-1

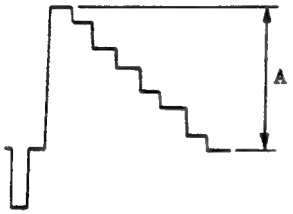
Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

(9-12. A/D INPUT LEVEL ADJUSTMENT)

**Step 3. Y input level adjustment**

Adjust RV307 by changing the position of VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13) so that the level with S3-2 = OFF is equal to the level with S3-2 = ON.

TP601/VA-45




Spec.: The level (A) with S3-2/PG-13 = OFF is equal to the level with S3-2/PG-13 = ON.
⊘ RV307/VA-45/C-1

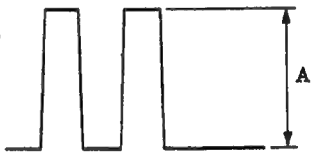
## 9-13. RGB OUTPUT LEVEL ADJUSTMENT OF THE IV-20 BOARD

### 9-13-1. RGB Output Level Adjustment of the IV-20 Board (1)

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13): ON
VIDEO OUTPUT RGB/Y, R-Y, B-Y SW (S3-5/PG-13): OFF (RGB)
TEST SIGNAL SELECT SW (S1-1/VA-45): OFF
ANALOG VIDEO OUTPUT SW (S701/VA-45): PRESET
For other setting same as section 5-5

**Step 1. R output level adjustment of the IV-20 board**

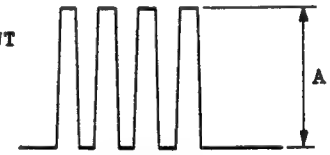
PICTURE MONITOR OUTPUT
R/CN PNL.




A = 700 ± 10 mVp-p
⊘RV501/IV-20

**Step 2. B output level adjustment of the IV-20 board**

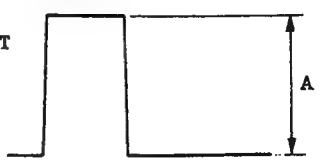
PICTURE MONITOR OUTPUT
B/CN PNL.




A = 700 ± 10 mVp-p
⊘RV551/IV-20

**Step 3. G output level adjustment of the IV-20 board**

PICTURE MONITOR OUTPUT
Y/CN PNL.




A = 700 ± 10 mVp-p
⊘RV601/IV-20

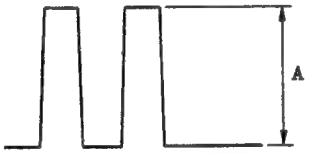
Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

## 9-13-2. RGB Output Level Adjustment of the IV-20 Board (2)

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
VIDEO TEST SIGNAL OUTPUT SW
(S3-2/PG-13): ON
VIDEO OUTPUT RGB/Y, R-Y, B-Y SW
(S3-5/PG-13): OFF (RGB)
TEST SIGNAL SELECT SW
(S1-1/VA-45): OFF
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
For other setting same as section 5-5

**Step 1. R output level adjustment**

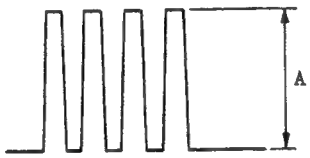
ANALOG VIDEO OUTPUT 1
R1(R-Y1)/CN PNL.
R2(R-Y2)/CN PNL.




A = 700 ± 10 mVp-p
R2(Right side): ⊘RV523/IV-20
R1(Left side): ⊘RV503/IV-20
R2 offset adjustment B = 0V : ⊘RV524/IV-20

**Step 2. B output level adjustment**

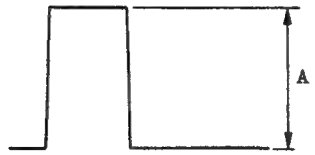
ANALOG VIDEO OUTPUT 1
R1(B-Y1)/CN PNL.
R2(B-Y2)/CN PNL.




A = 700 ± 10 mVp-p
B2(Right side): ⊘RV573/IV-20
B1(Left side): ⊘RV553/IV-20
B2 offset adjustment B = 0V : ⊘RV574/IV-20

**Step 3. B output level adjustment**

ANALOG VIDEO OUTPUT 1
G1(Y1)/CN PNL.
G2(Y2)/CN PNL.



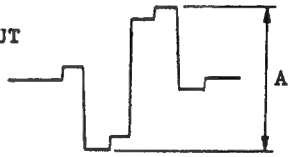

A = 700 ± 10 mVp-p
G2(Right side): ⊘RV623/IV-20
G1(Left side): ⊘RV603/IV-20
G2 offset adjustment B = 0V : ⊘RV624/IV-20

## 9-14. R-Y, B-Y, Y OUTPUT LEVEL ADJUSTMENT OF THE IV-20 BOARD

Connection; See Connection 3, Section 5-4.
Equipment; Oscilloscope
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
VIDEO TEST SIGNAL OUTPUT SW
(S3-2/PG-13): ON
TEST SIGNAL SELECT SW
(S1-1/VA-45): OFF
INPUT SW
(S3-6/PG-13): OFF
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
SHORT SOCETT
CN542 → CN543 CN592 → CN593
OFF ON OFF ON
CN642 → CN643
OFF ON
For other setting same as section 5-5

**Step 1. R-Y output level adjustment**

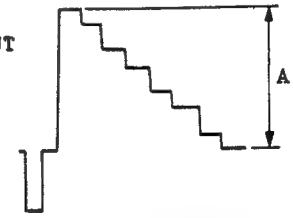
PICTURE MONITOR OUTPUT
R/CN PNL.




A = 700 ± 10 mVp-p
⊘RV522/IV-20

**Step 2. B-Y output level adjustment**

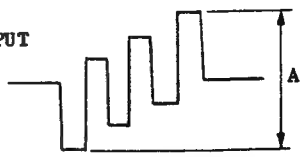
PICTURE MONITOR OUTPUT
B/CN PNL.




A = 700 ± 10 mVp-p
⊘RV572/IV-20

**Step 3. Y output level adjustment**

PICTURE MONITOR OUTPUT
G/CN PNL.




A = 700 ± 10 mVp-p
⊘ RV622/IV-20

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

## 9-15-1. BETACAM OUTPUT LEVEL ADJUSTMENT

Connection; See Connection 3, Section 5-4.

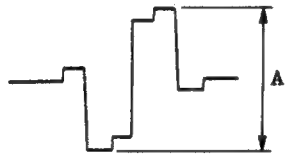
Equipment; Oscilloscope

Setting of Switches & Controls;

TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
VIDEO TEST SIGNAL OUTPUT SW
(S3-2/PG-13): ON
TEST SIGNAL SELECT SW
(S1-1/VA-45): OFF
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
For other setting same as section 5-5

**Step 1. R-Y output level adjustment**

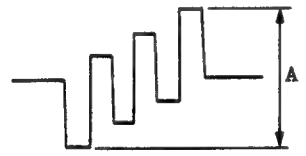
TP503/IV-20




A = 1870 ± 20 mVp-p (CN541: ON)
EBU : A = 1400 ± 20 mVp-p (CN541: OFF)
⊘RV541/IV-20

**Step 2. B-Y output level adjustment**

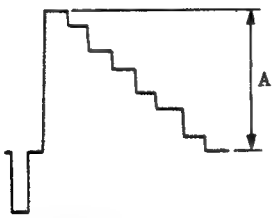
TP553/IV-20




A = 1870 ± 20 mVp-p (CN591: ON)
EBU : A = 1400 ± 20 mVp-p (CN591: OFF)
⊘RV591/IV-20

**Step 3. Y output level adjustment**

TP603/IV-20




A = 1400 ± 20 mVp-p
⊘RV641/IV-20

## 9-15-2. WFM OUTPUT LEVEL ADJUSTMENT

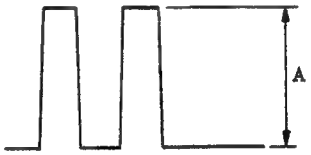
Connection; See Connection 3, Section 5-4.

Equipment; Oscilloscope

Setting of Switches & Controls;

TEST SW (S3/IF-139): ON
BYPASS6 SW (S3-1/PG-13): ON
VIDEO TEST SIGNAL OUTPUT SW
(S3-2/PG-13): ON
TEST SIGNAL SELECT SW
(S1-1/VA-45): OFF
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
WFM SIGNAL SELECT/MON MENU/
DVR-1000 CONT. PNL.: VIDEO (RED)
CN542: ON CN543: OFF
CN592: ON CN593: OFF
CN642: ON CN643: OFF
For other setting same as section 5-5

WFM OUTPUT/CN PNL.




A = 700 ± 10 mVp-p
⊘RV652/IV-20

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

### 9-15-3. WFM INPUT LEVEL ADJUSTMENT

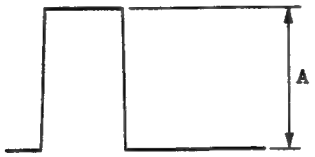
Equipment; Oscilloscope

Setting of Switches & Controls;

Set to remote mode on the control panel of the DVR-1000 and set the WFM Select to CTL.

Apply a 0.7 Vp-p signal to the WFM INPUT.

WFM OUT/ON PNL.




A = 700 ± 10 mVp-p

●RV651/IV-20

### 9-16. VIDEO OUTPUT DC OFFSET ADJUSTMENT

Connection; See Connection 3, Section 5-4.

Equipment; Waveform monitor

Component video signal generator

Setting of Switches & Controls;

TEST SW (S3/IF-139): ON

PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU : ON

VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): RGB

BYPASS6 SW (S3-1/PG-13): ON

VIDEO OUTPUT RGB/Y, R-Y, B-Y SW (S3-5/PG-13): OFF (RGB)

ANALOG VIDEO INPUT SW (S101/VA-45): PRESET

ANALOG VIDEO OUTPUT SW (S701/VA-45): PRESET

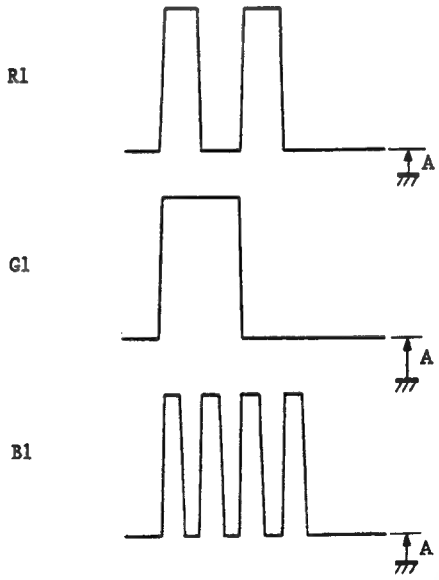
For other setting same as section 5-5

Input Signal (ANALOG VIDEO INPUT 1):

100% COLOR BARS (RGB)

**Adjustment IV-14 board**

Measure the DC offset voltage of each R/G/B channel at ANALOG VIDEO OUTPUT 1 (R1, G1, B1).




When the difference of offset voltage among three channels is 50 mV or more, mount the following resistors, which is selected according to the difference of voltage, to the channel with the lowest offset voltage.

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

(9-16. VIDEO OUTPUT DC OFFSET ADJUSTMENT)

**Mount position**

In case R1-CH is lower ...

Between pin 1 and pin 3 of IC23

In case B1-CH is lower ...

Between pin 1 and pin 3 of IC28

In case G1-CH is lower ...

Between pin 1 and pin 3 of IC33

**Mount resistor**

| Voltage difference(mV) | Mount resistor | SONY part number |
|---|---|---|
| 15 - 25 | 24 k , METAL, 1/6W | 1-215-454-00 |
| 26 - 40 | 15 k , METAL, 1/6W | 1-215-449-00 |
| 41 - 60 | 10 k , METAL, 1/6W | 1-215-445-00 |
| 61 - 85 | 6.8 k , METAL, 1/6W | 1-215-441-00 |
| 86 - 120 | 5.1 k , METAL, 1/6W | 1-215-438-00 |

Measure the difference of offset voltage between channels at ANALOG VIDEO OUTPUT 1 (R2, G2, B2) and PICTURE MONITOR OUTPUT (R, G, B) in a similar manner, then mount a resistor to the channel with the lower voltage.

**Mount position**

ANALOG VIDEO OUTPUT 1

In case R2-CH is lower ...

Between pin 1 and pin 3 of IC22

In case B2-CH is lower ...

Between pin 1 and pin 3 of IC27

In case G2-CH is lower ...

Between pin 1 and pin 3 of IC32

PICTURE MONITOR OUTPUT

In case R-CH is lower ...

Between pin 1 and pin 3 of IC54

In case B-CH is lower ...

Between pin 1 and pin 3 of IC50

In case G-CH is lower ...

Between pin 1 and pin 3 of IC46

**9-17. BETACAM INPUT LEVEL ADJUSTMENT**

Connection; See Connection 3, Section 5-4.
(Connect the ANALOG VIDEO INPUT-2 connector and the ANALOG VIDEO OUTPUT-2 connector with a cable.)

Equipment; Oscilloscope

Setting of Switches & Controls;

TEST SW (S3/IF-139): ON
ANALOG VIDEO INPUT SW (S101/VA-45): PRESET
ANALOG VIDEO OUTPUT SW (S701/VA-45): PRESET
TEST SIGNAL SELECT SW (S1-1/VA-45): OFF
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU/DVR-1000 CONT. PNL.: ON
Set the short pins of JP1 (on the boards with numbers ending with 11) and CN1 (on the boars with numbers ending with 12) to on. (PG-13)
INPUT SW (S3-6/PG-13): ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): Y, R-Y, B-Y
VIDEO SELECT BNC/MULTI SW (S5/PG-13): MULTI
BYPASS6 SW (S3-1/PG-13): ON
For other setting same as section 5-5

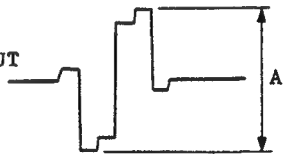
Input Signal (ANALOG VIDEO INPUT 2);

The signal of ANALOG VIDEO OUTPUT-2 connector output (Y, R-Y, B-Y: color bars) is used as an input signal.

**Step 1. R-Y gain adjustment**

Input color bars signal.

PICTURE MONITOR OUTPUT
R/CN PNL.




A = 700 ± 10 mVp-p

●RV101/IV-20

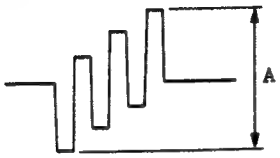
EBU level CN101: ON, other levels: OFF

(9-17. BETACAM INPUT LEVEL ADJUSTMENT)

**Step 2. B-Y gain adjustment**

Input color bars signal.

PICTURE MONITOR OUTPUT
B/CN PNL.

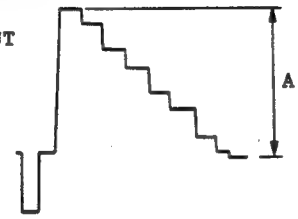



A = 700 ± 10 mVp-p
⊘RV121/IV-20

**Step 3. Y gain adjustment**

Input color bars signal.

PICTURE MONITOR OUTPUT
G/CN PNL.




A = 700 ± 10 mVp-p
⊘RV141/IV-20

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

## 9-18. SETUP CLEARANCE CIRCUIT ADJUSTMENT (in case of 525/60 line standard only)

Connection; See Connection 3, Section 5-4.
(Connect the ANALOG VIDEO INPUT-2 connector and the ANALOG VIDEO OUTPUT-2 connector with a cable.)

Equipment; Oscilloscope
Component signal generator

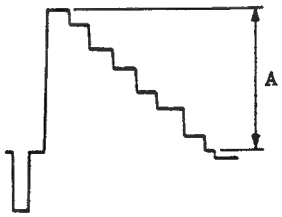
Mode of DVR/DVPC-1000;
EE

Setting of Switches & Controls;
ANALOG VIDEO INPUT SW
(S101/VA-45): PRESET
ANALOG VIDEO OUTPUT SW
(S701/VA-45): PRESET
VIDEO TEST SIGNAL OUTPUT SW
(S3-2/PG-13): ON
TEST SIGNAL SELECT SW
(S1-1/VA-45): OFF
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU : ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW
(S4/PG-13): Y, R-Y, B-Y
VIDEO SELECT BNC/MULTI SW
(S5/PG-13): MULTI
TEST SW (S3/IF-139): ON
SYSTEM SELECT SW (S2/IF-139): 525
For other setting same as section 5-5

Input Signal (ANALOG VIDEO INPUT 2);
The signal of ANALOG VIDEO OUTPUT-2 connector output (Y, R-Y, B-Y: color bars) is used as an input signal.

**VA-45 board adjustment**

TP302




A = 1400 ± 20 mVp-p
⊘RV303/VA-45/A-1

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

## 9-19. A/D, D/A FREQUENCY CHARACTERISTIC ADJUSTMENT

Connection; See Connection 3, Section 5-4.

Equipment; Oscilloscope
Component video signal generator

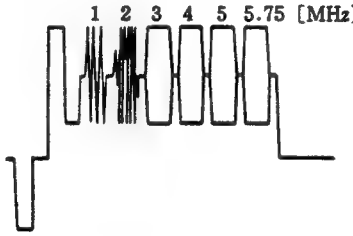
Setting of Switches & Controls;
TEST SW (S3/IF-139): ON
PROCESSOR CONT. MODE/SYSTEM SETUP SUB MENU: ON
VIDEO SELECT RGB/Y, R-Y, B-Y SW (S4/PG-13): Y, R-Y, B-Y
VIDEO SELECT BNC/MULTI SW (S5/PG-13): BNC
BYPASS6 SW (S3-1/PG-13): ON
VIDEO OUTPUT RGB/Y, R-Y, B-Y SW (S3-5/PG-13): ON (Y, R-Y, B-Y)
TEST SIGNAL SELECT SW (S1-1/VA-45): ON
For other setting same as section 5-5

Input Signal (ANALOG VIDEO INPUT 1);
NARROW BAND MULTIBURST (Y, R-Y, B-Y)

**Step 1.**
Set the VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13) to on.

**Step 2. D/A output Y frequency characteristic adjustment**

ANALOG VIDEO OUT 1
G(Y)/CN PNL.




Spec.: 0 - 5 MHz = Flat
RV603/VA-45/G-1

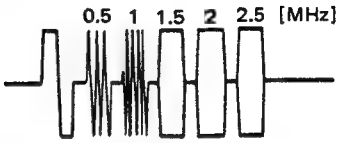
**Step 3. D/A output B-Y frequency characteristic adjustment**

ANALOG VIDEO OUT 1
B(B-Y)/CN PNL.

Spec.: 0 - 2.5 MHz = Flat
RV503/VA-45/E-1

**Step 4. D/A output R-Y frequency characteristic adjustment**

ANALOG VIDEO OUT 1
R(R-Y)/CN PNL.

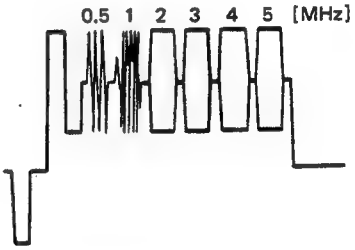



Spec.: 0 - 2.5 MHz = Flat
RV403/VA-45/C-1

**Step 5.**
Set the VIDEO TEST SIGNAL OUTPUT SW (S3-2/PG-13) to off. Turn RV106, 206, and 306 on the VA-45 board fully counterclockwise, then check the following section.

**Step 6. A/D output Y frequency characteristic check**

ANALOG VIDEO OUT 1
G(Y)/CN PNL.

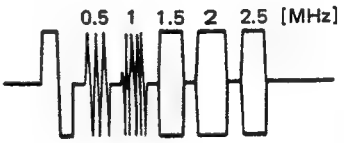



Spec.: 0 - 5 MHz = Flat

If it does not meet the specification, adjust by RV306/VA-45/A-1.

**Step 7. A/D output B-Y frequency characteristic adjustment**

ANALOG VIDEO OUT 1
B(B-Y)/CN PNL.




Spec.: 0 - 2.5 MHz = Flat

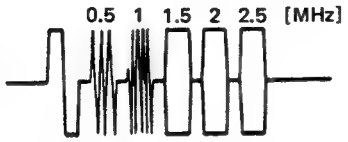
If it does not meet the specification, adjust by RV206/VA-45/A-1.

Serial No: 21001 and Higher (UC)
Serial No: 11201 and Higher (EK)

(9-19. A/D, D/A FREQUENCY CHARACTERISTIC ADJUSTMENT)

**Step 8. A/D output R-Y frequency characteristic adjustment**

ANALOG VIDEO OUT 1
R(R-Y)/CN PNL.




Spec.: 0 - 2.5 MHz = Flat

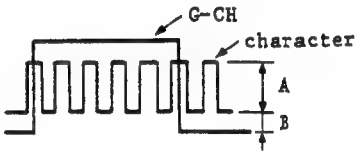
If it does not meet the specification, adjust by ⊘RV106/VA-45/A-1.

**9-20. CHARACTER ADJUSTMENT**

Connection; See Connection 3, Section 5-4.
Equipment; Waveform monitor
Setting of Switches & Controls;
SUPER (SUPERIMPOSITION)/TC & CHAR
MENU : ON

**Step 1. G-CH character level and offset adjustment**

ANALOG MONITOR OUT
G-CH/CN PNL.




A: 500 ± 15 mV
⊘RV461/IV-20
B: 100 ± 5 mV
⊘RV462/IV-20

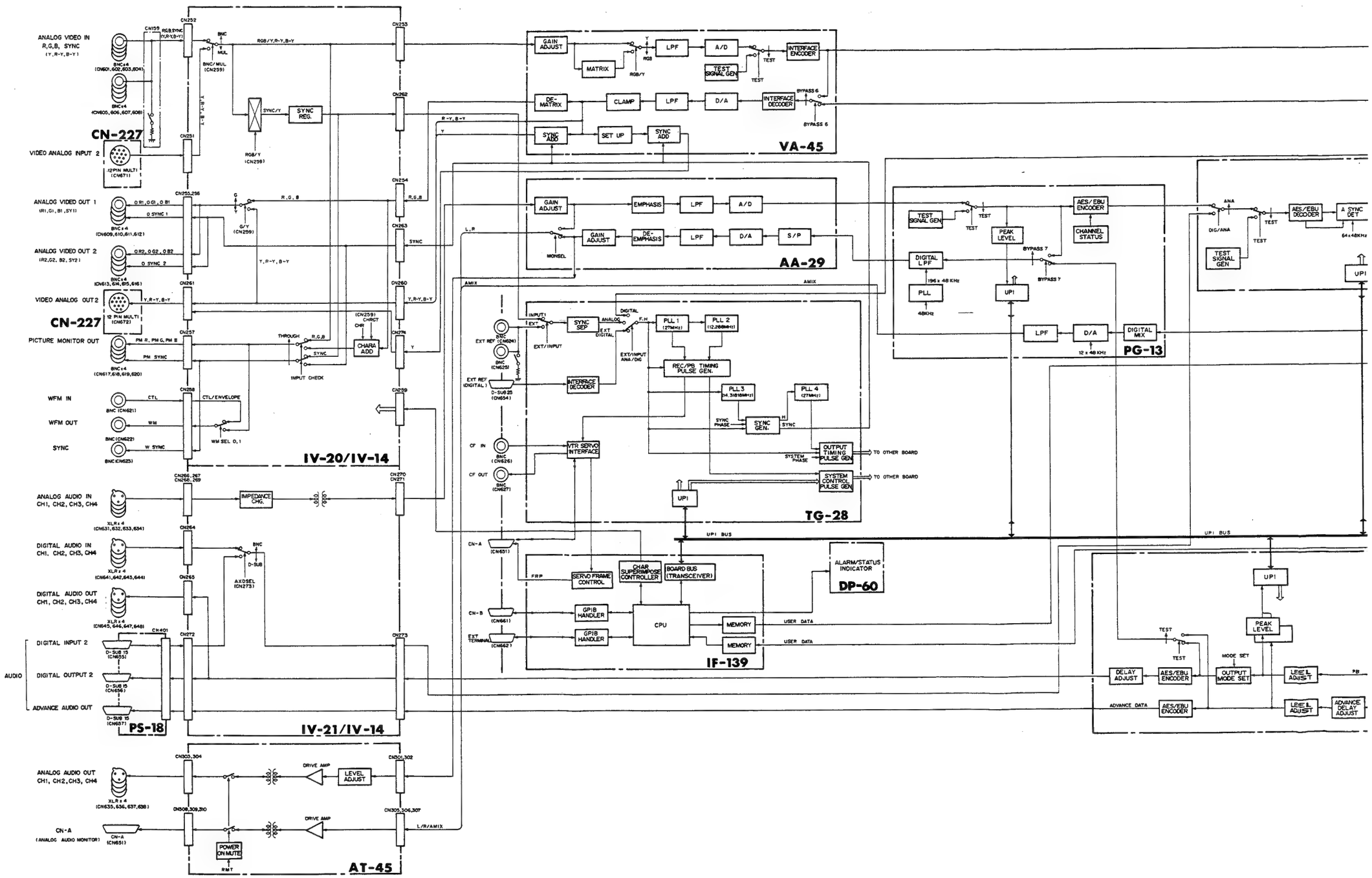
**Step 2. R, B-CH check**

ANALOG MONITOR OUT
R-CH/CN PNL.

B-CH/CN PNL.

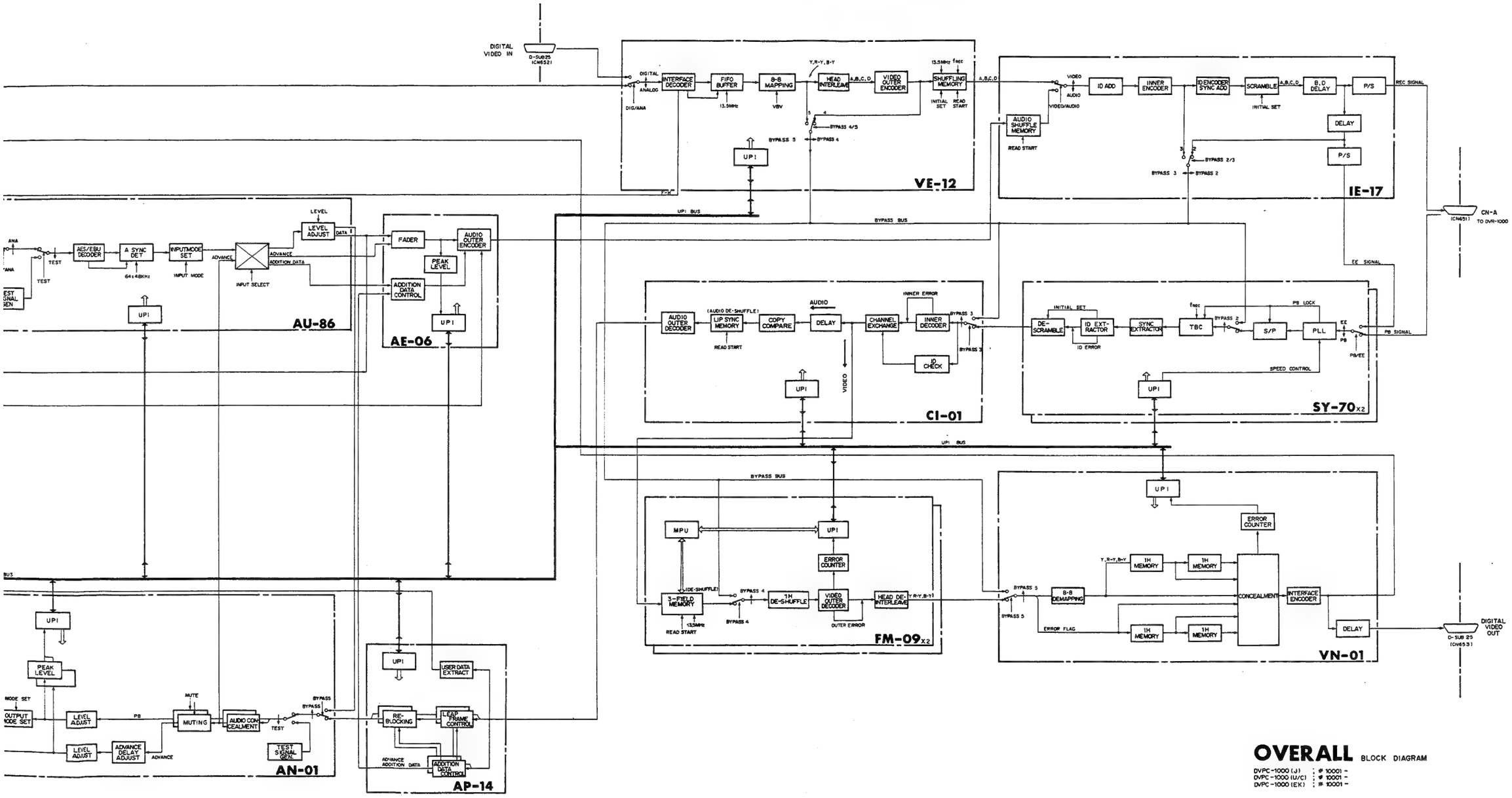
Make sure, that the character level is within each signal level.

# SECTION A
# BLOCK DIAGRAMS




A-1

A-2

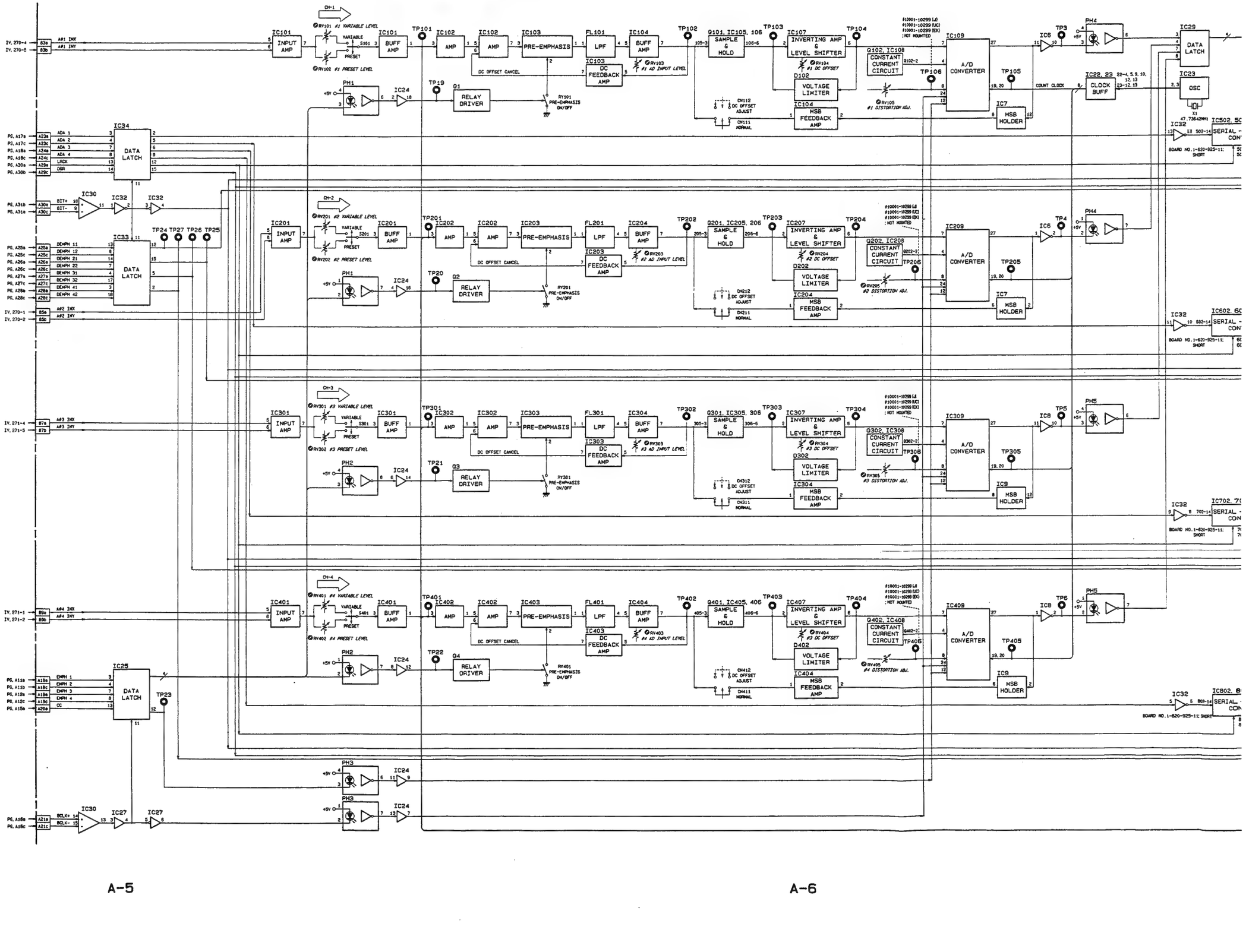


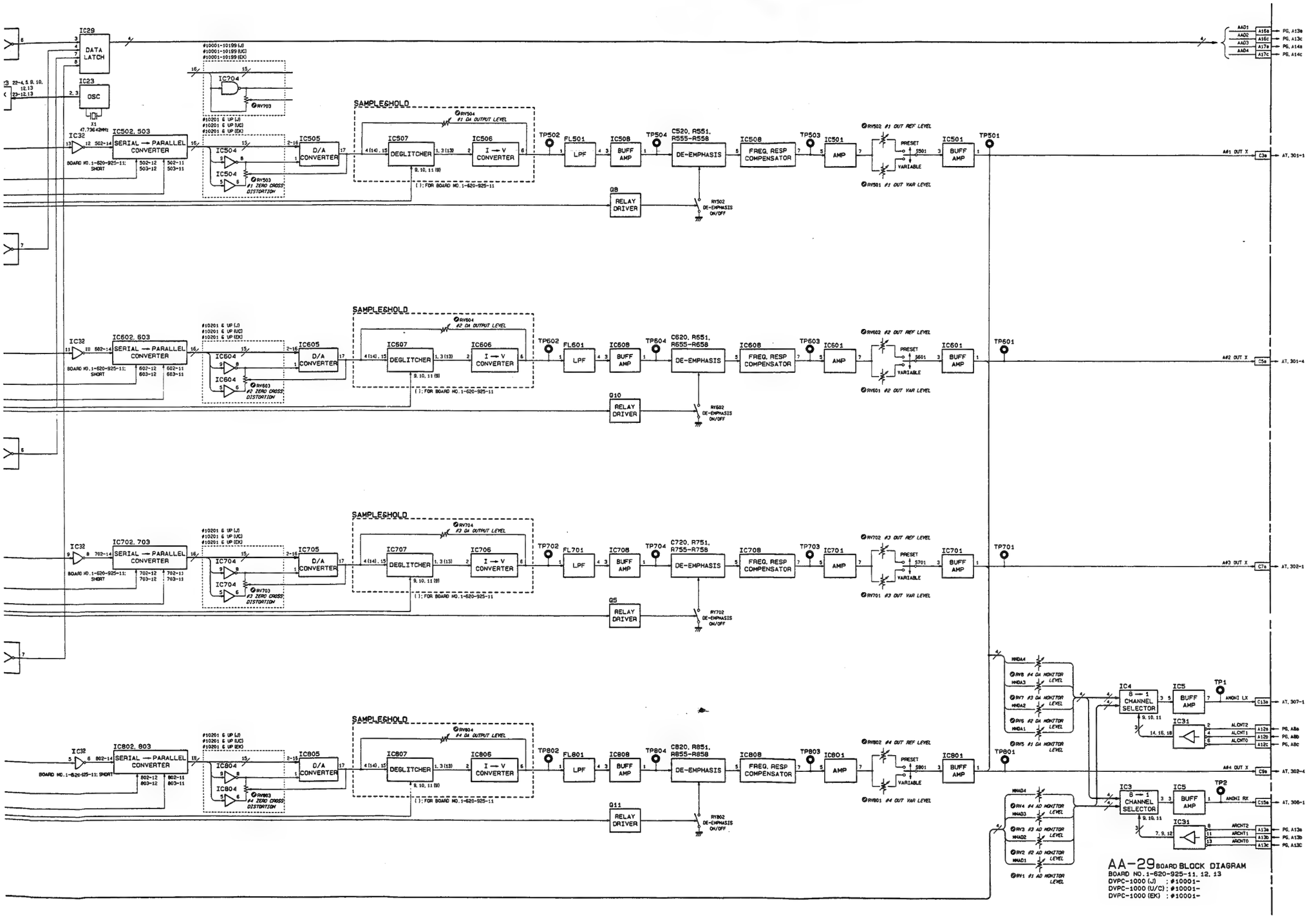

**OVERALL** BLOCK DIAGRAM

DVPC-1000 (J) : # 10001 -
DVPC-1000 (U/C) : # 10001 -
DVPC-1000 (EK) : # 10001 -

## AA-29 BOARD

Audio A/D, D/A Converter



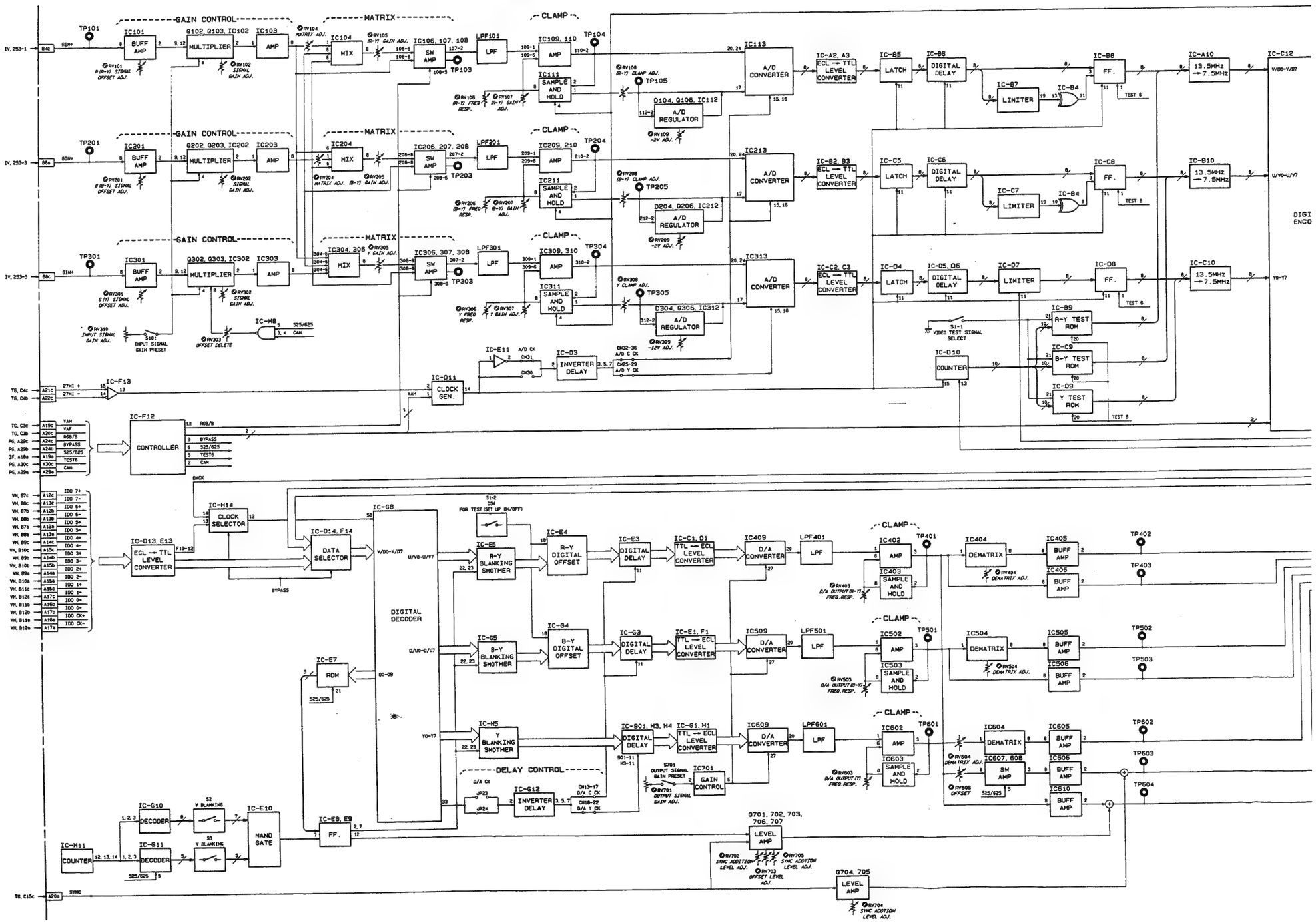


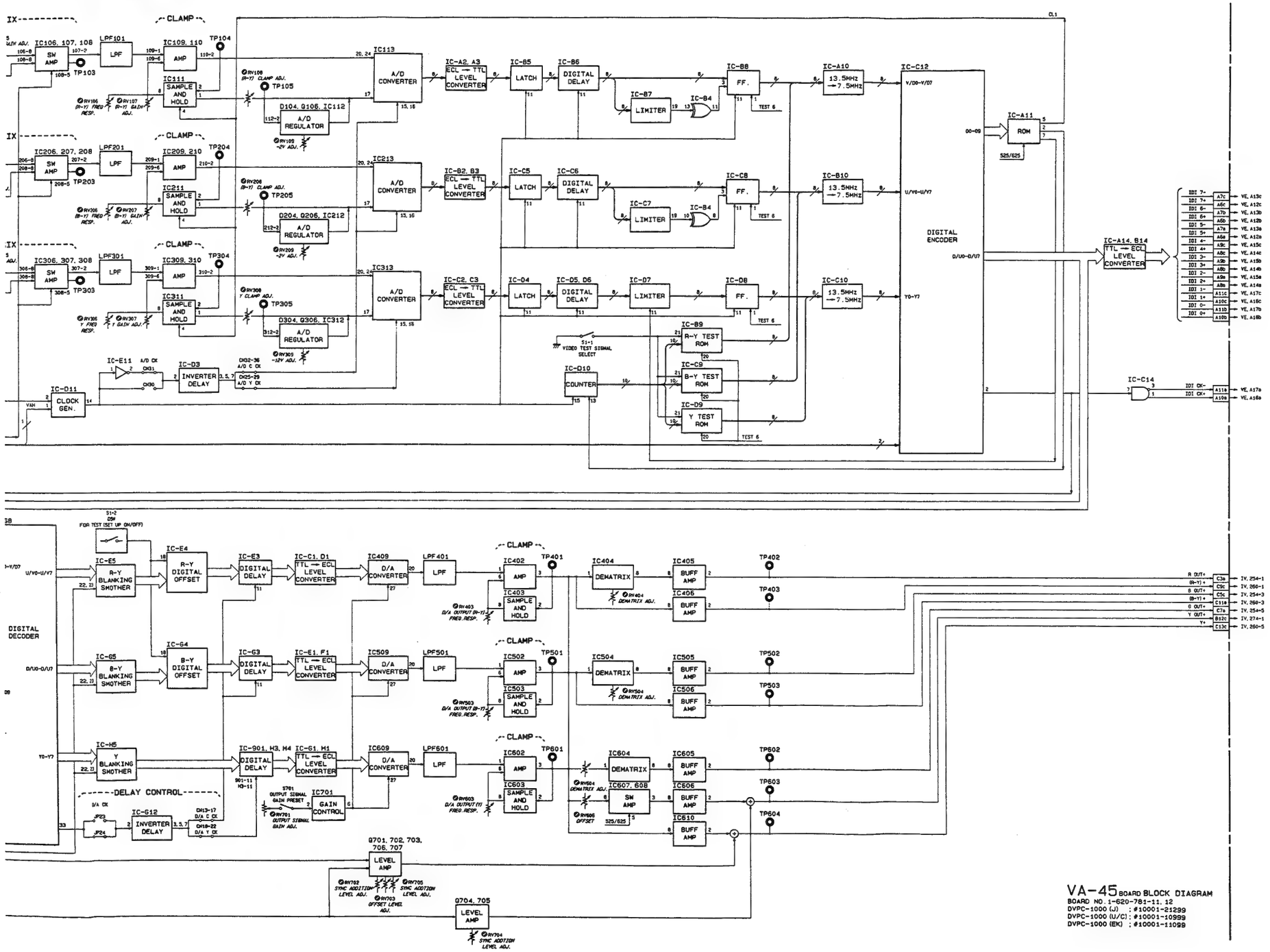

AA-29 BOARD BLOCK DIAGRAM
BOARD NO.1-620-925-11, 12, 13
DVPC-1000 (J) : #10001-
DVPC-1000 (U/C) : #10001-
DVPC-1000 (EK) : #10001-

## VA-45 BOARD

Video A/D, D/A Converter

| |
|---|
| # 10001 TO 21299 (J) |
| # 10001 TO 10999 (UC) |
| # 10001 TO 11099 (EK) |



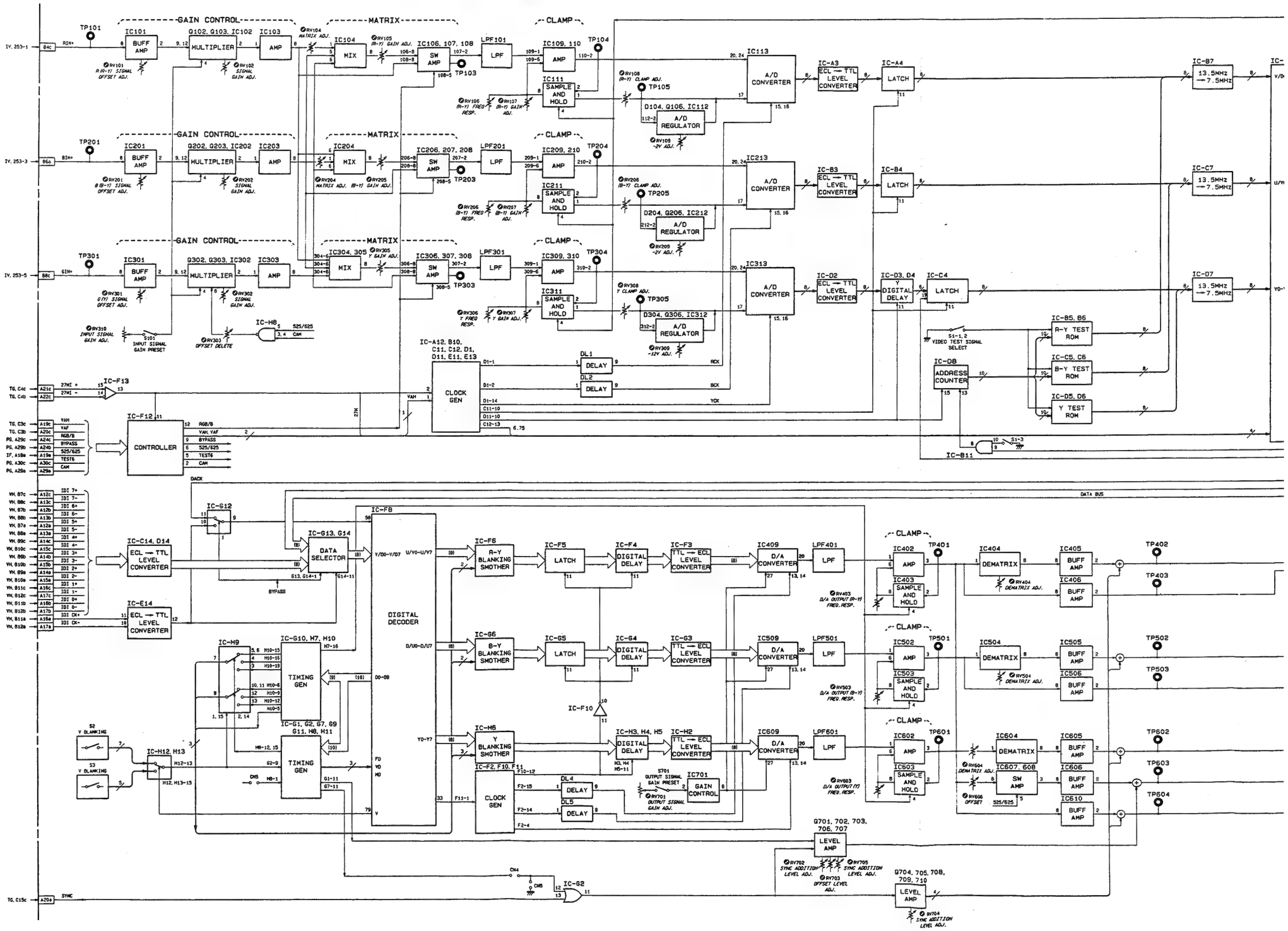



VA-45 BOARD BLOCK DIAGRAM
BOARD NO. 1-620-781-11, 12
DVPC-1000 (J) : #10001-21299
DVPC-1000 (U/C) : #10001-10999
DVPC-1000 (EK) : #10001-11099

## VA-45 BOARD

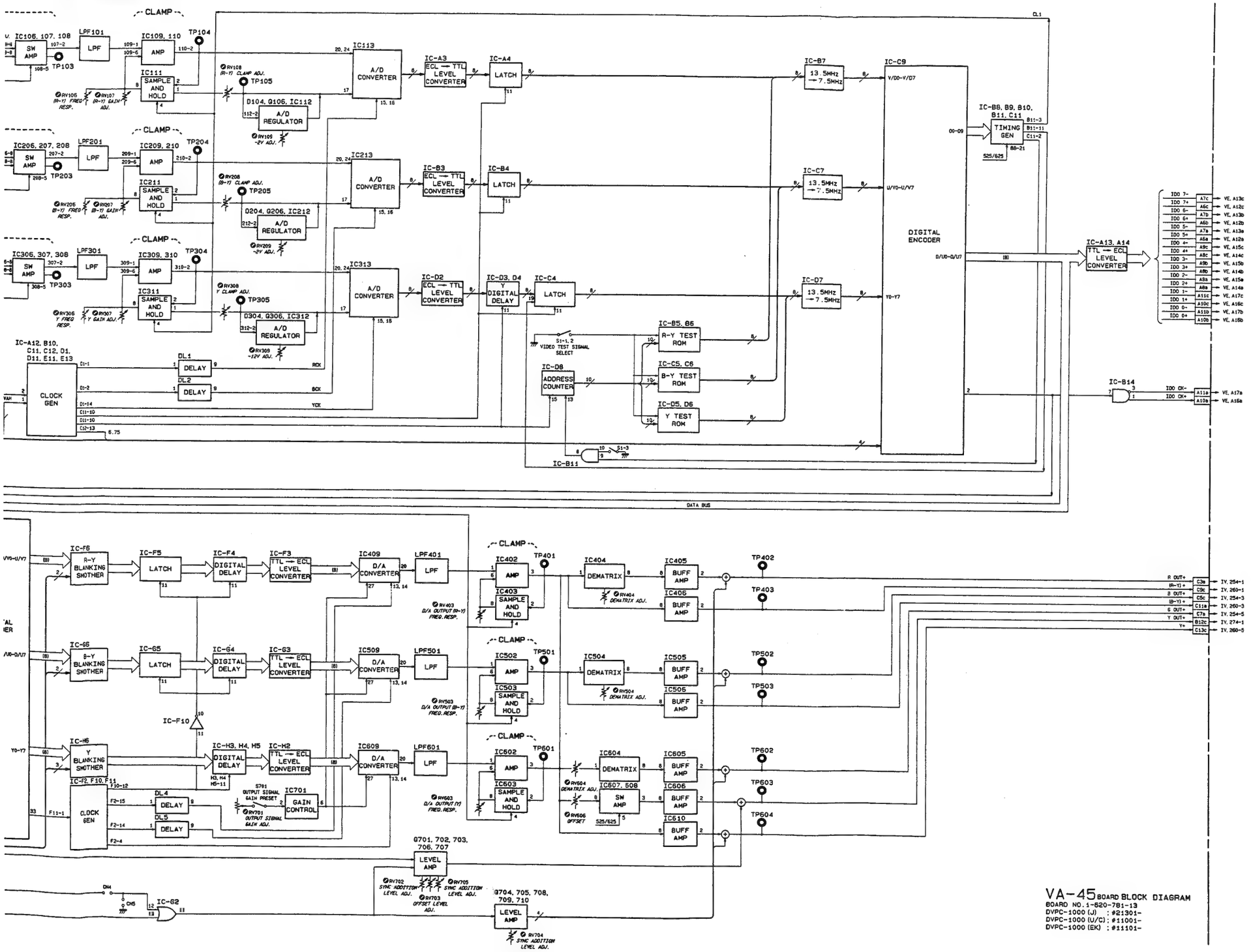
Video A/D, D/A Converter

| |
|---|
| #21301 & UP (J) |
| #11001 & UP (UC) |
| #11101 & UP (EK) |




A-9 (a)

A-10 (a)




VA-45 BOARD BLOCK DIAGRAM
BOARD NO.1-520-781-13
DVPC-1000 (J) : #21301-
DVPC-1000 (J/C) : #11001-
DVPC-1000 (EK) : #11101-

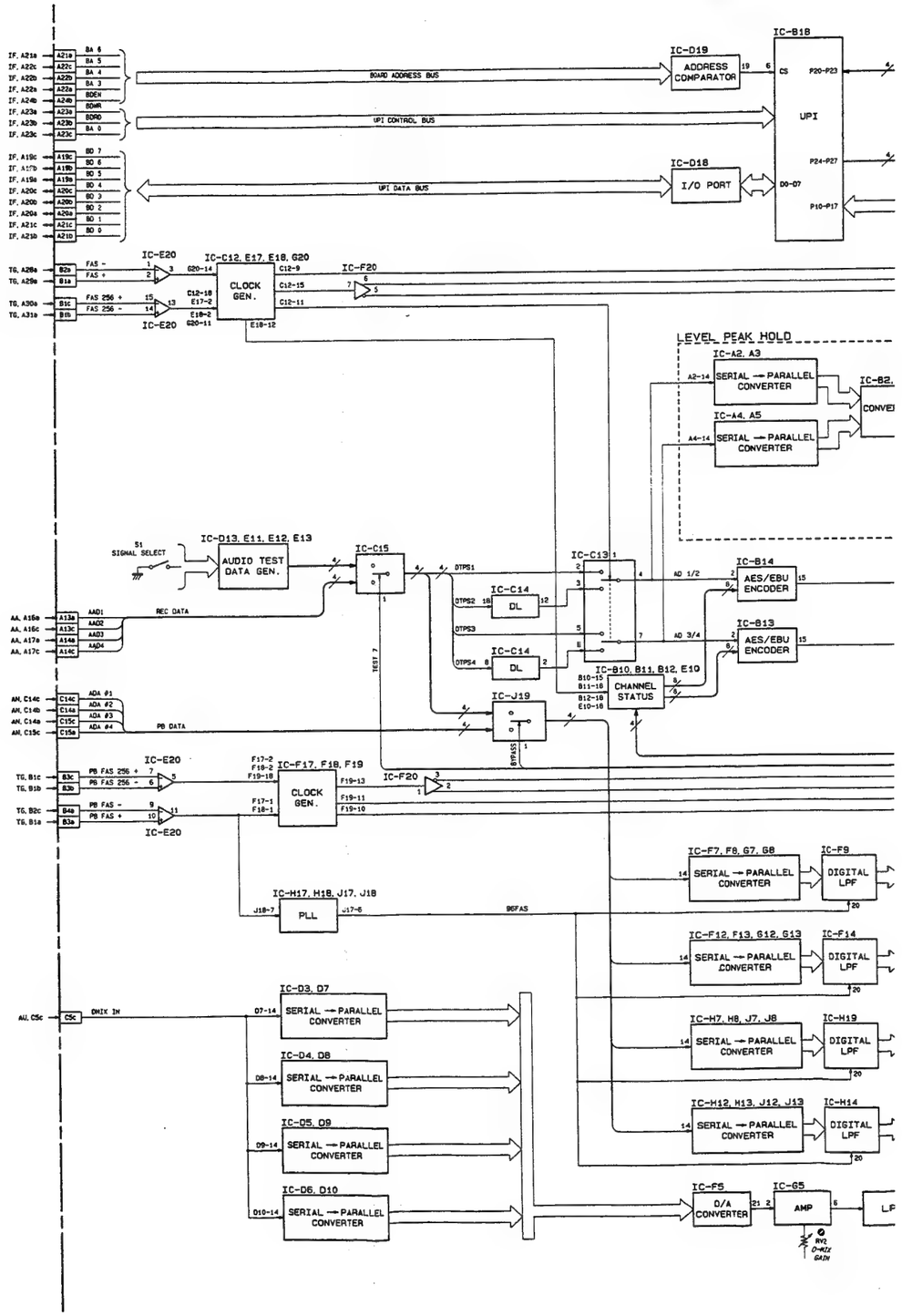
## PG-13 BOARD

Pulse Generator

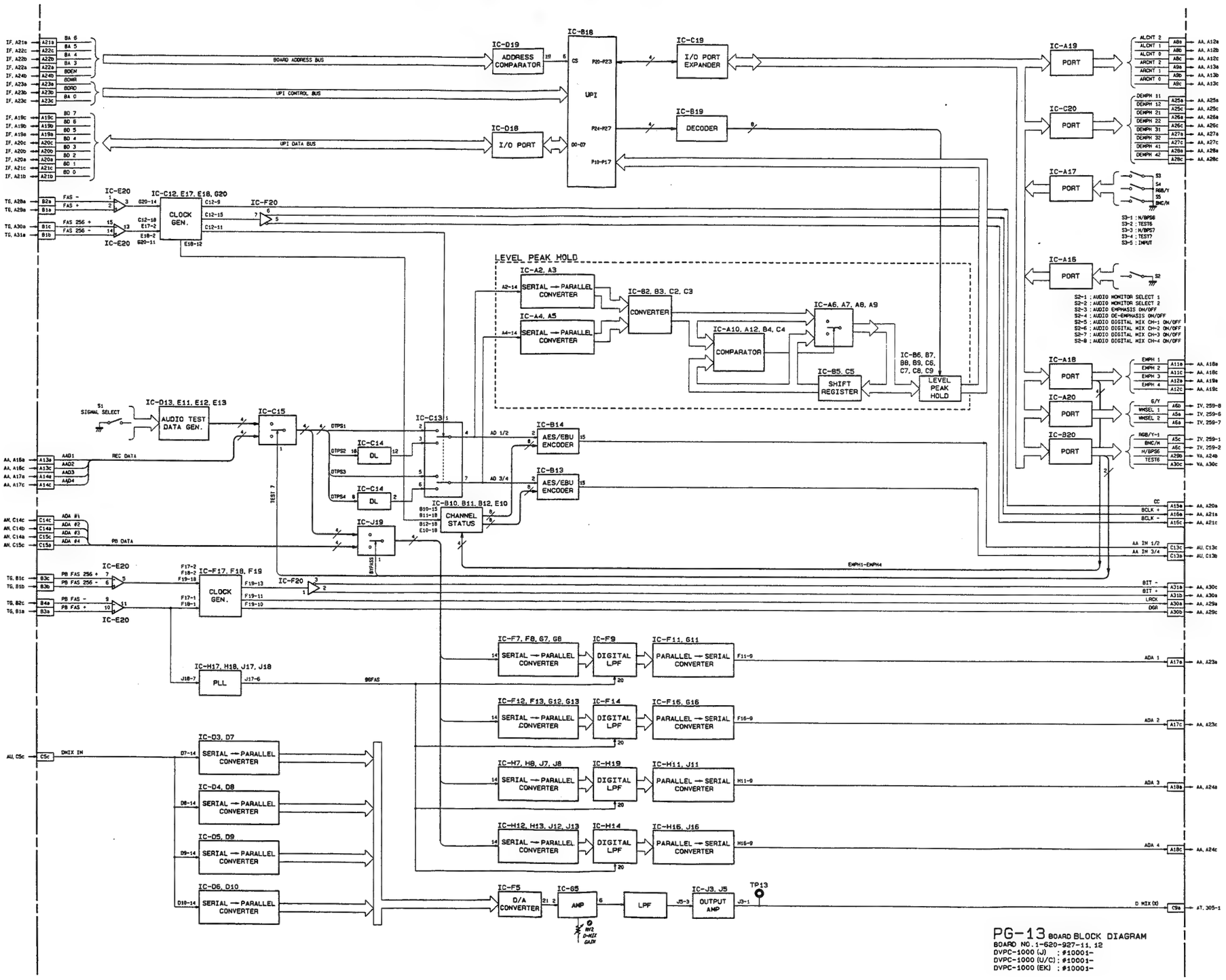




PG-13 BLOC

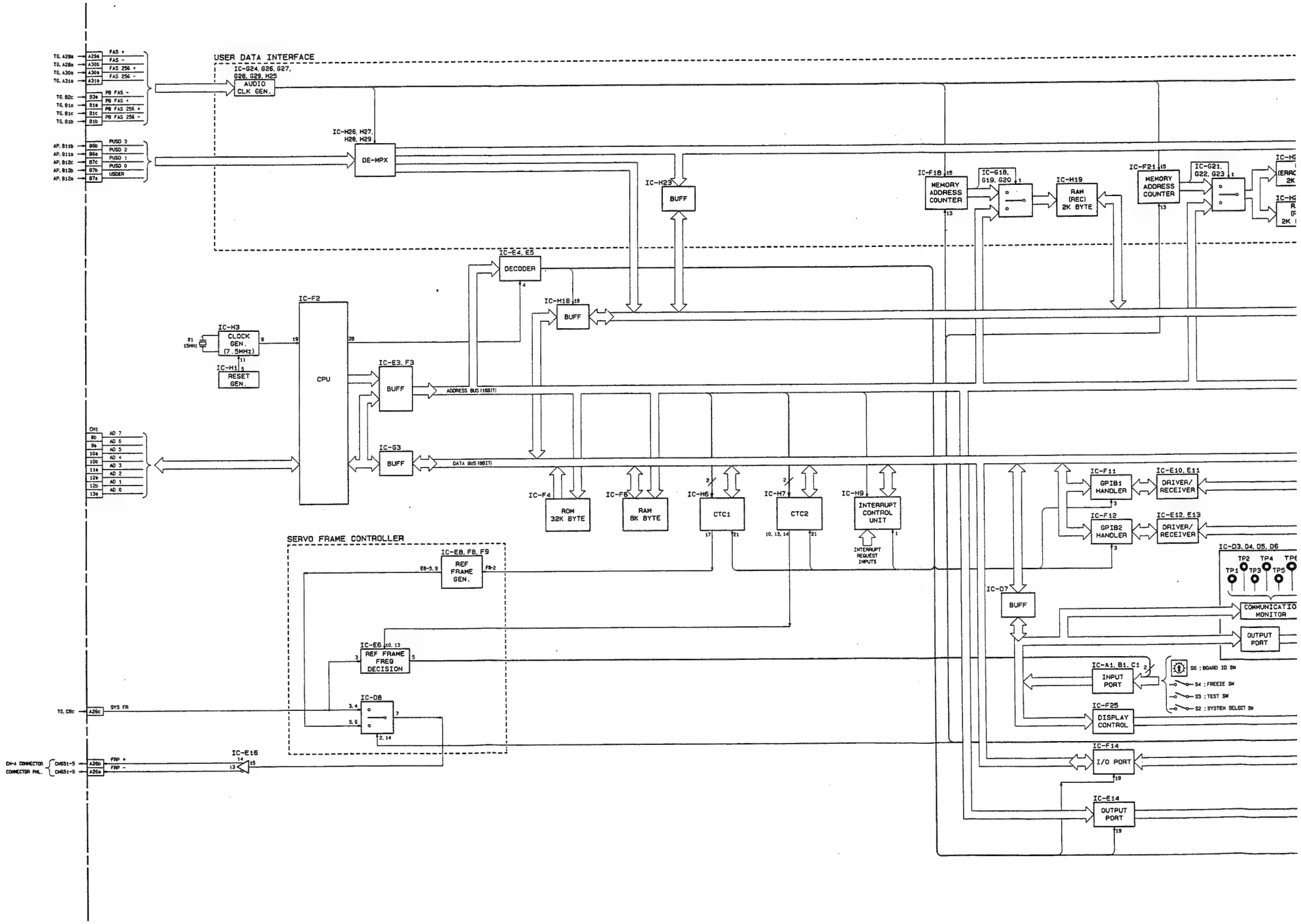


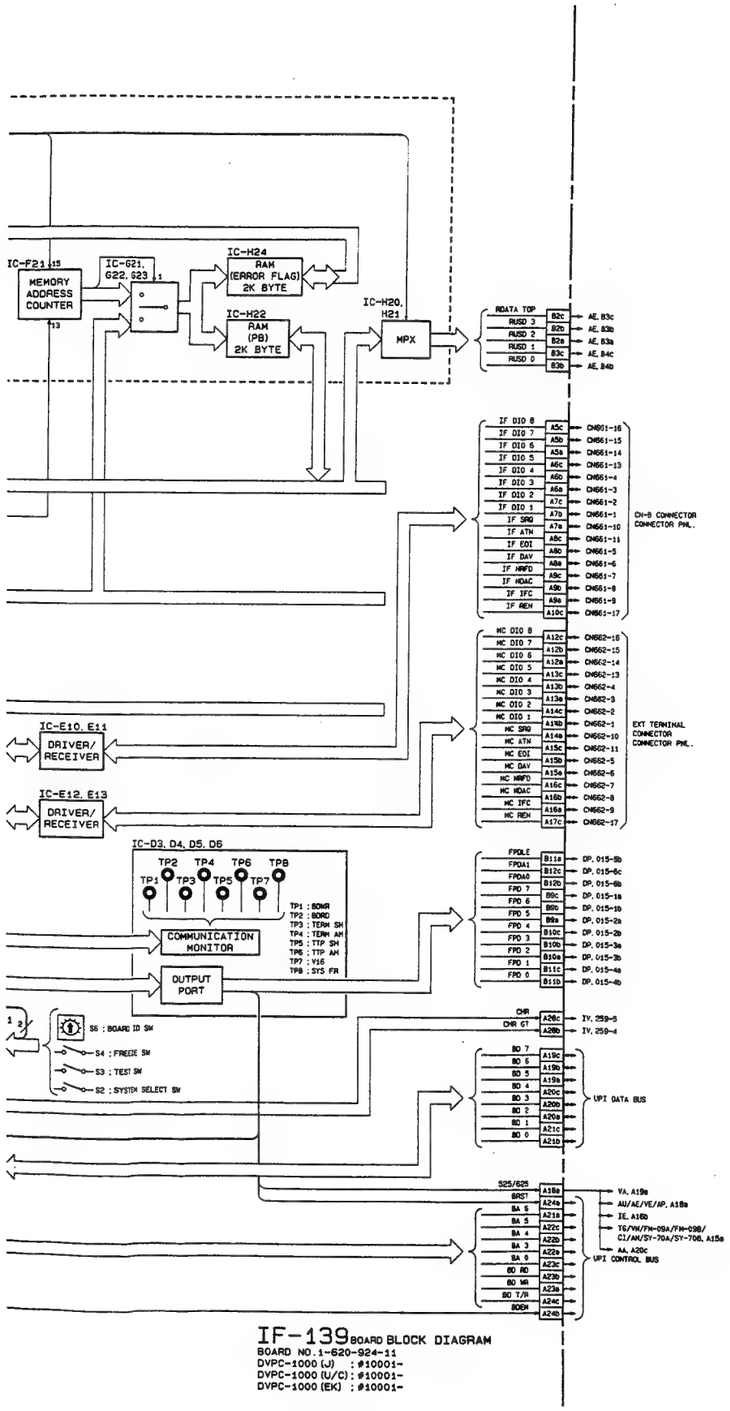
## PG-13 BOARD
Pulse Generator



## IF-139 BOARD

TTP Interface





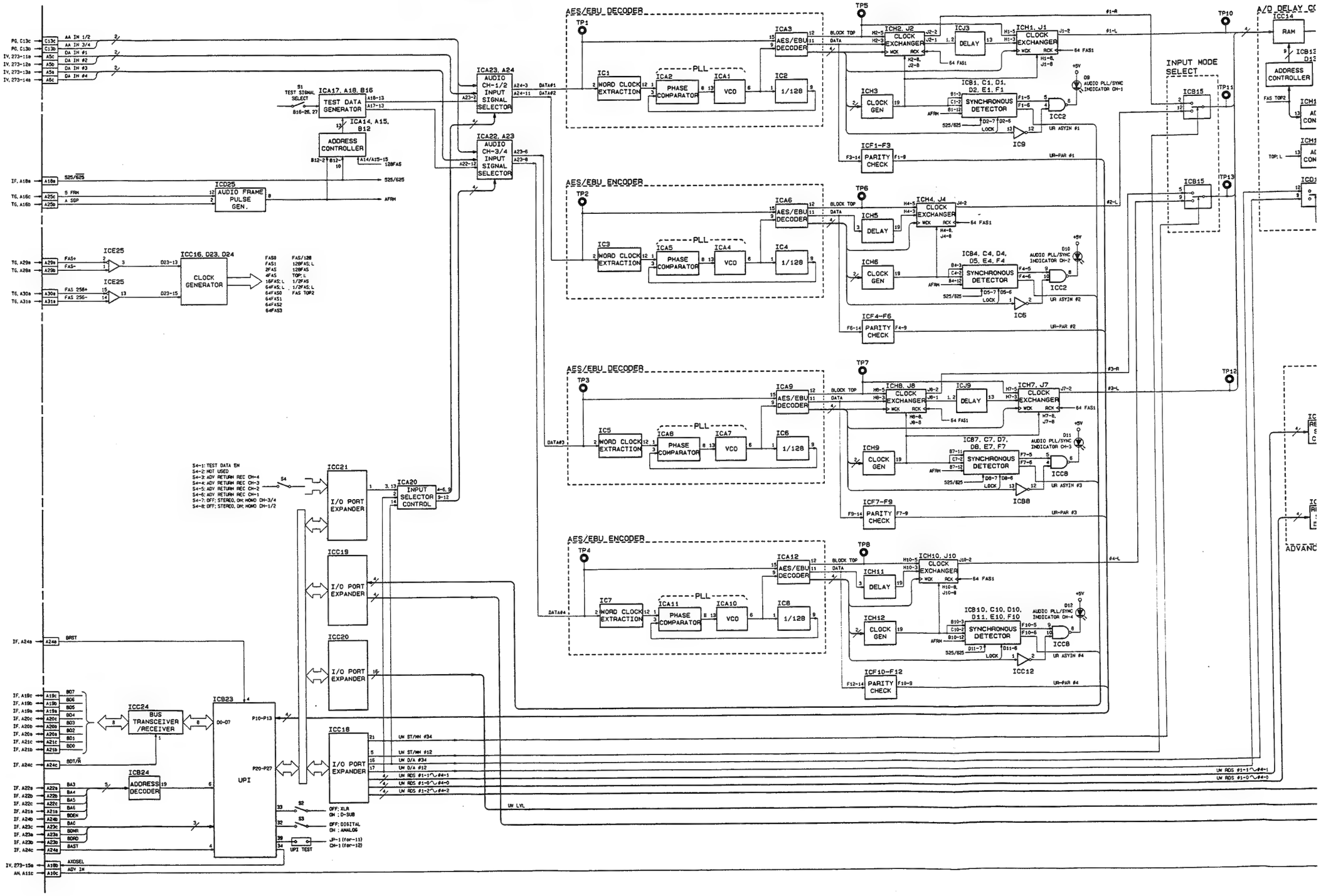

## IF-139 BOARD BLOCK DIAGRAM

BOARD NO.1-620-924-11
DVPC-1000 (J) : #10001-
DVPC-1000 (U/C) : #10001-
DVPC-1000 (EK) : #10001-

## AU-86 BOARD

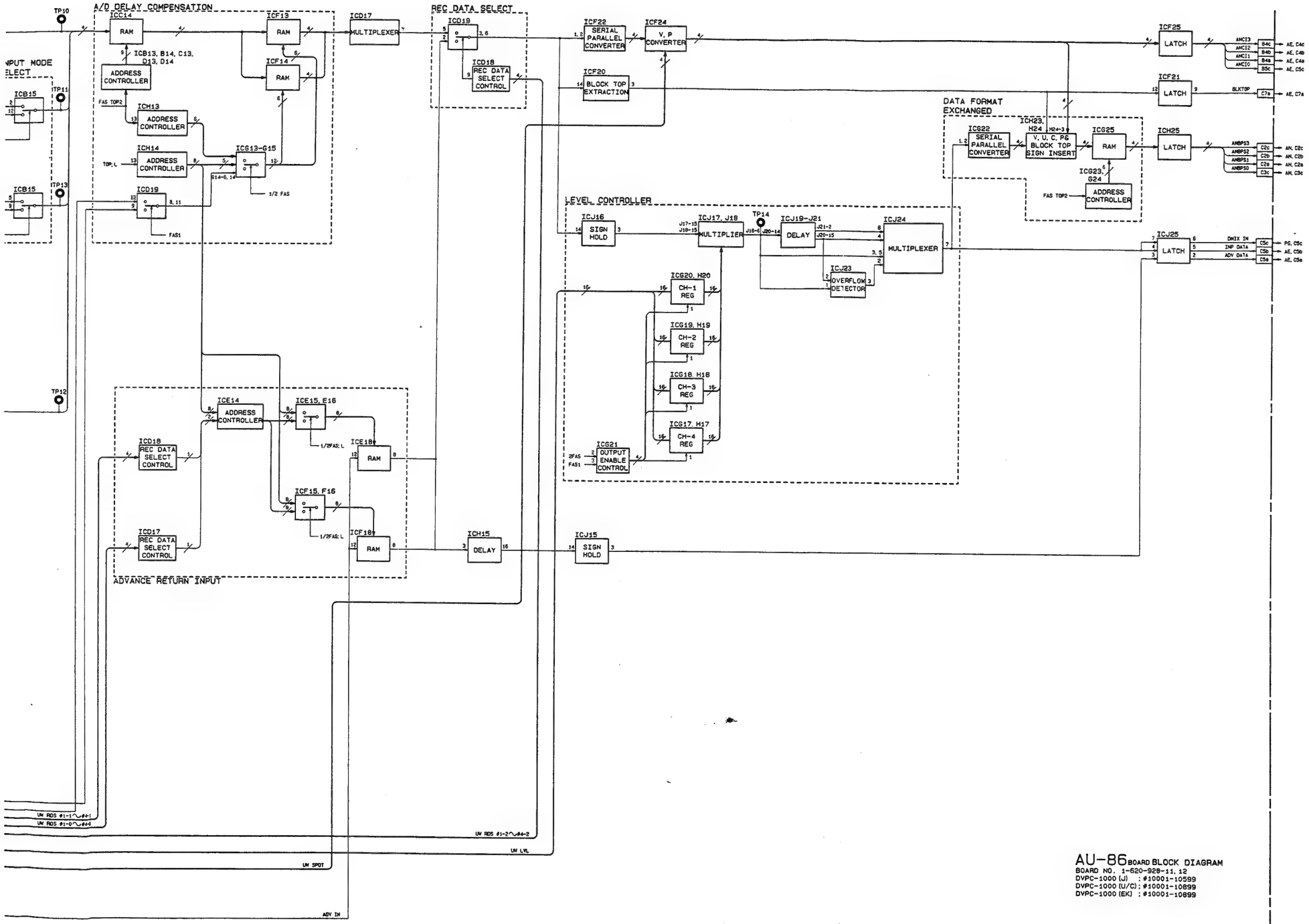
Audio Input

| |
|---|
| # 10001 TO 10599 (J) |
| # 10001 TO 10899 (UC) |
| # 10001 TO 10899 (EK) |




A-19 (a)

A-20 (a)

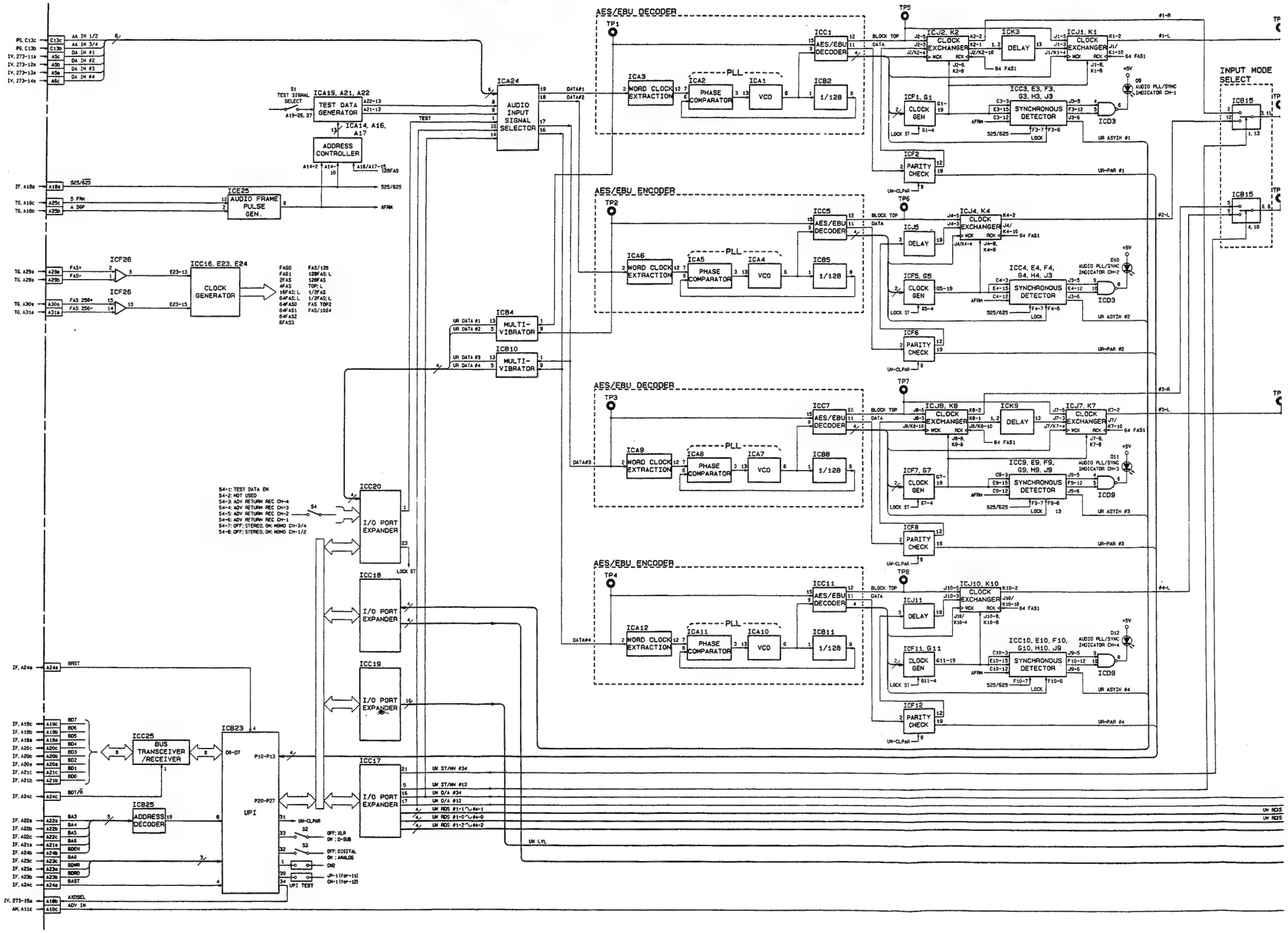



AU-86 BOARD BLOCK DIAGRAM
BOARD NO. 1-520-928-11, 12
DVPC-1000 (J) : #10001-10599
DVPC-1000 (U/C) : #10001-10899
DVPC-1000 (EK) : #10001-10899

## AU-86 BOARD

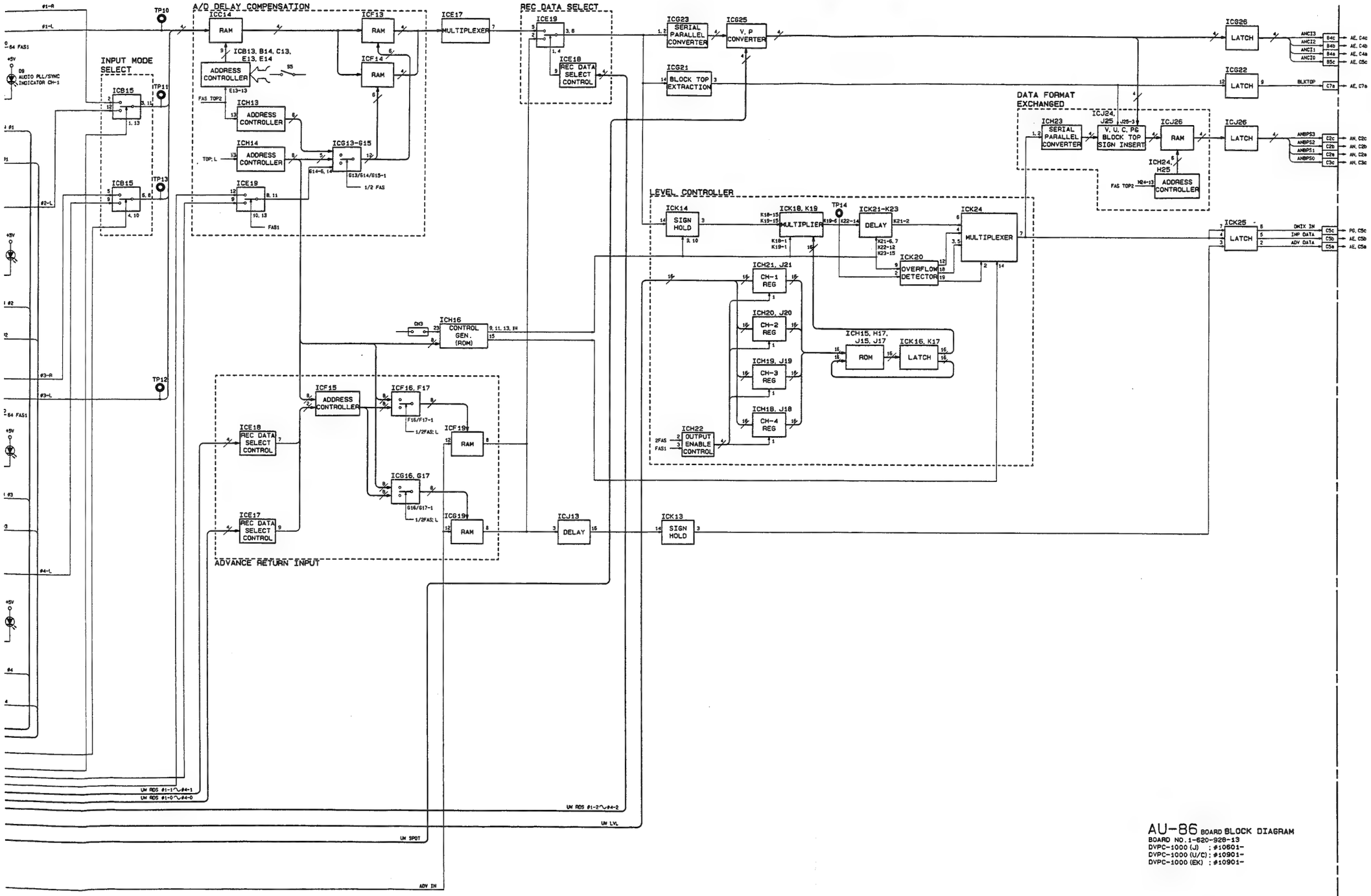
Audio Input

| |
|---|
| # 10601 & UP (J) |
| # 10901 & UP (UC) |
| # 10901 & UP (EK) |




A-19 (b)

A-20 (b)

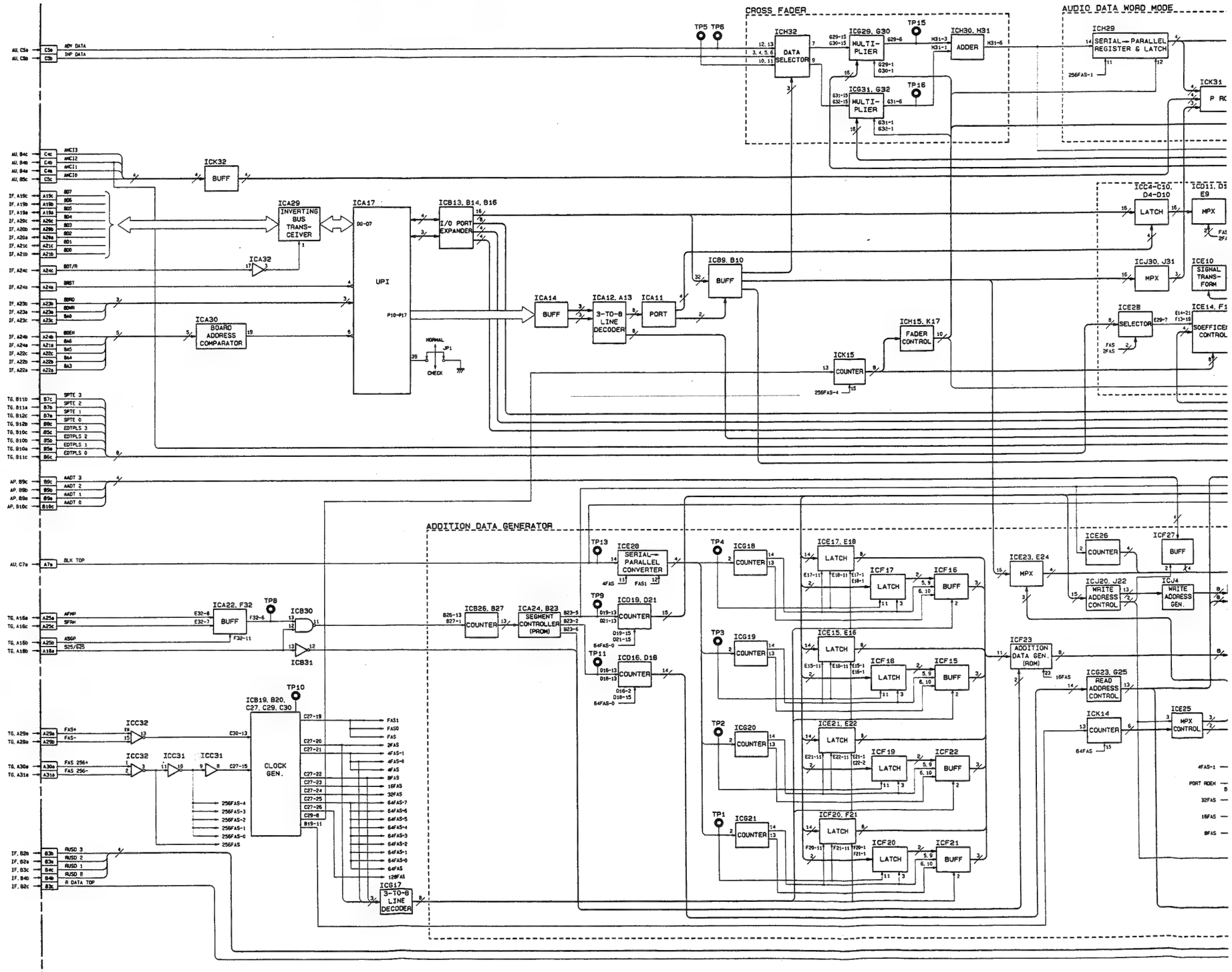


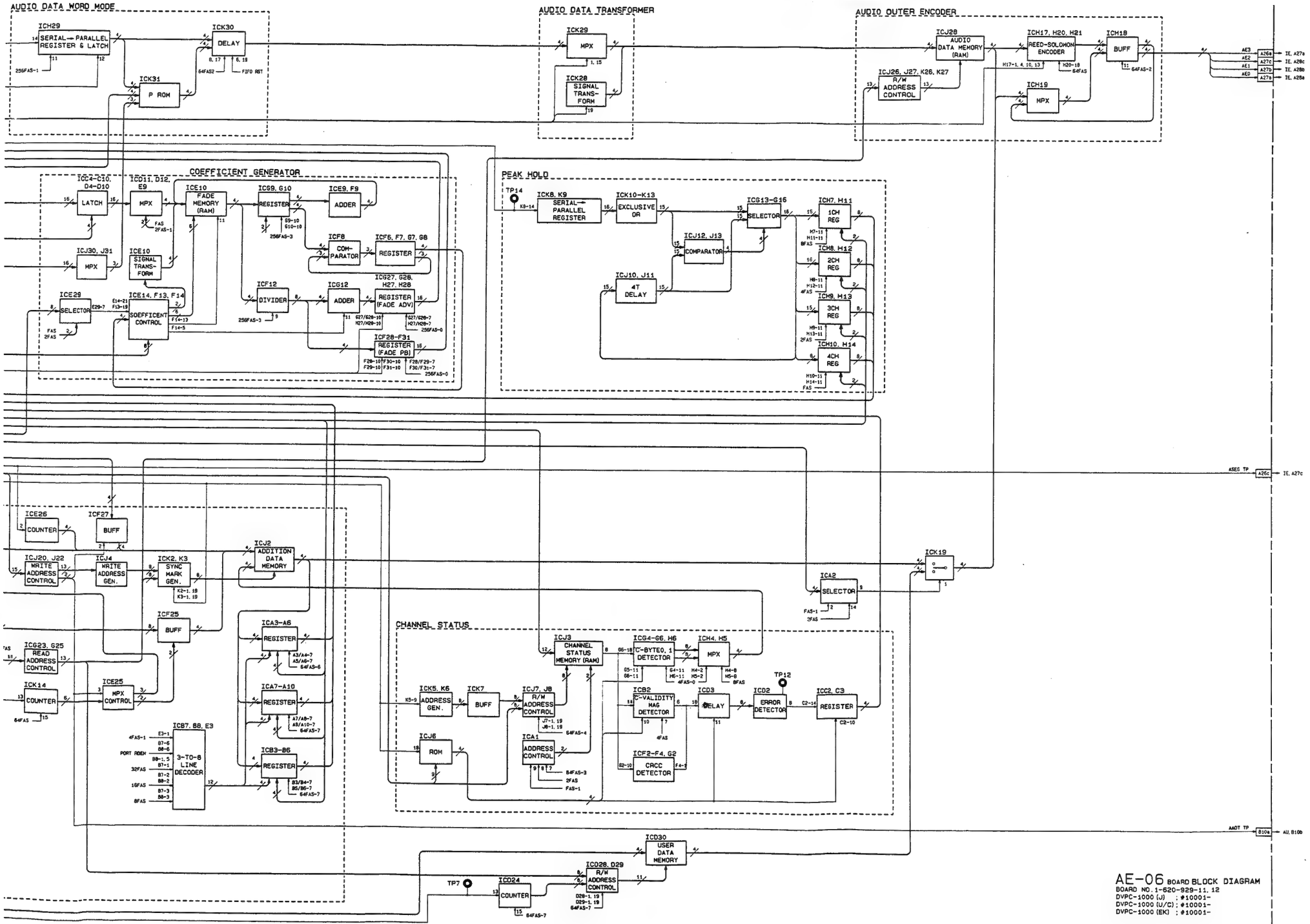

AU-86 BOARD BLOCK DIAGRAM
BOARD NO. 1-520-928-13
DVPC-1000 (J) : #10601-
DVPC-1000 (U/C) : #10901-
DVPC-1000 (EK) : #10901-

## AE-06 BOARD

Audio Outer Encoder

BLOCK DIAGRAM **AE-06** [redacted] **AE-06** BLOCK DIAGRAM

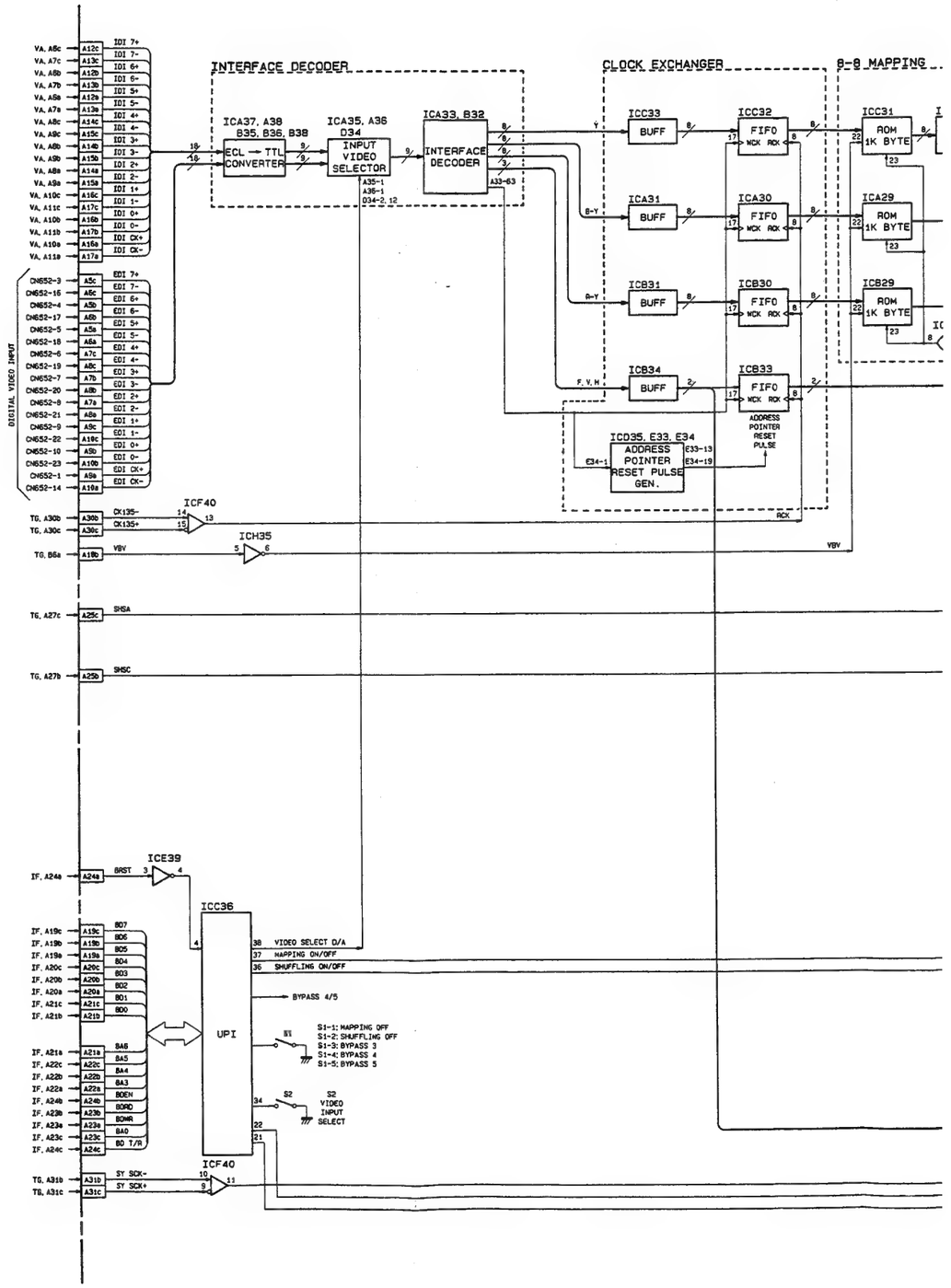


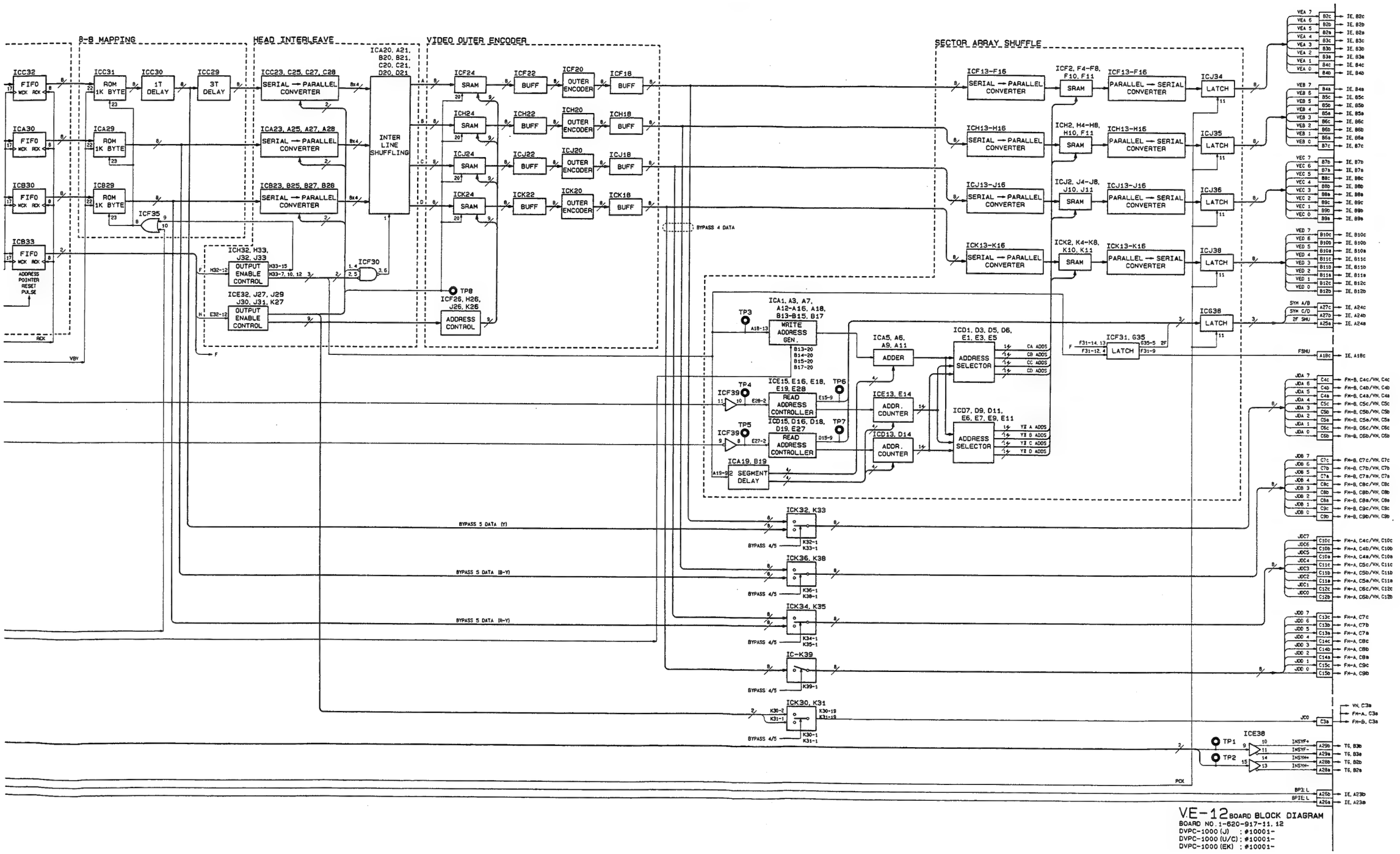



AE-06 BOARD BLOCK DIAGRAM
BOARD NO. 1-520-929-11, 12
DVPC-1000 (J) : #10001-
DVPC-1000 (U/C) : #10001-
DVPC-1000 (EK) : #10001-

## VE-12 BOARD

Video Outer Encoder



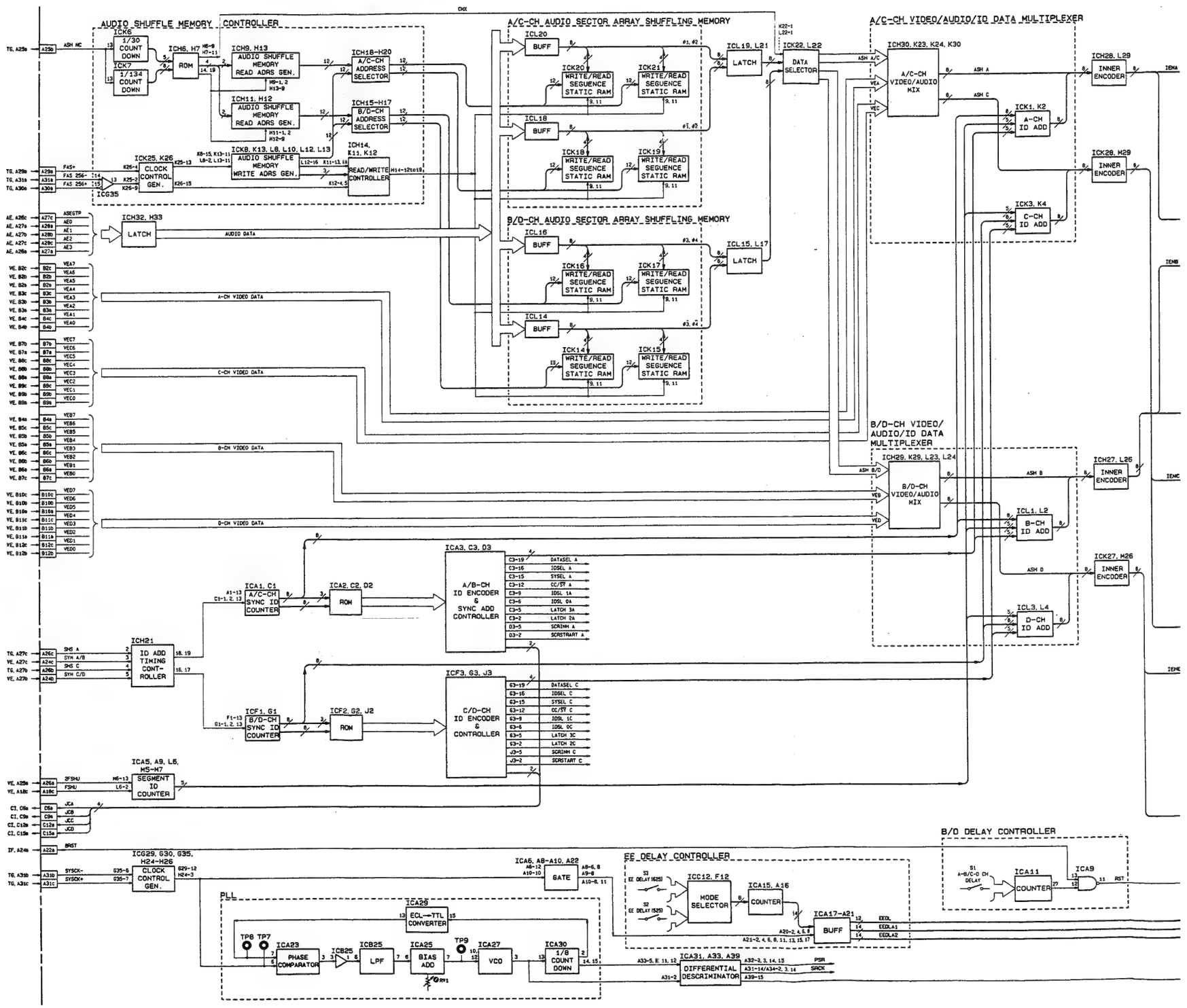



VE-12 BOARD BLOCK DIAGRAM
BOARD NO. 1-620-917-11, 12
DVPC-1000 (J) : #10001-
DVPC-1000 (U/C) : #10001-
DVPC-1000 (EK) : #10001-

## IE-17 BOARD

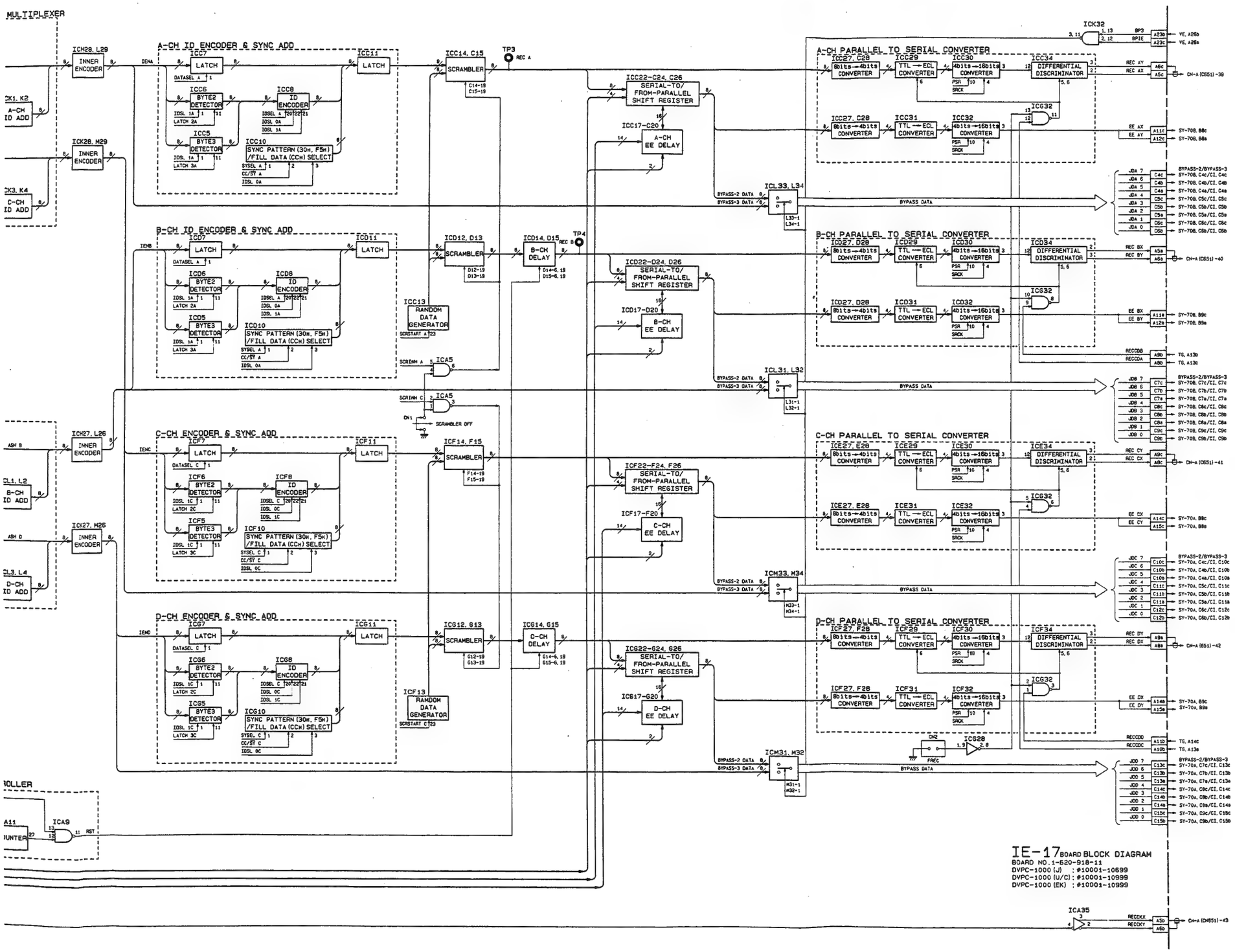
Inner Encoder

| |
|---|
| # 10001 TO 10699 (J) |
| # 10001 TO 10999 (UC) |
| # 10001 TO 10999 (EK) |




A-31 (a)

A-32 (a)


MULTIPLEXER
ICH28, L29
INNER ENCODER
A-CH ID ENCODER & SYNC ADD
ICC7 LATCH
ICC11 LATCH
ICC6 BYTE2 DETECTOR
ICC8 ID ENCODER
ICC5 BYTE3 DETECTOR
ICC10 SYNC PATTERN (30H, F5H) /FILL DATA (CCH) SELECT
ICC14, C15 SCRAMBLER
TP3 REC A
ICC22-C24, C26 SERIAL-TO/FROM-PARALLEL SHIFT REGISTER
ICC17-C20 A-CH EE DELAY
ICL33, L34
BYPASS-2 DATA
BYPASS-3 DATA
BYPASS DATA
A-CH PARALLEL TO SERIAL CONVERTER
ICC27, C28 8bits→4bits CONVERTER
ICC29 TTL→ECL CONVERTER
ICC30 4bits→16bits CONVERTER
ICC34 DIFFERENTIAL DISCRIMINATOR
ICC31 TTL→ECL CONVERTER
ICC32 4bits→16bits CONVERTER
ICG32
ICK32
REC AY
REC AX
EE AX
EE AY
CN-A (CB51)-39
SY-70B, B8c
SY-70B, B8a
B-CH ID ENCODER & SYNC ADD
ICD7 LATCH
ICD11 LATCH
ICD6 BYTE2 DETECTOR
ICD8 ID ENCODER
ICD5 BYTE3 DETECTOR
ICD10 SYNC PATTERN (30H, F5H) /FILL DATA (CCH) SELECT
ICD12, D13 SCRAMBLER
ICD14, D15 B-CH DELAY
TP4 REC B
ICD22-D24, D26 SERIAL-TO/FROM-PARALLEL SHIFT REGISTER
ICD17-D20 B-CH EE DELAY
ICL31, L32
B-CH PARALLEL TO SERIAL CONVERTER
REC BX
REC BY
EE BX
EE BY
CN-A (CB51)-40
SY-70B, B9c
SY-70B, B9a
ICC13 RANDOM DATA GENERATOR
SCRSTART A
SCRINH A
ICA5
SCRINH C
CN1
SCRAMBLER OFF
C-CH ENCODER & SYNC ADD
ICF7 LATCH
ICF11 LATCH
ICF6 BYTE2 DETECTOR
ICF8 ID ENCODER
ICF5 BYTE3 DETECTOR
ICF10 SYNC PATTERN (30H, F5H) /FILL DATA (CCH) SELECT
ICF14, F15 SCRAMBLER
ICF22-F24, F26 SERIAL-TO/FROM-PARALLEL SHIFT REGISTER
ICF17-F20 C-CH EE DELAY
ICM33, M34
C-CH PARALLEL TO SERIAL CONVERTER
REC CY
REC CX
EE CX
EE CY
CN-A (CB51)-41
SY-70A, B8c
SY-70A, B8a
D-CH ENCODER & SYNC ADD
ICG7 LATCH
ICG11 LATCH
ICG6 BYTE2 DETECTOR
ICG8 ID ENCODER
ICG5 BYTE3 DETECTOR
ICG10 SYNC PATTERN (30H, F5H) /FILL DATA (CCH) SELECT
ICG12, G13 SCRAMBLER
ICG14, G15 D-CH DELAY
ICF13 RANDOM DATA GENERATOR
SCRSTART C
ICG22-G24, G26 SERIAL-TO/FROM-PARALLEL SHIFT REGISTER
ICG17-G20 D-CH EE DELAY
ICM31, M32
D-CH PARALLEL TO SERIAL CONVERTER
REC DY
REC DX
EE DX
EE DY
CN-A (B51)-42
SY-70A, B9c
SY-70A, B9a
ICG28
CN2
FREQ
CONTROLLER
ICA9
RST
ICA35
RECCKX
RECCKY
CN-A (CN51)-43
IE-17 BOARD BLOCK DIAGRAM
BOARD NO.:1-620-918-11
DVPC-1000 (J) : #10001-10699
DVPC-1000 (U/C) : #10001-10999
DVPC-1000 (EK) : #10001-10999

A-33 (a)

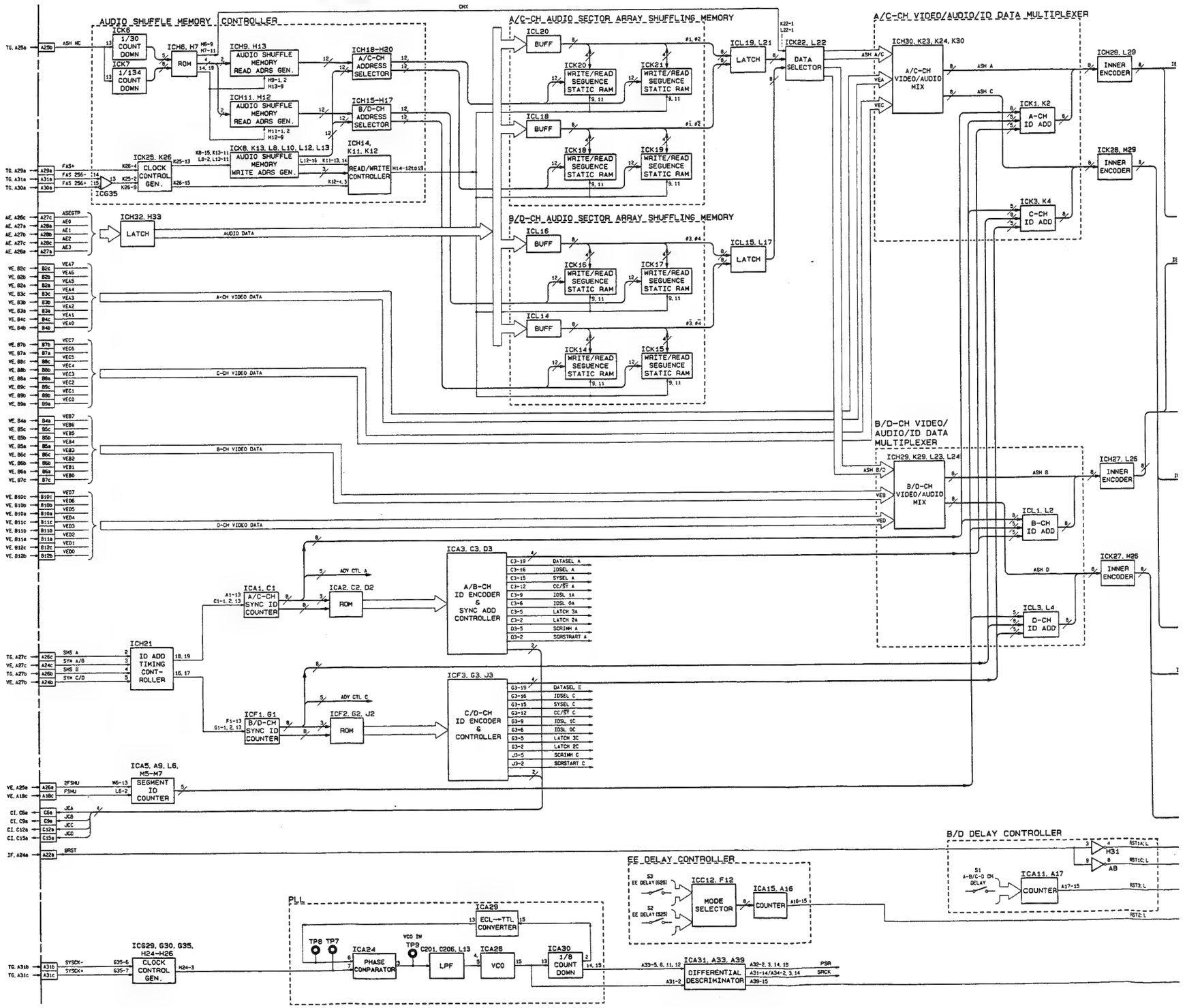
A-34 (a)

## IE-17 BOARD

Inner Encoder

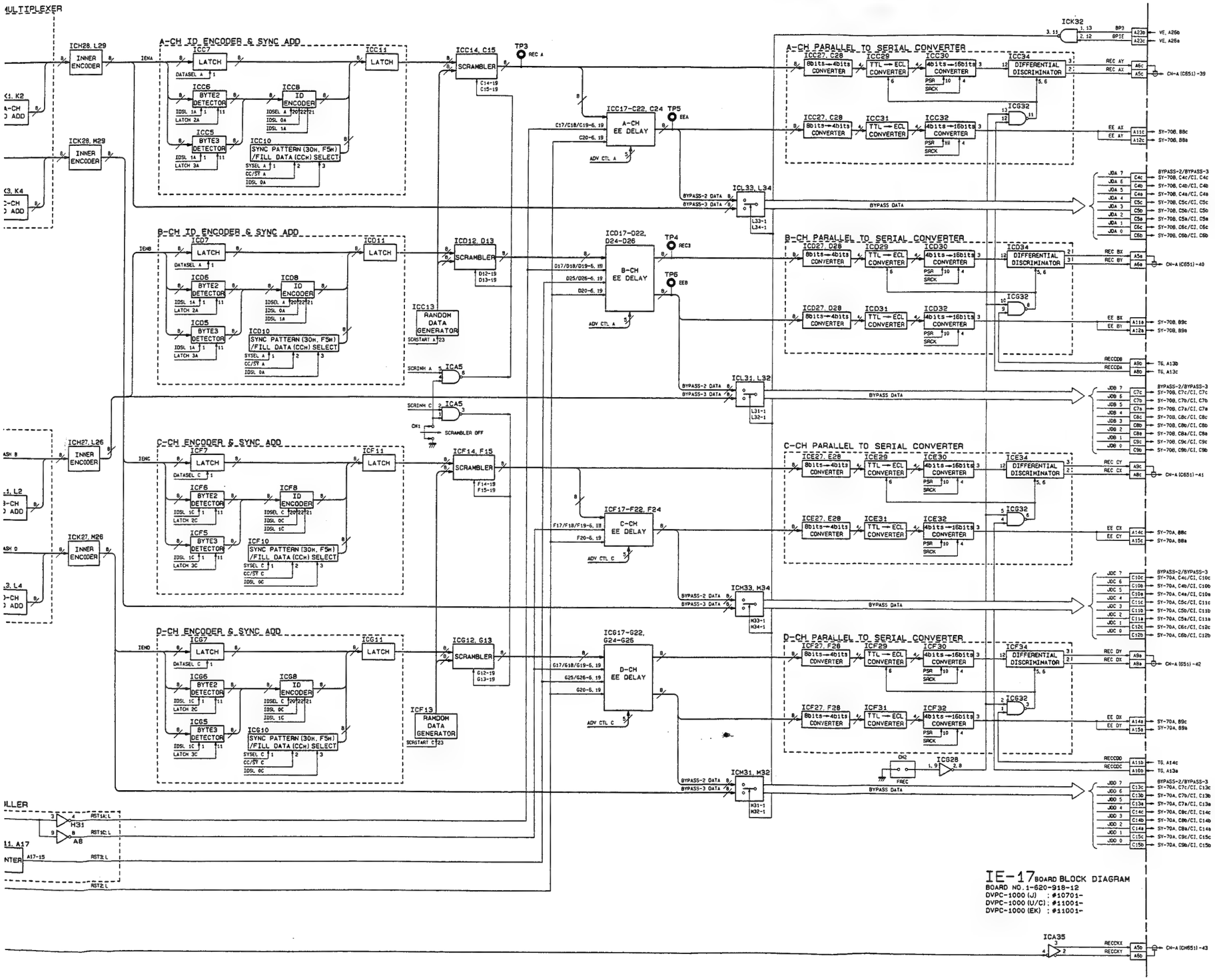
| |
|---|
| # 10701 & UP (J) |
| # 11001 & UP (UC) |
| # 11001 & UP (EK) |

# BLOCK DIAGRAM IE-17 [redacted] IE-17 BLOCK DIAGRAM




A-31 (b)

A-32 (b)


A-CH ID ENCODER & SYNC ADD
B-CH ID ENCODER & SYNC ADD
C-CH ENCODER & SYNC ADD
D-CH ENCODER & SYNC ADD
A-CH PARALLEL TO SERIAL CONVERTER
B-CH PARALLEL TO SERIAL CONVERTER
C-CH PARALLEL TO SERIAL CONVERTER
D-CH PARALLEL TO SERIAL CONVERTER
INNER ENCODER
LATCH
BYTE2 DETECTOR
BYTE3 DETECTOR
ID ENCODER
SYNC PATTERN (30H, F5H) /FILL DATA (CCH) SELECT
SCRAMBLER
A-CH EE DELAY
B-CH EE DELAY
C-CH EE DELAY
D-CH EE DELAY
RANDOM DATA GENERATOR
8bits→4bits CONVERTER
TTL→ECL CONVERTER
4bits→16bits CONVERTER
DIFFERENTIAL DISCRIMINATOR
BYPASS DATA
SCRAMBLER OFF
IE-17 BOARD BLOCK DIAGRAM
BOARD NO.1-620-918-12
DVPC-1000 (J) : #10701-
DVPC-1000 (U/C) : #11001-
DVPC-1000 (EK) : #11001-

A-33 (b)

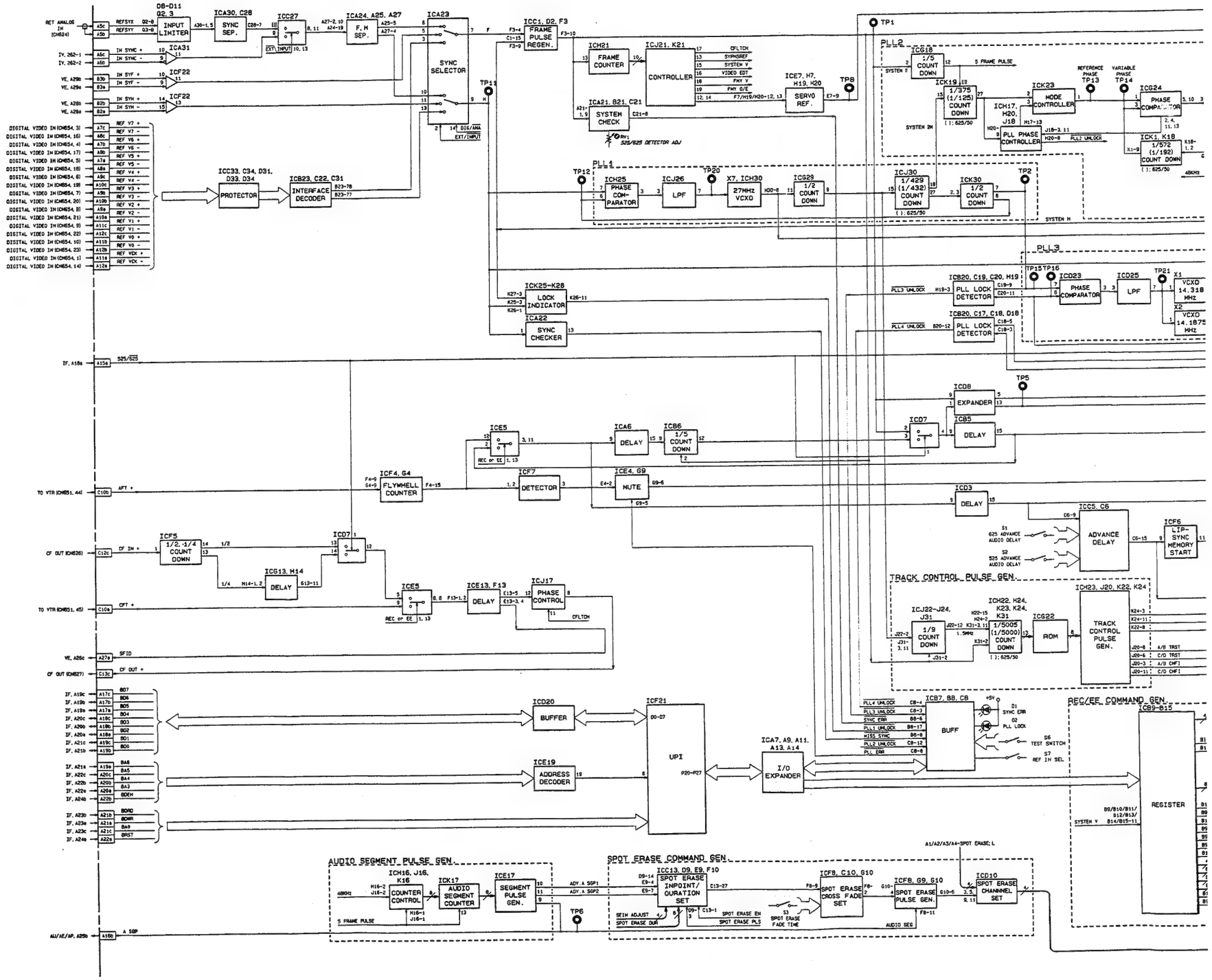
A-34 (b)

## TG-28 BOARD

Timing Controller

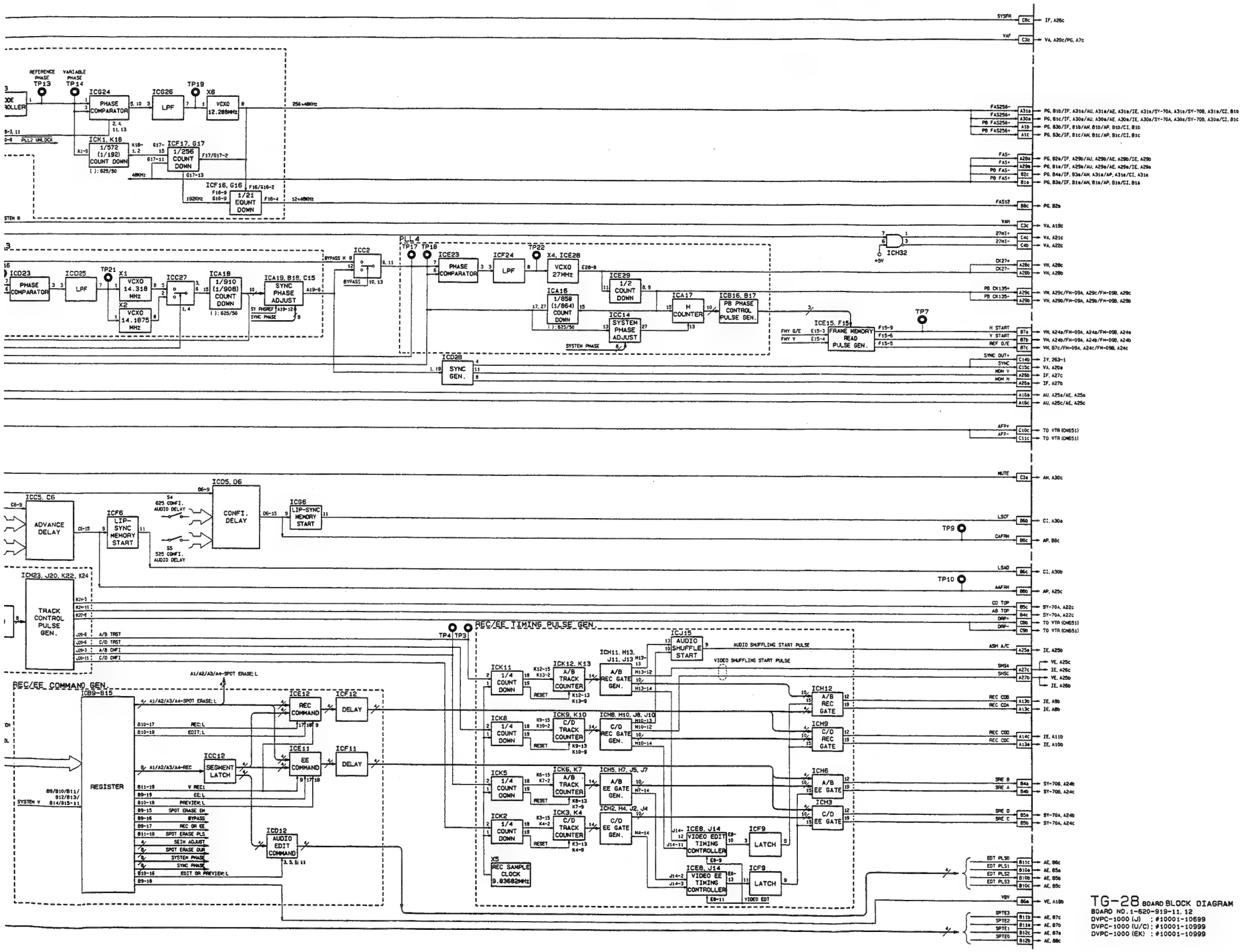
| |
|---|
| # 10001 TO 10699 (J) |
| # 10001 TO 10999 (UC) |
| # 10001 TO 10999 (EK) |

BLOCK DIAGRAM **TG-28** [redacted] **TG-28** BLOCK DIAGRAM




A-35 (a)

A-36 (a)







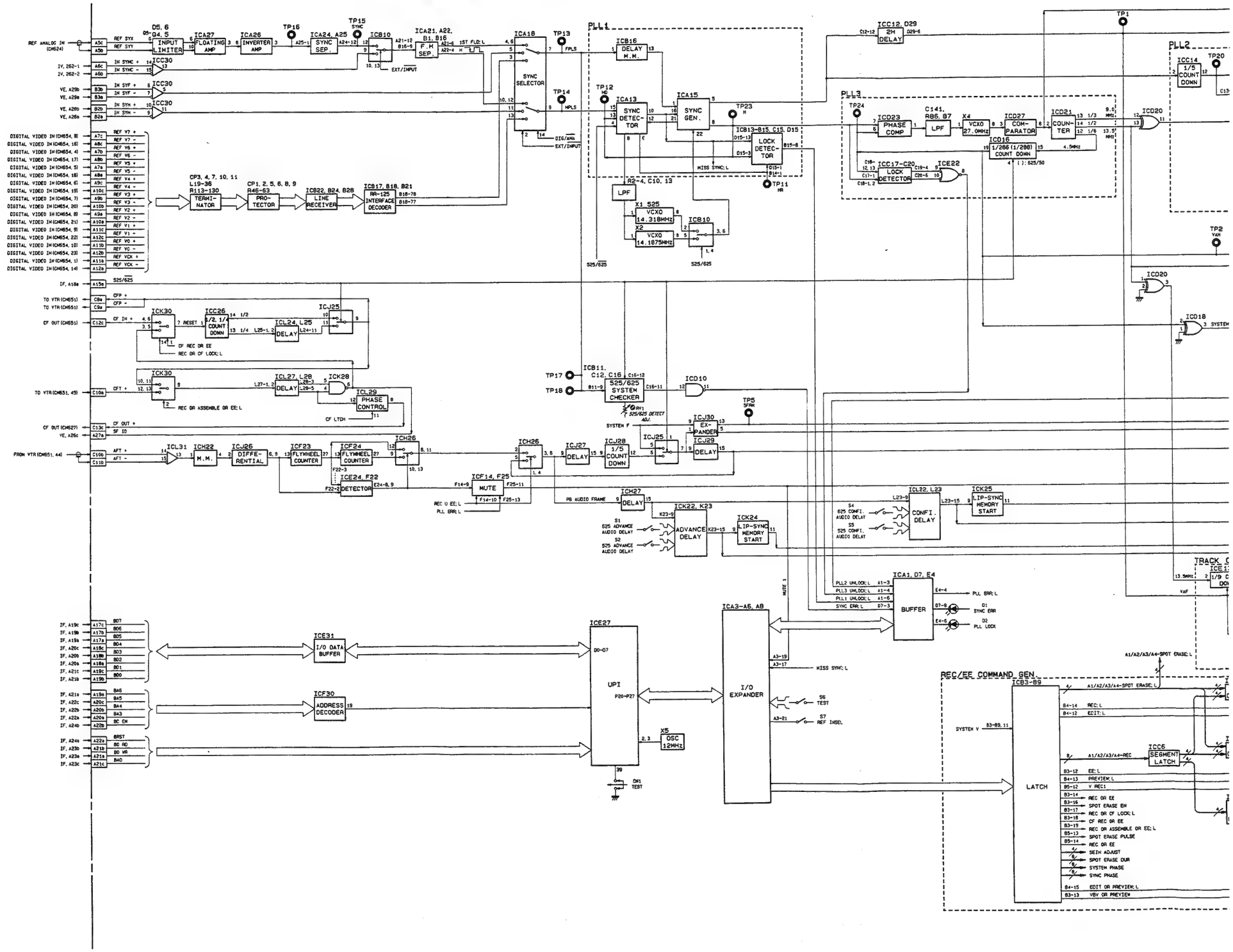
A-37 (a)

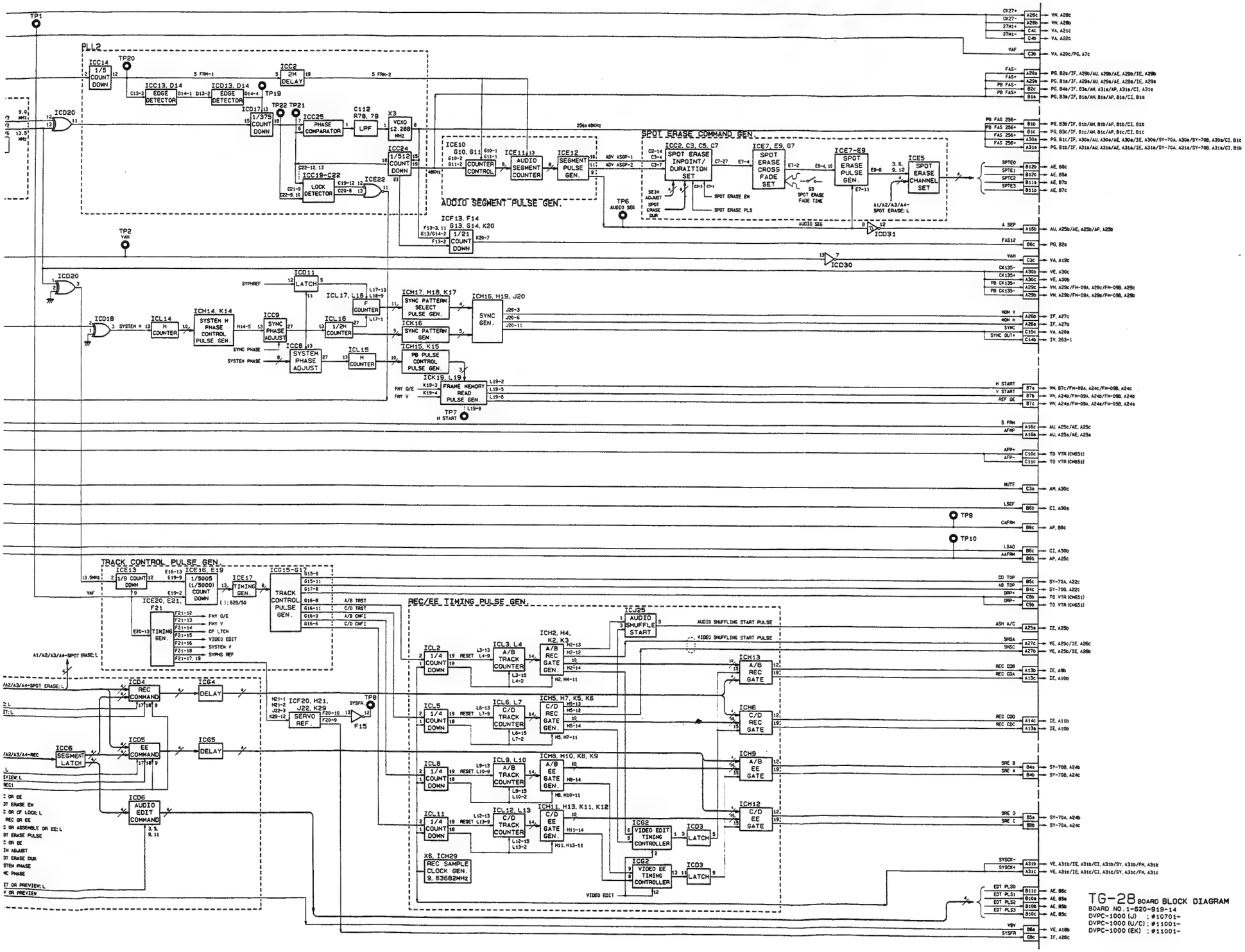
A-38 (a)

TG-28 BOARD BLOCK DIAGRAM
BOARD NO. 1-620-919-11, 12
DVPC-1000 (J) : #10001-10699
DVPC-1000 (U/C) : #10001-10999
DVPC-1000 (EK) : #10001-10999

**TG-28 BOARD**
Timing Controller

| |
|---|
| # 10701 & UP (J) |
| # 11001 & UP (UC) |
| # 11001 & UP (EK) |





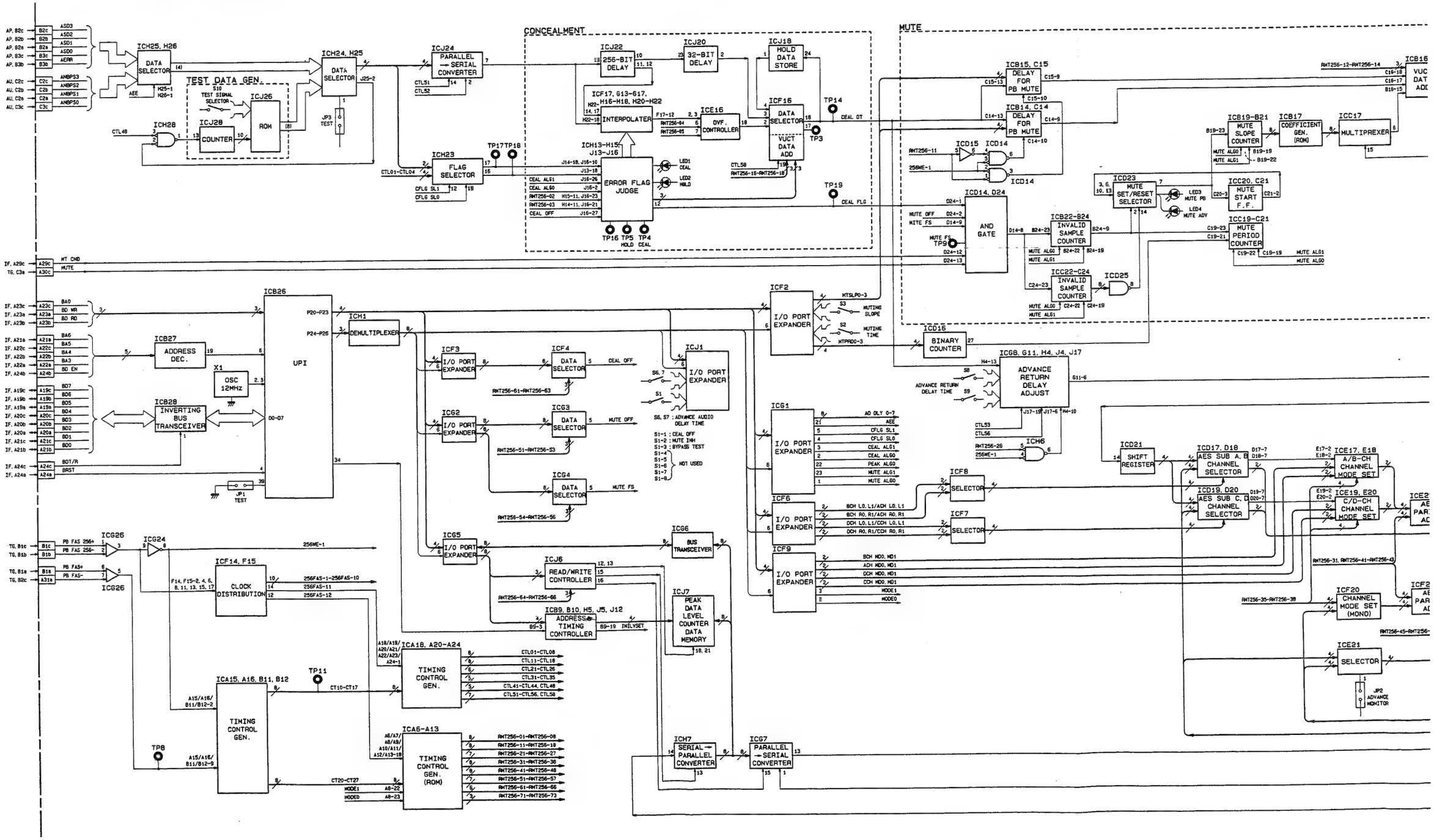

TG-28 BOARD BLOCK DIAGRAM
BOARD NO.1-520-919-14
DVPC-1000 (J) : #10701-
DVPC-1000 (U/C) : #11001-
DVPC-1000 (EK) : #11001-

A-37 (b)

A-38 (b)

## AN-01 BOARD
Audio Concealment

| |
|---|
| # 10001 TO 10699 (J) |
| # 10001 TO 10999 (UC) |
| # 10001 TO 10999 (EK) |




A-39 (a)

A-40 (a)

LEVEL CONTROLLER

COEFFICIENT REGISTER & DELAY

PEAK LEVEL DETECTOR

CRC GENERATOR

CRC OPERATOR

AES BLOCK COUNTER&CH-ST CONVERTER

TIME AXIS CONVERTER

ICB16, C16 VUCT DATA ADD

ICC17 MULTIPREXER

ICH2, J2 ADVANCE DELAY ADJUST

ICJ20 LATCH

ICH5

ICH8 MSB HOLD

ICH9, J9 MULTIPLIER FOR ADV (GAIN ADJ)

ICH10, J10 MULTIPLIER FOR CONFI. (GAIN ADJ)

ICG9, G10 VUCT ADD & OVER FLOW/ UNDER FLOW CONTROLLER

ICH8, J8 16BIT SHIFT REGISTER

ICJ21 232 BIT DELAY

TP15

TP20

TP7

ICC5, C6 AES START & CH-ST DETECTOR

ICJ20 DELAY

ICD7 LATCH

ICD8 PARALLEL →SERIAL CONVERTER

ICB2 CRC DATA PARALLEL →SERIAL CONVERTER

ICC7 SELECTOR

ICD3 ROM

ICD5, D6 AES 192 SAMPLE COUNTER

ICD2 ROM

ICC1, D1

ICA2, C2, C3 CRC GEN.

TP12

TP13

ICG12 SERIAL → PARALLEL CONVERTER

ICH12 DELAY

ICJ12 SELECTOR / MAGNETUDE COMPARATOR

ICJ11 ADDER & SUBTRACTOR

ICH11 SERIAL → PARALLEL CONVERTER

ICH12 DELAY

ICJ21 DELAY

ICE11, F11 SELECTOR

ICD12, E12 DELAY

ICE13, F13 SELECTOR

ICE10, F10 SELECTOR

ICD10, F12 DELAY

ICE17, E18 A/B-CH CHANNEL MODE SET

ICE19, E20 C/D-CH CHANNEL MODE SET

ICE22 AES PARITY ADD

ICE23 AES ENCODER

ICE24-E27, F25, F26 DELAY ADJUST

ICE27 LATCH

ICF20 CHANNEL MODE SET (MONO)

ICF21 AES PARITY ADD

ICF22 AES ENCODER

ICD22 LATCH

ICE21 SELECTOR

JP2 ADVANCE MONITOR

ADV CH1-CH4

PB CH1-CH4

ADVRT → A11c → AU, A10c

DA OUT #1 → A5c → IV, 273-1A

DA OUT #2 → A5b → IV, 273-2A

DA OUT #3 → A5a → IV, 273-3A

DA OUT #4 → A6c → IV, 273-4A

EAD O #1 → A8c → IV, 273-6A

EAD O #2 → A8b → IV, 273-7A

EAD O #3 → A8a → IV, 273-8A

EAD O #4 → A9c → IV, 273-9A

AD A #1 → C14c → PG, C14c

AD A #2 → C14d → PG, C14a

AD A #3 → C14a → PG, C15c

AD A #4 → C15c → PG, C15a

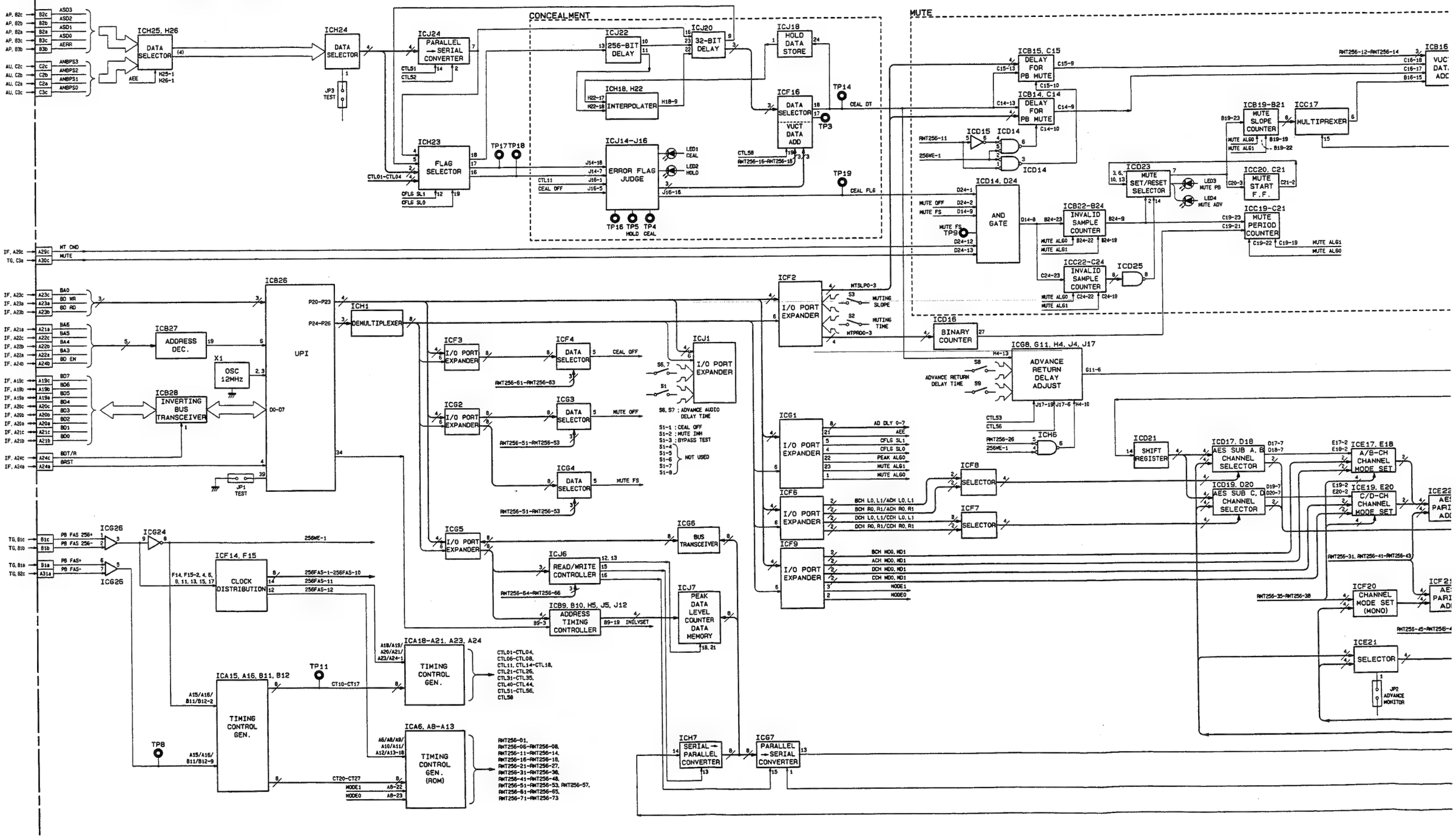
AN-01 BOARD BLOCK DIAGRAM
BOARD NO. 1-620-926-11
DVPC-1000 (J) : #10001-10699
DVPC-1000 (U/C) : #10001-10999
DVPC-1000 (EK) : #10001-10999

A-41 (a)

A-42 (a)

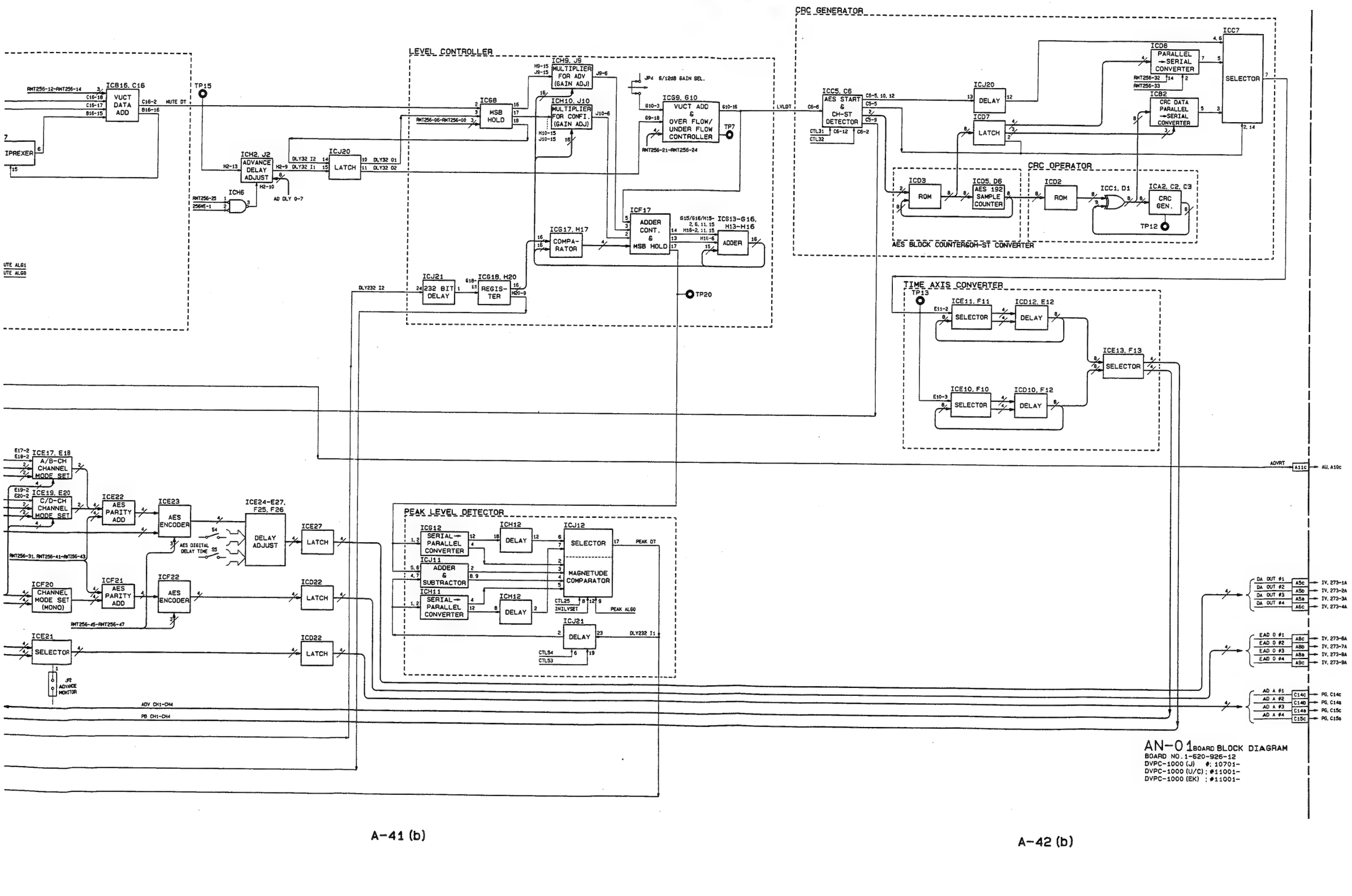
# AN-01 BOARD
Audio Concealment

**# 10701 & UP (J)**
**# 11001 & UP (UC)**
**# 11001 & UP (EK)**




A-39 (b)

A-40 (b)



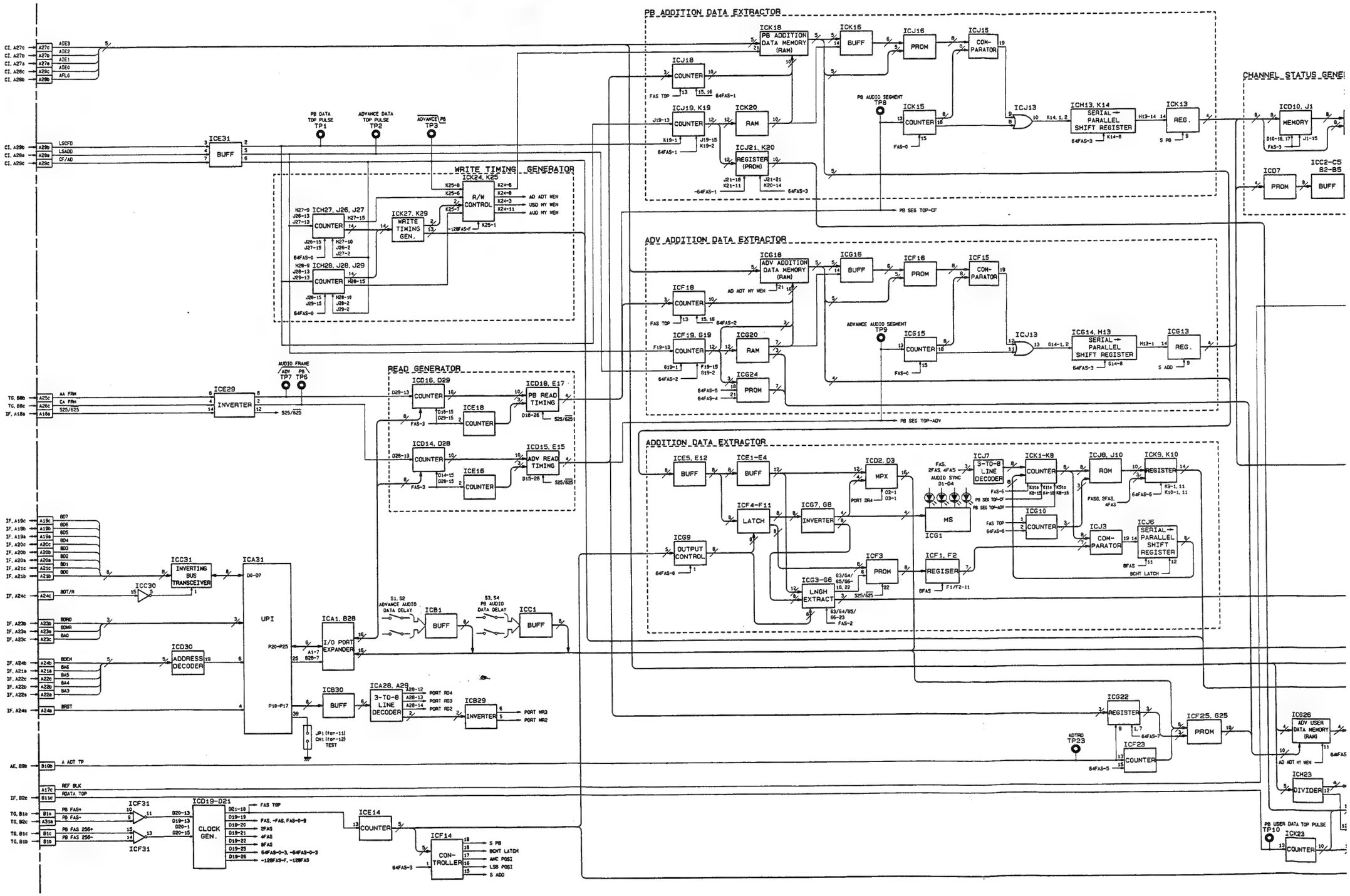

AN-01 BOARD BLOCK DIAGRAM
BOARD NO. 1-620-926-12
DVPC-1000 (J) #: 10701-
DVPC-1000 (U/C) : #11001-
DVPC-1000 (EK) : #11001-

A-41 (b)

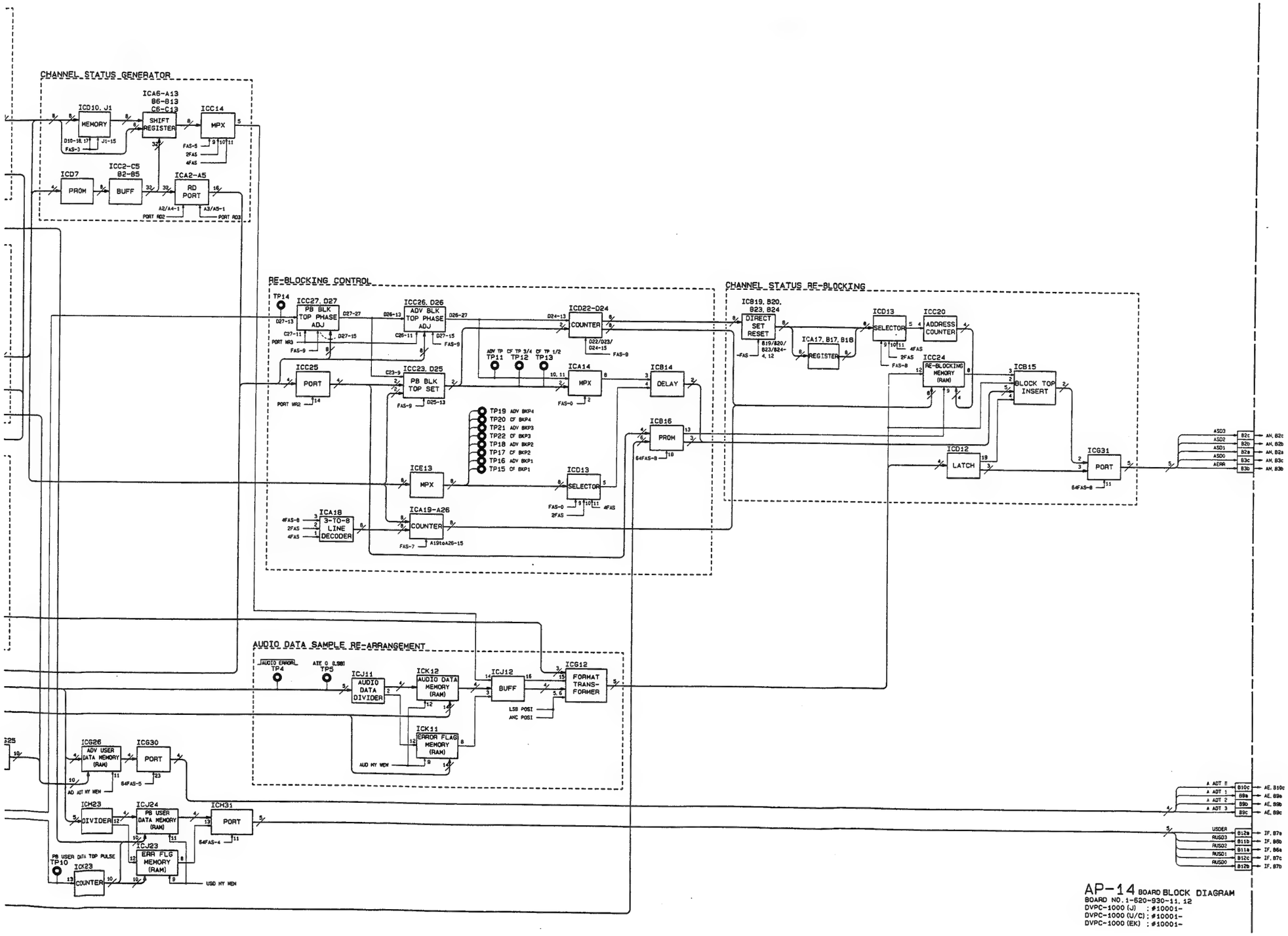
A-42 (b)

## AP-14 BOARD

Audio Output Control




A-43 A-44

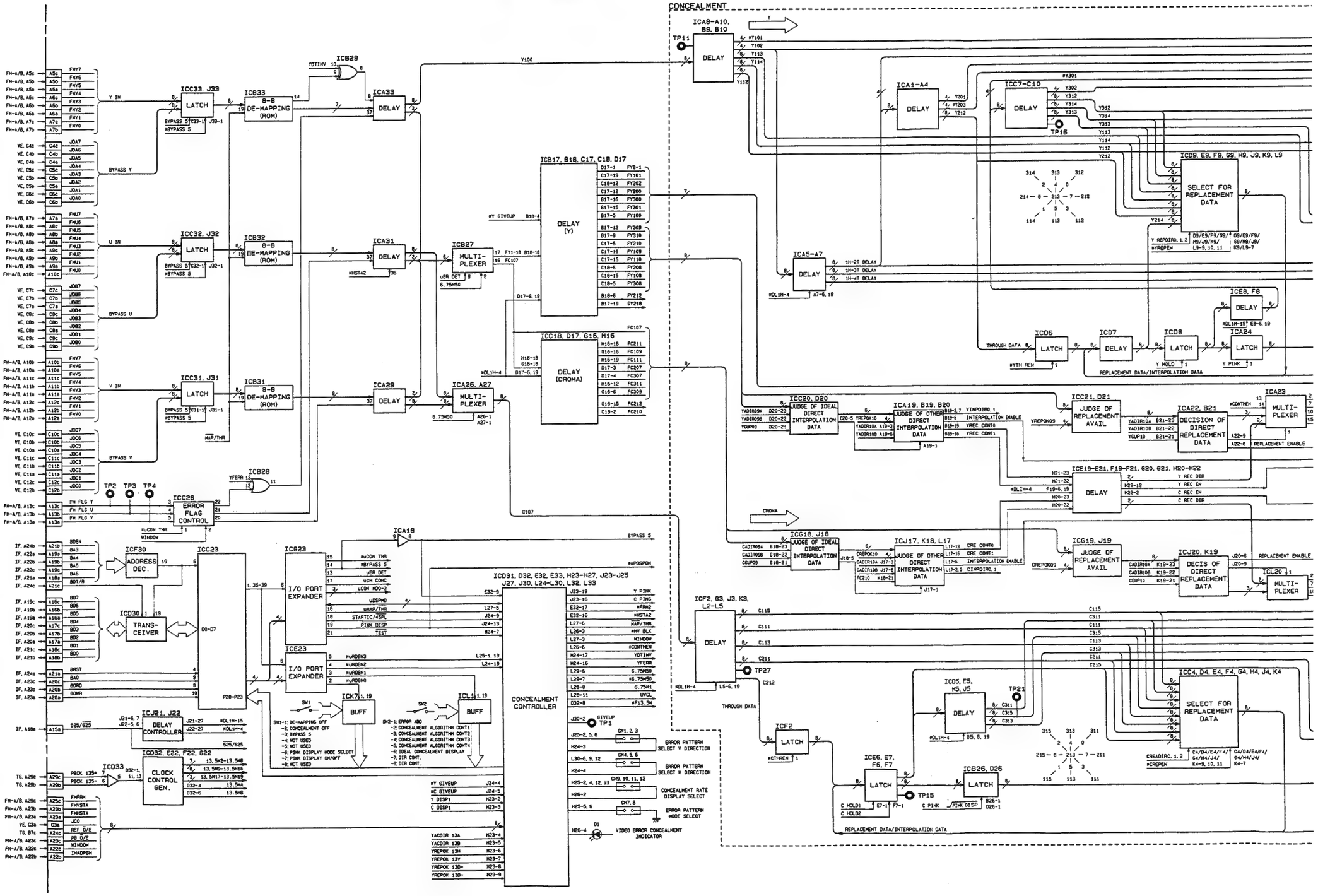



AP-14 BOARD BLOCK DIAGRAM
BOARD NO.1-620-930-11, 12
DVPC-1000 (J) : #10001-
DVPC-1000 (U/C) : #10001-
DVPC-1000 (EK) : #10001-

## VN-01 BOARD

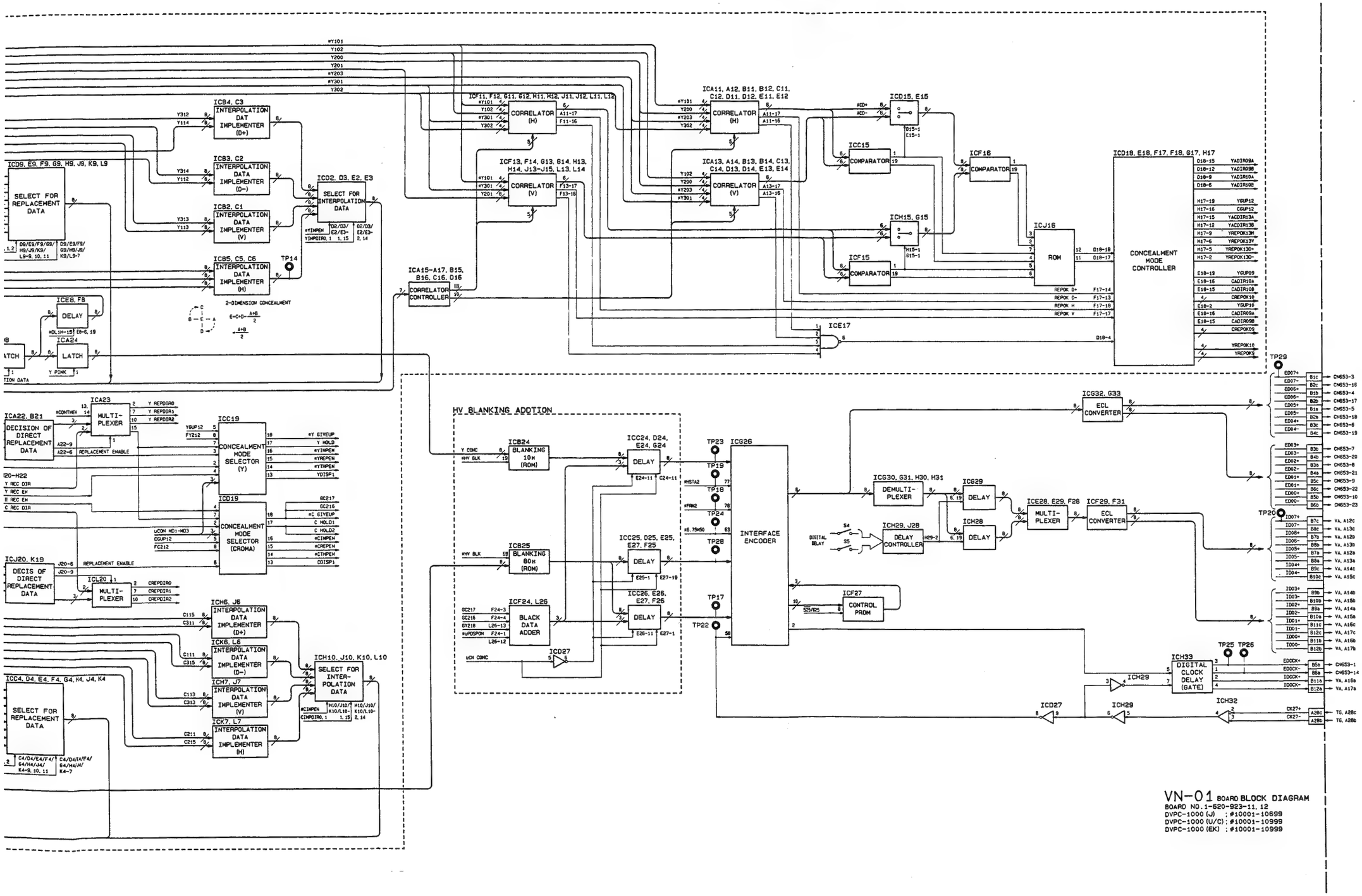
Video Concealment

| |
|---|
| # 10001 TO 10699 (J) |
| # 10001 TO 10999 (UC) |
| # 10001 TO 10999 (EK) |




A-47 (a)

A-48 (a)


ICB4, C3 INTERPOLATION DAT IMPLEMENTER (D+)
ICB3, C2 INTERPOLATION DATA IMPLEMENTER (D-)
ICB2, C1 INTERPOLATION DATA IMPLEMENTER (V)
ICB5, C5, C6 INTERPOLATION DATA IMPLEMENTER (H)
2-DIMENSION CONCEALMENT
ICD9, E9, F9, G9, H9, J9, K9, L9 SELECT FOR REPLACEMENT DATA
ICD2, D3, E2, E3 SELECT FOR INTERPOLATION DATA
ICE8, F8 DELAY
ICA24 LATCH
TP14
ICF11, F12, G11, G12, H11, H12, J11, J12, L11, L12 CORRELATOR (H)
ICF13, F14, G13, G14, H13, H14, J13-J15, L13, L14 CORRELATOR (V)
ICA11, A12, B11, B12, C11, C12, D11, D12, E11, E12 CORRELATOR (H)
ICA13, A14, B13, B14, C13, C14, D13, D14, E13, E14 CORRELATOR (V)
ICA15-A17, B15, B16, C16, D16 CORRELATOR CONTROLLER
ICD15, E15
ICC15 COMPARATOR
ICF16 COMPARATOR
ICH15, G15
ICF15 COMPARATOR
ICJ16 ROM
ICE17
ICD18, E18, F17, F18, G17, H17 CONCEALMENT MODE CONTROLLER
HV BLANKING ADDTION
ICB24 BLANKING 10H (ROM)
ICB25 BLANKING 80H (ROM)
ICC24, D24, E24, G24 DELAY
ICC25, D25, E25, E27, F25 DELAY
ICC26, E26, E27, F26 DELAY
ICF24, L26 BLACK DATA ADDER
ICD27
TP23 TP19 TP18 TP24 TP28 TP17 TP22
ICG26 INTERFACE ENCODER
ICG30, G31, H30, H31 DEMULTI-PLEXER
ICG29 DELAY
ICH29, J28 DELAY CONTROLLER
ICH28 DELAY
ICE28, E29, F28 MULTI-PLEXER
ICF29, F31 ECL CONVERTER
ICF27 CONTROL PROM
ICG32, G33 ECL CONVERTER
TP29 TP20
ICH33 DIGITAL CLOCK DELAY (GATE)
ICH32
TP25 TP26
ICA22, B21 DECISION OF DIRECT REPLACEMENT DATA
ICA23 MULTI-PLEXER
ICC19 CONCEALMENT MODE SELECTOR (Y)
ICD19 CONCEALMENT MODE SELECTOR (CROMA)
ICJ20, K19 DECIS OF DIRECT REPLACEMENT DATA
ICL20 MULTI-PLEXER
ICH6, J6 INTERPOLATION DATA IMPLEMENTER (D+)
ICK6, L6 INTERPOLATION DATA IMPLEMENTER (D-)
ICH7, J7 INTERPOLATION DATA IMPLEMENTER (V)
ICK7, L7 INTERPOLATION DATA IMPLEMENTER (H)
ICH10, J10, K10, L10 SELECT FOR INTER-POLATION DATA
ICC4, D4, E4, F4, G4, H4, J4, K4 SELECT FOR REPLACEMENT DATA
VN-01 BOARD BLOCK DIAGRAM
BOARD NO.1-520-923-11, 12
DVPC-1000 (J) : #10001-10699
DVPC-1000 (U/C) : #10001-10999
DVPC-1000 (EK) : #10001-10999

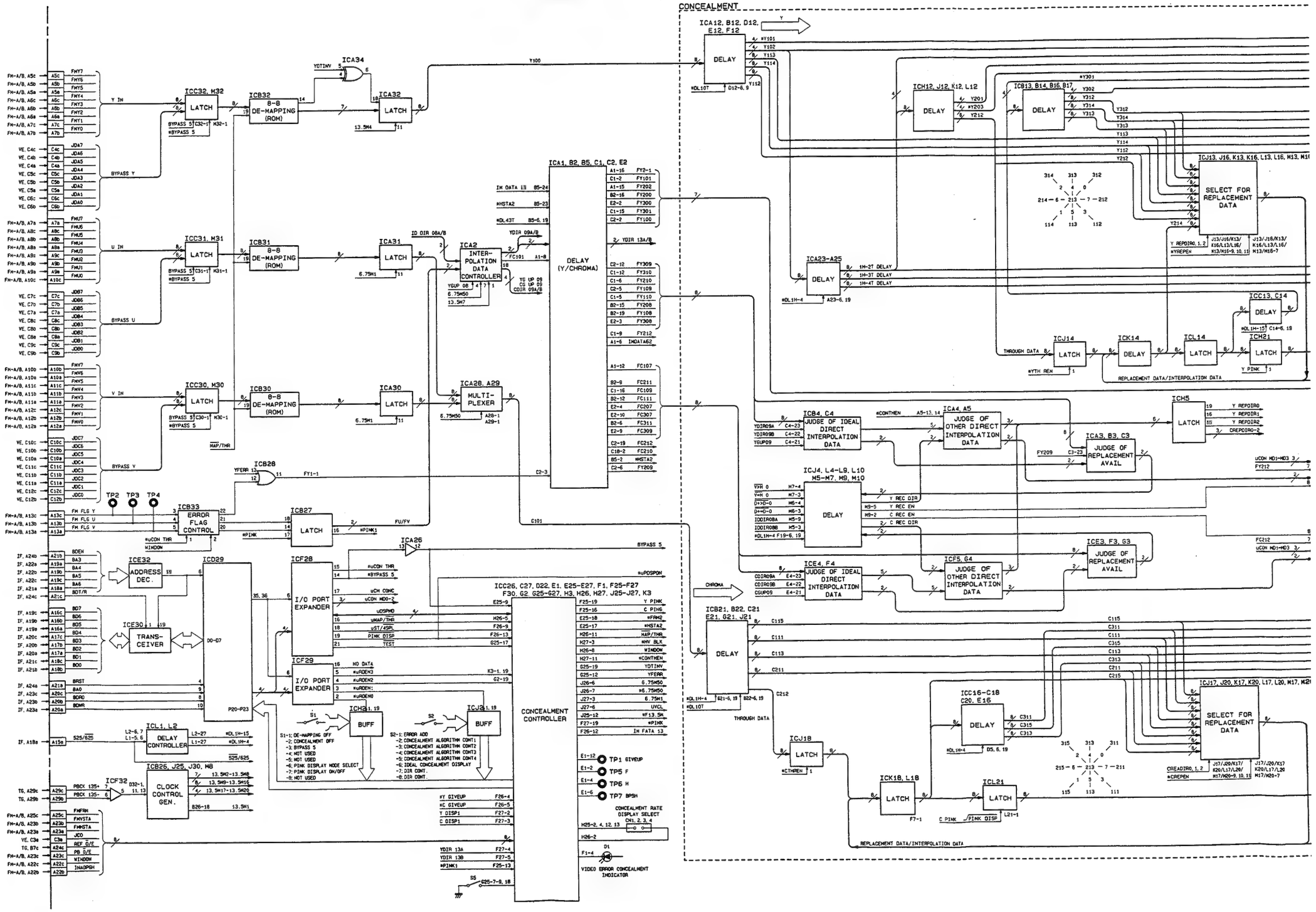
A-49 (a)

A-50 (a)

## VN-01 BOARD

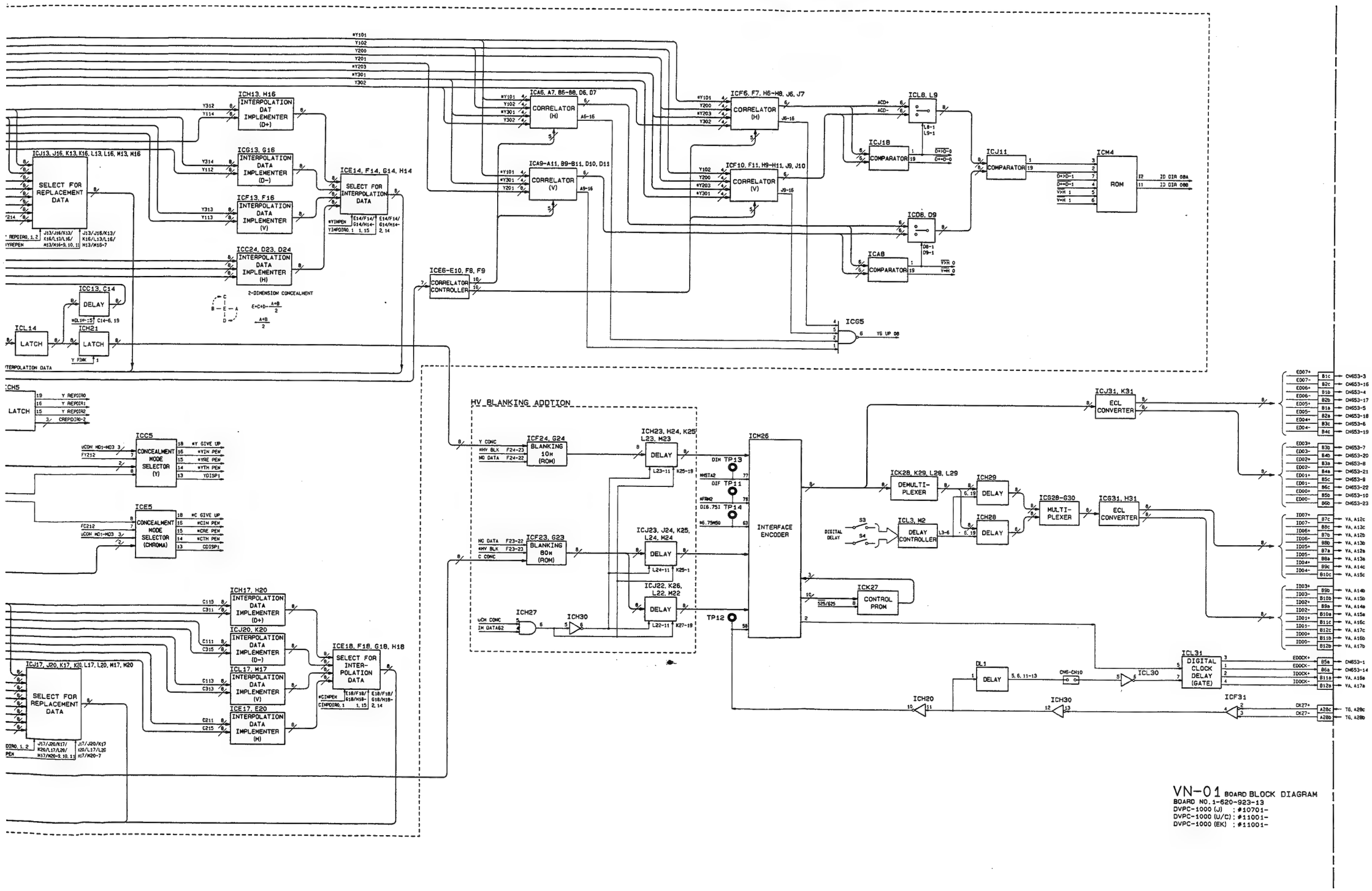
Video Concealment

| |
|---|
| # 10701 & UP (J) |
| # 11001 & UP (UC) |
| # 11001 & UP (EK) |




A-47 (b)

A-48 (b)



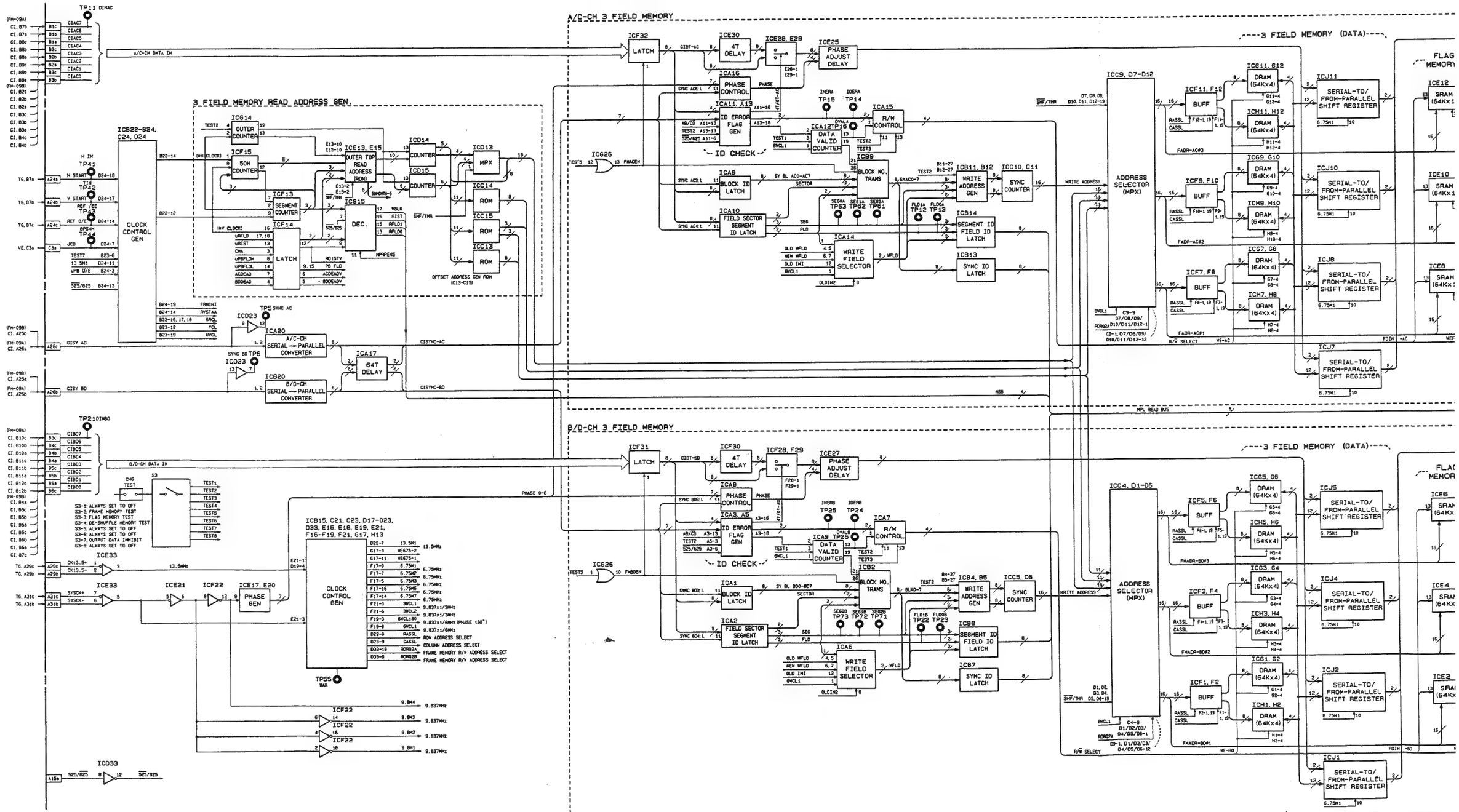

VN-01 BOARD BLOCK DIAGRAM
BOARD NO.1-620-923-13
DVPC-1000 (J) : #10701-
DVPC-1000 (U/C) : #11001-
DVPC-1000 (EK) : #11001-

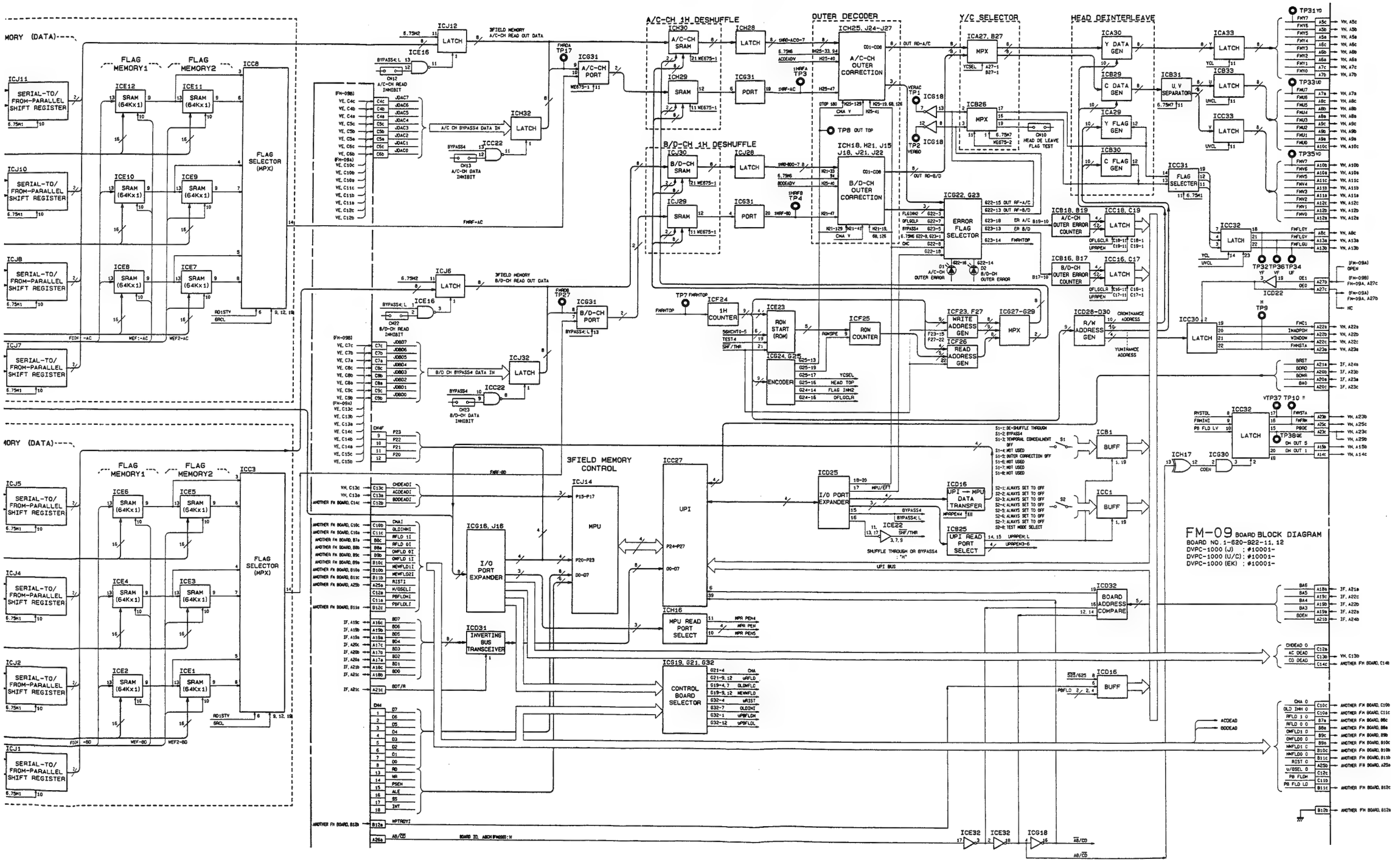
A-49 (b)

A-50 (b)

## FM-09 BOARD

Frame Memory

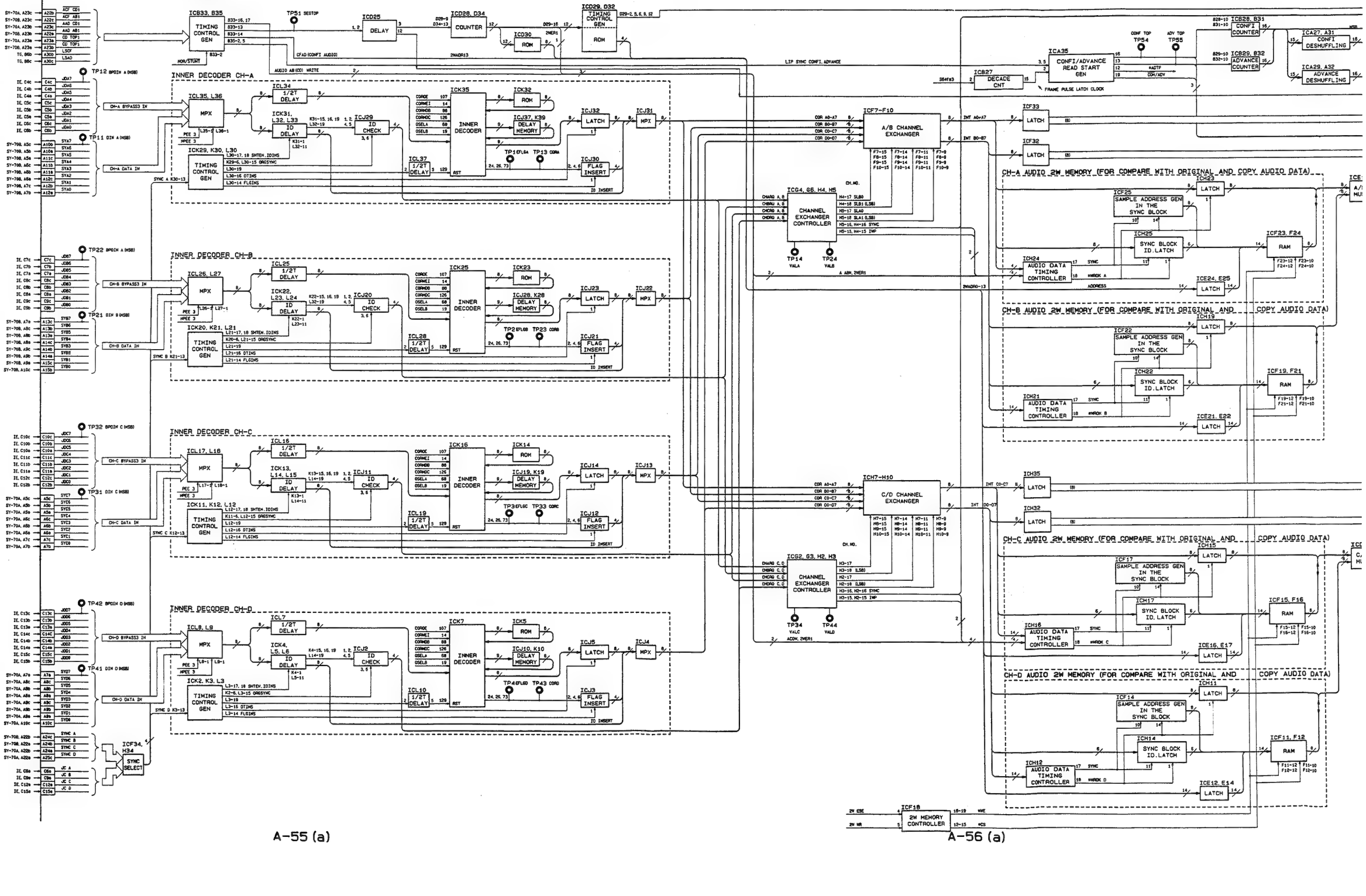



MEMORY (DATA)
FLAG MEMORY1
FLAG MEMORY2
FLAG SELECTOR (MPX)
SERIAL-TO/FROM-PARALLEL SHIFT REGISTER
SRAM (64Kx1)
A/C-CH 1H DESHUFFLE
B/D-CH 1H DESHUFFLE
OUTER DECODER
A/C-CH OUTER CORRECTION
B/D-CH OUTER CORRECTION
Y/C SELECTOR
HEAD DEINTERLEAVE
ERROR FLAG SELECTOR
3FIELD MEMORY CONTROL
I/O PORT EXPANDER
INVERTING BUS TRANSCEIVER
MPU READ PORT SELECT
CONTROL BOARD SELECTOR
UPI
MPU
UPI BUS
UPI → MPU DATA TRANSFER
UPI READ PORT SELECT
BOARD ADDRESS COMPARE
FM-09 BOARD BLOCK DIAGRAM
BOARD NO.1-520-922-11, 12
DVPC-1000 (J) : #10001-
DVPC-1000 (U/C): #10001-
DVPC-1000 (EK) : #10001-

# CI-01 BOARD

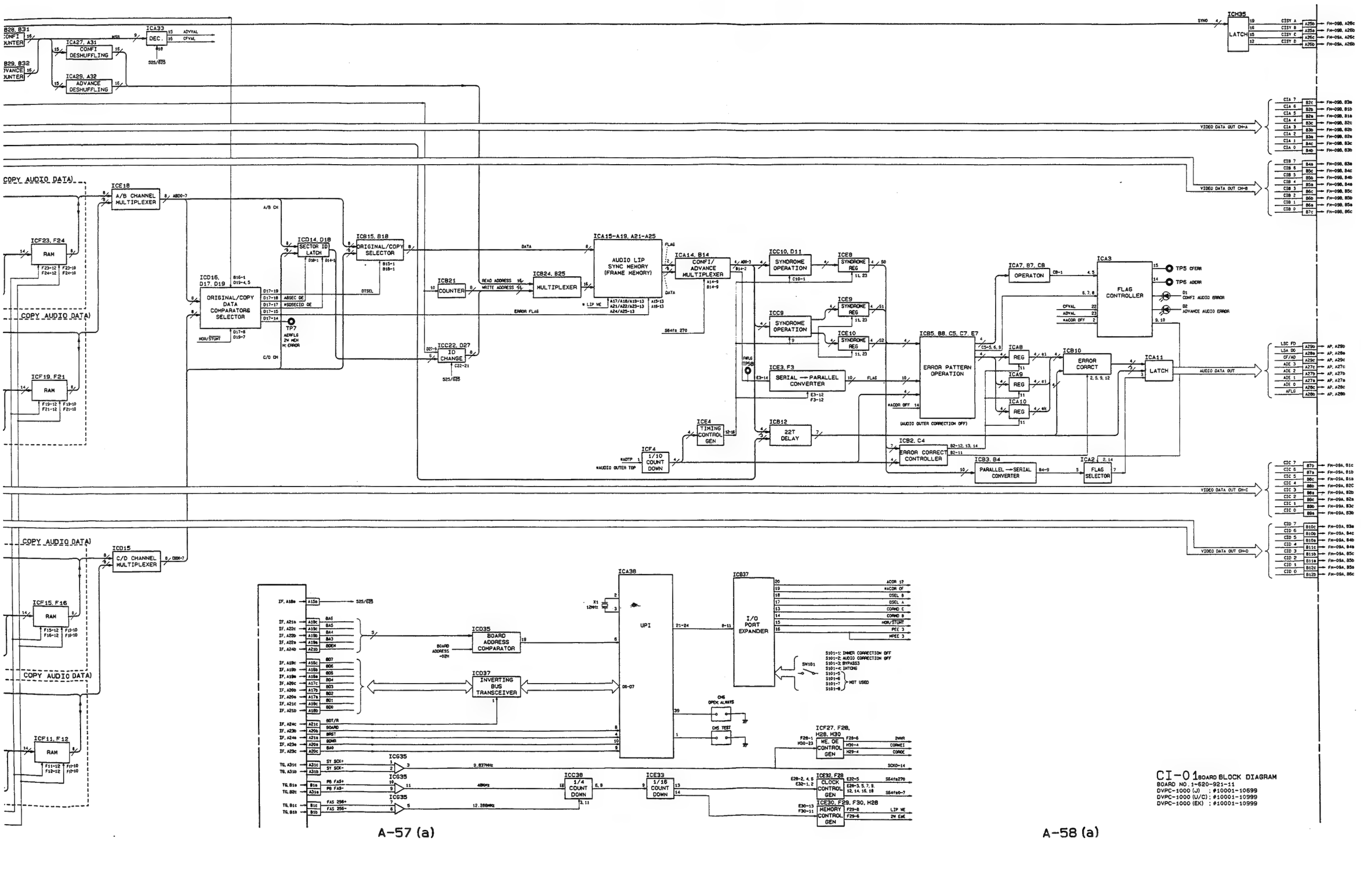
Inner Decoder

# 10001 TO 10699 (J)
# 10001 TO 10999 (UC)
# 10001 TO 10999 (EK)




A-55 (a)

A-56 (a)

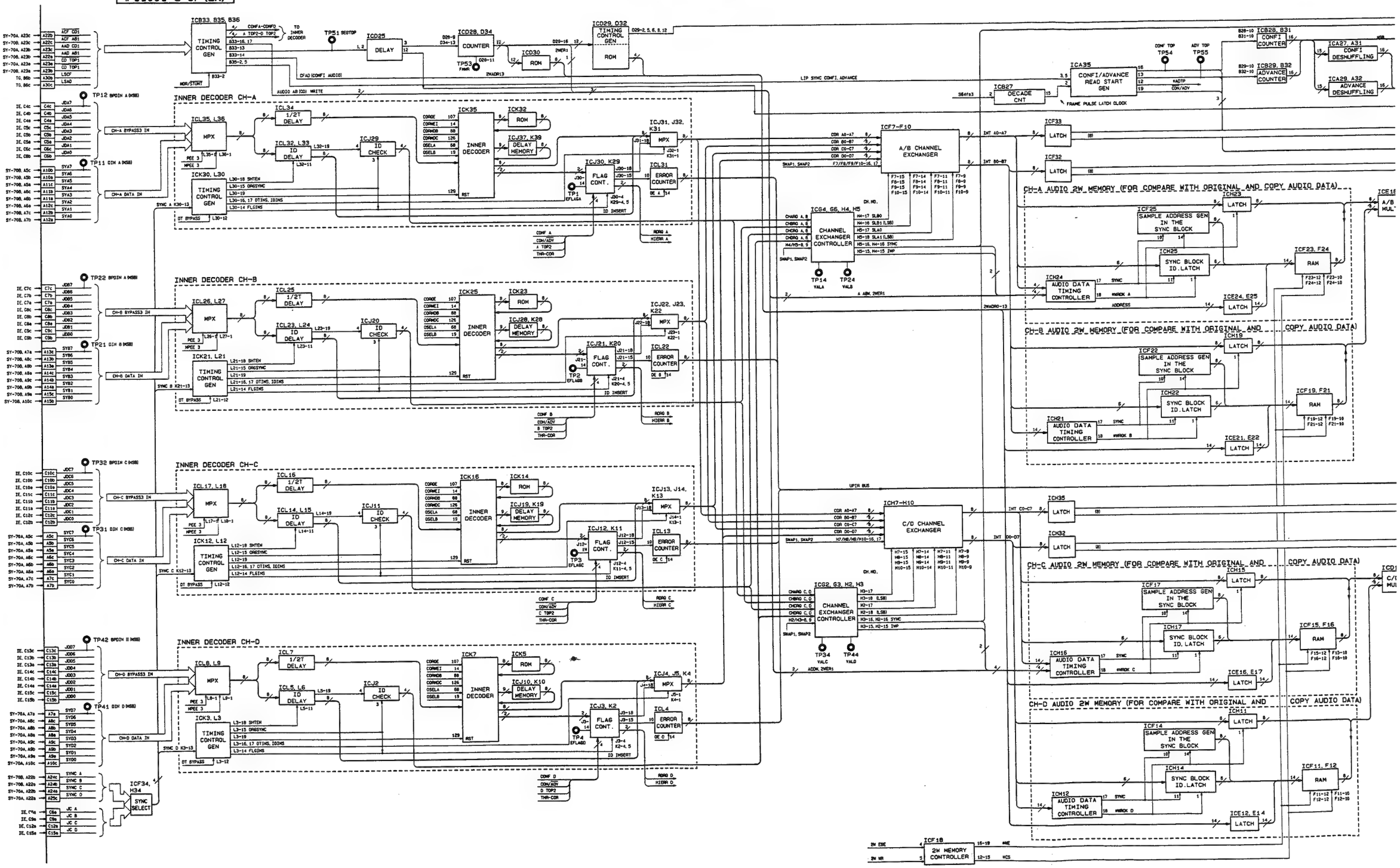

ICA27, A31
CONFI DESHUFFLING
ICA29, A32
ADVANCE DESHUFFLING
ICA33
DEC.
ICH35
LATCH
VIDEO DATA OUT CH-A
VIDEO DATA OUT CH-B
VIDEO DATA OUT CH-C
VIDEO DATA OUT CH-D
COPY AUDIO DATA)
ICE18
A/B CHANNEL MULTIPLEXER
ICF23, F24
RAM
ICF19, F21
RAM
ICD16, D17, D19
ORIGINAL/COPY DATA COMPARATORS SELECTOR
ICD14, D18
SECTOR ID LATCH
ICB15, B18
ORIGINAL/COPY SELECTOR
ICB21
COUNTER
ICB24, B25
MULTIPLEXER
ICA15-A19, A21-A25
AUDIO LIP SYNC MEMORY (FRAME MEMORY)
ICA14, B14
CONFI/ ADVANCE MULTIPLEXER
ICC22, D27
ID CHANGE
ICC10, D11
SYNDROME OPERATION
ICE8
SYNDROME REG
ICC9
SYNDROME OPERATION
ICE9
SYNDROME REG
ICE10
SYNDROME REG
ICE3, F3
SERIAL — PARALLEL CONVERTER
ICE4
TIMING CONTROL GEN
ICB12
22T DELAY
ICF4
1/10 COUNT DOWN
ICB5, B8, C5, C7, E7
ERROR PATTERN OPERATION
ICA7, B7, C8
OPERATON
ICA8
REG
ICA9
REG
ICA10
REG
ICA3
FLAG CONTROLLER
ICB10
ERROR CORRECT
ICA11
LATCH
ICB2, C4
ERROR CORRECT CONTROLLER
ICB3, B4
PARALLEL — SERIAL CONVERTER
ICA2
FLAG SELECTOR
TP5 CFERR
TP6 ADERR
D1 CONFI AUDIO ERROR
D2 ADVANCE AUDIO ERROR
AUDIO DATA OUT
(AUDIO OUTER CORRECTION OFF)
COPY AUDIO DATA)
ICD15
C/D CHANNEL MULTIPLEXER
ICF15, F16
RAM
ICF11, F12
RAM
ICA38
UPI
ICB37
I/O PORT EXPANDER
ICD35
BOARD ADDRESS COMPARATOR
ICD37
INVERTING BUS TRANSCEIVER
ICC35
ICC38
1/4 COUNT DOWN
ICE33
1/16 COUNT DOWN
ICF27, F28, H28, H30
WE, OE CONTROL GEN
ICE32, F28
CLOCK CONTROL GEN
ICE30, F29, F30, H28
MEMORY CONTROL GEN
SW101
CI-01 BOARD BLOCK DIAGRAM
BOARD NO.1-620-921-11
DVPC-1000 (J) : #10001-10699
DVPC-1000 (U/C) : #10001-10999
DVPC-1000 (EK) : #10001-10999

A-57 (a)

A-58 (a)

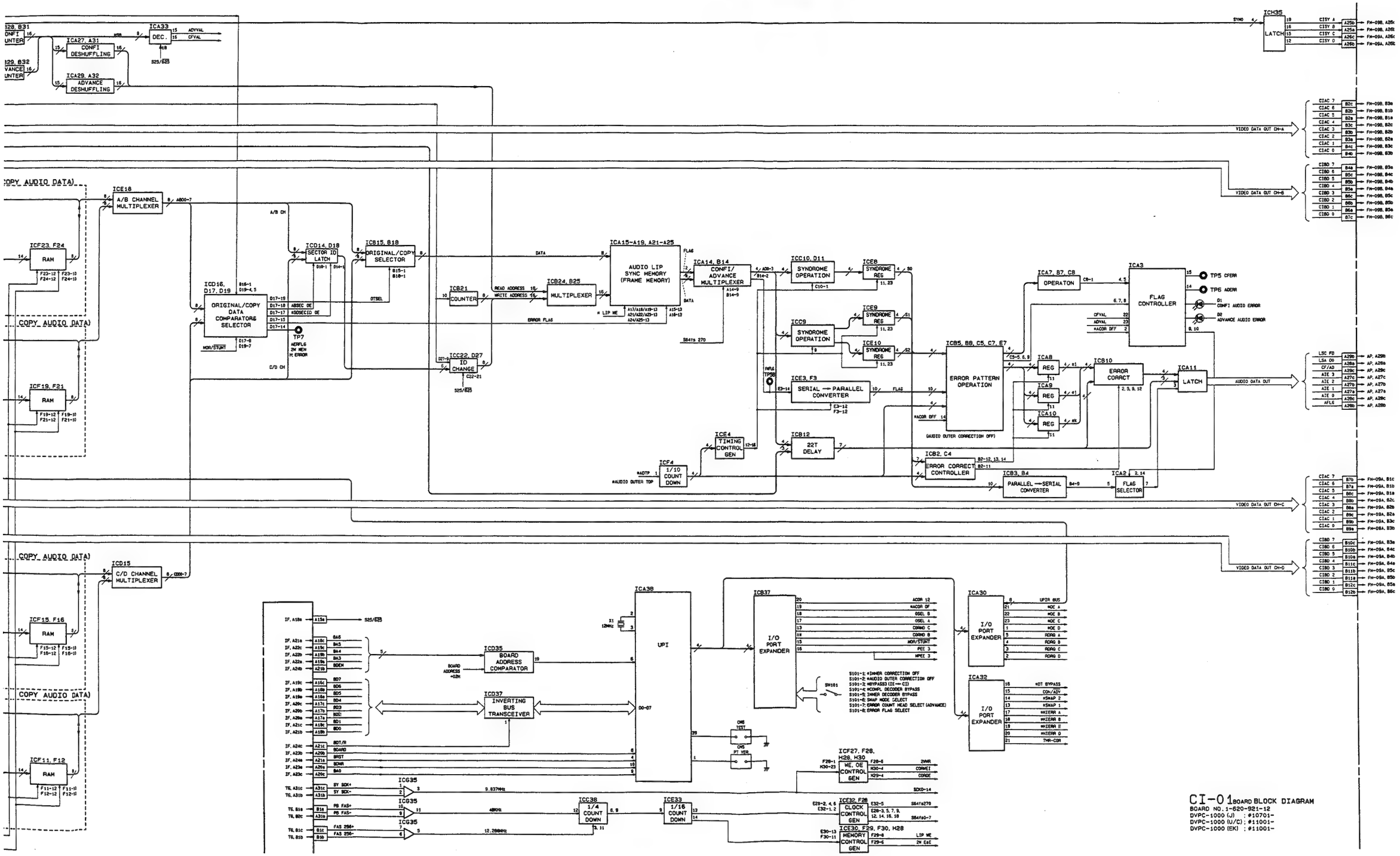
# CI-01 BOARD
Inner Decoder

| |
|---|
| # 10701 & UP (J) |
| # 11001 & UP (UC) |
| # 11001 & UP (EK) |




A-55 (b)

A-56 (b)


ICH35
LATCH
SYNO
CISY A
CISY B
CISY C
CISY D
VIDEO DATA OUT CH-A
VIDEO DATA OUT CH-B
VIDEO DATA OUT CH-C
VIDEO DATA OUT CH-D
COPY AUDIO DATA)
ICE18
A/B CHANNEL MULTIPLEXER
ICF23, F24
RAM
ICF19, F21
RAM
ICD16, D17, D19
ORIGINAL/COPY DATA COMPARATOR& SELECTOR
ICD14, D18
SECTOR ID LATCH
ICB15, B18
ORIGINAL/COPY SELECTOR
ICB21
COUNTER
ICB24, B25
MULTIPLEXER
ICA15~A19, A21~A25
AUDIO LIP SYNC MEMORY (FRAME MEMORY)
ICA14, B14
CONFI/ ADVANCE MULTIPLEXER
ICC22, D27
ID CHANGE
TP7
ICC10, D11
SYNDROME OPERATION
ICC9
SYNDROME OPERATION
ICE8
SYNDROME REG
ICE9
SYNDROME REG
ICE10
SYNDROME REG
ICA7, B7, C8
OPERATON
ICA3
FLAG CONTROLLER
TP5 CFERR
TP6 ADERR
D1 CONFI AUDIO ERROR
D2 ADVANCE AUDIO ERROR
ICB5, B6, C5, C7, E7
ERROR PATTERN OPERATION
(AUDIO OUTER CORRECTION OFF)
ICA8
REG
ICA9
REG
ICA10
REG
ICB10
ERROR CORRCT
ICA11
LATCH
AUDIO DATA OUT
ICE3, F3
SERIAL → PARALLEL CONVERTER
ICE4
TIMING CONTROL GEN
ICB12
22T DELAY
ICF4
1/10 COUNT DOWN
ICB2, C4
ERROR CORRECT CONTROLLER
ICB3, B4
PARALLEL → SERIAL CONVERTER
ICA2
FLAG SELECTOR
COPY AUDIO DATA)
ICD15
C/D CHANNEL MULTIPLEXER
ICF13, F16
RAM
ICF11, F12
RAM
ICA38
UPI
ICB37
I/O PORT EXPANDER
ICA30
I/O PORT EXPANDER
ICA32
I/O PORT EXPANDER
ICD35
BOARD ADDRESS COMPARATOR
ICD37
INVERTING BUS TRANSCEIVER
ICG35
ICC38
1/4 COUNT DOWN
ICE33
1/16 COUNT DOWN
ICE32, F26
CLOCK CONTROL GEN
ICE30, F29, F30, H28
MEMORY CONTROL GEN
ICF27, F28, H26, H30
WE, OE CONTROL GEN
CI-01 BOARD BLOCK DIAGRAM
BOARD NO.1-620-921-12
DVPC-1000 (J) : #10701-
DVPC-1000 (U/C) : #11001-
DVPC-1000 (EK) : #11001-

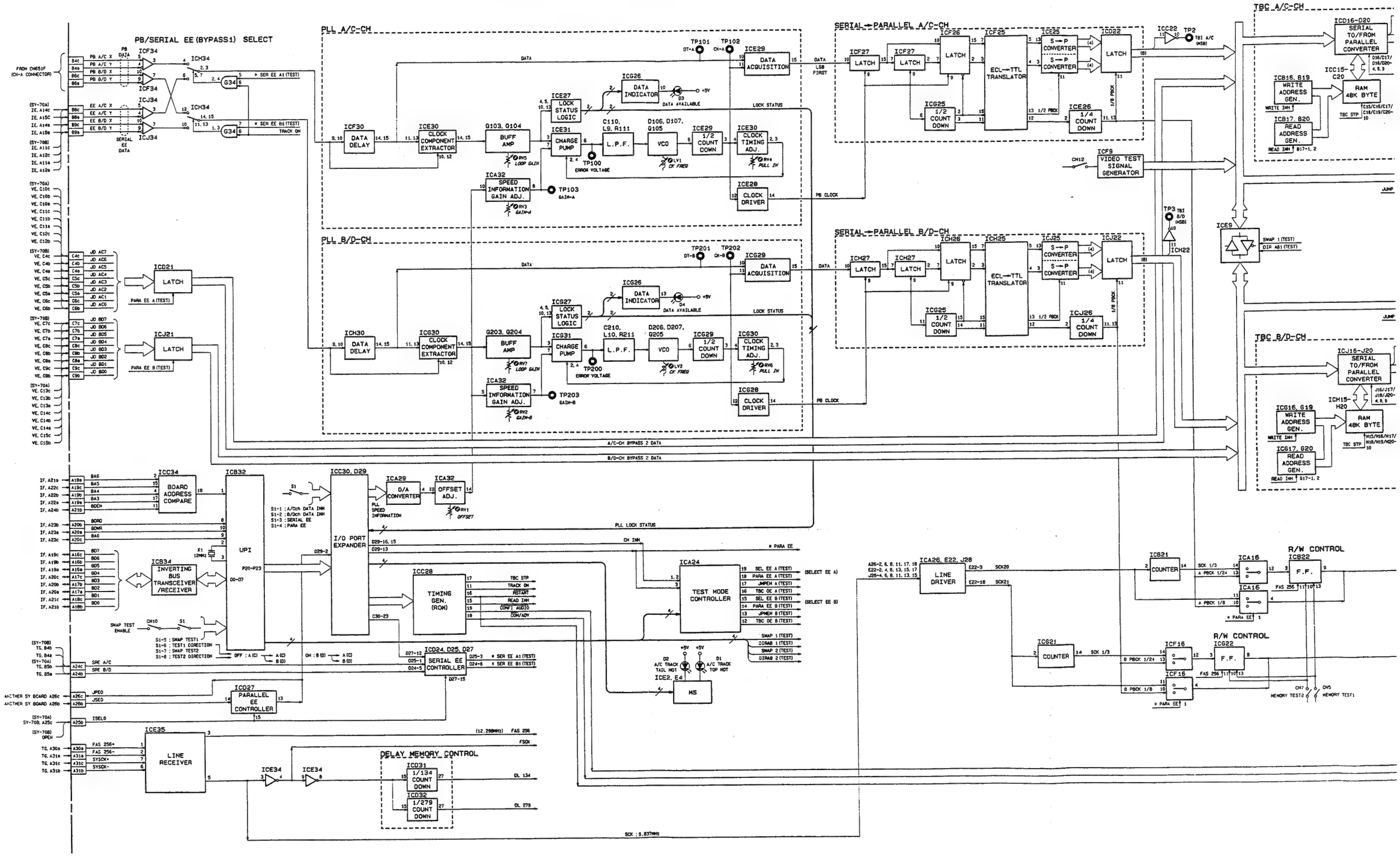
A-57 (b)

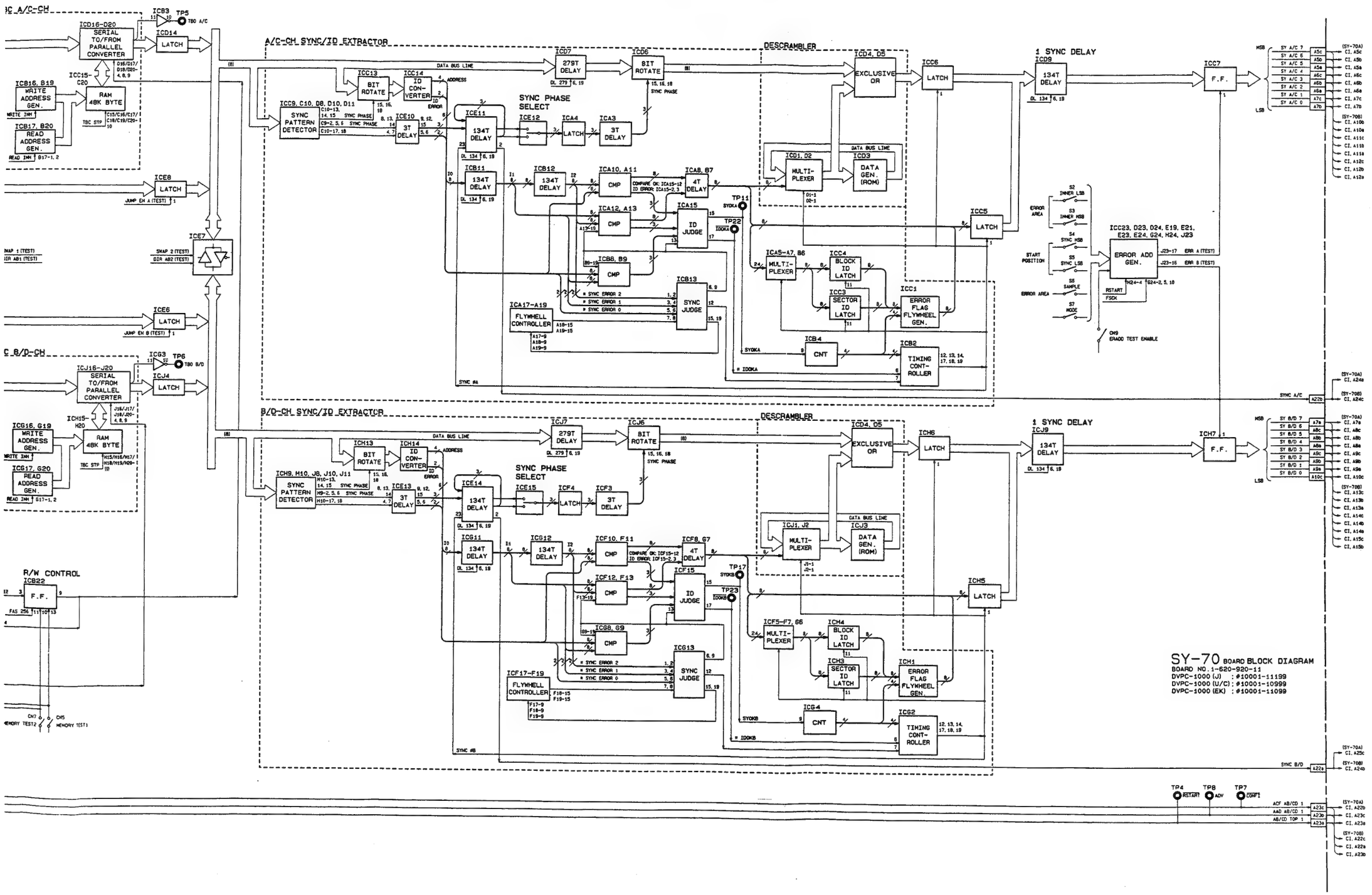
A-58 (b)

**SY-70 BOARD**
SYNC/ID Extractor

| |
|---|
| # 10001 TO 11199 (J) |
| # 10001 TO 10999 (UC) |
| # 10001 TO 11099 (EK) |



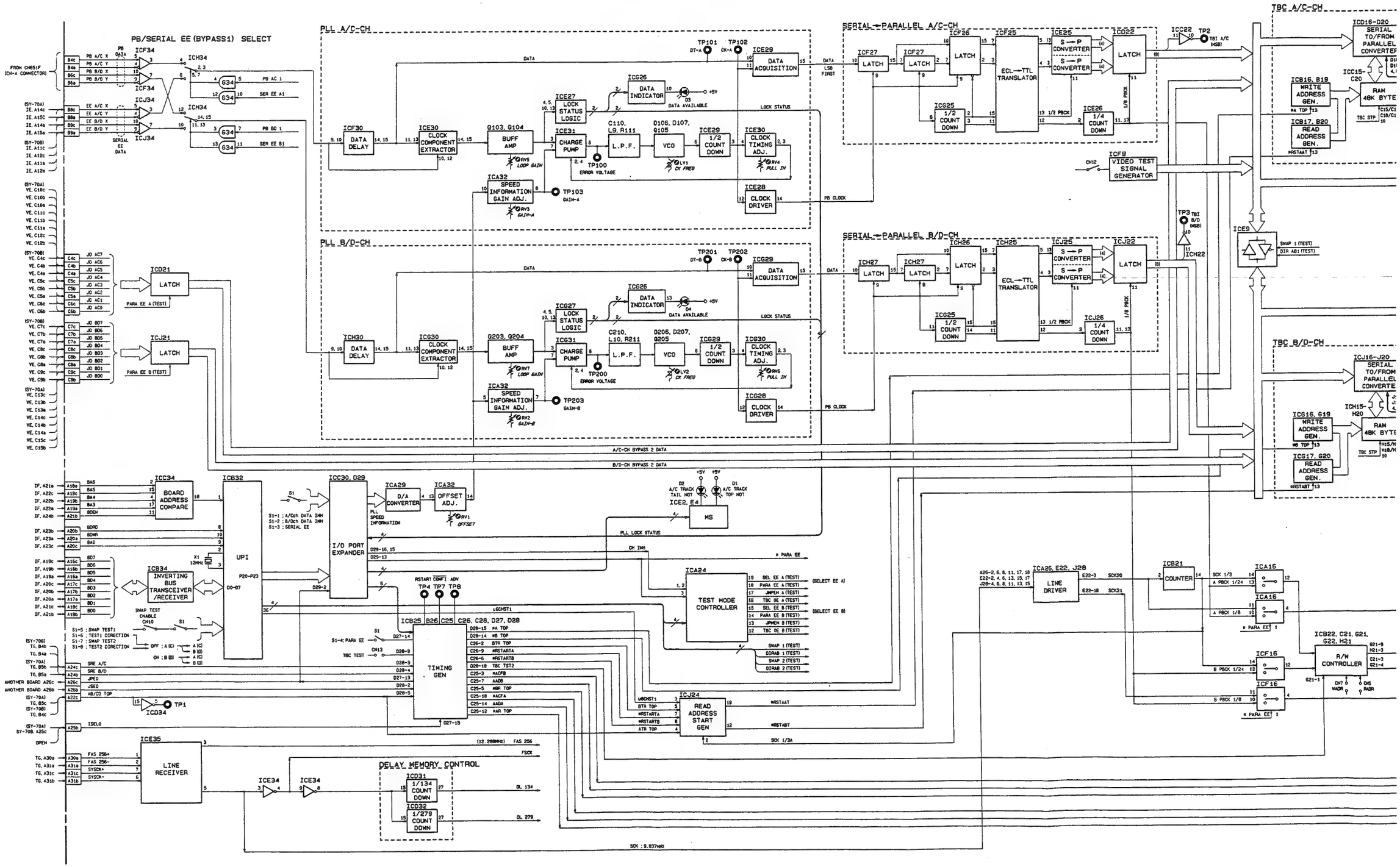



A/C-CH SYNC/ID EXTRACTOR
B/D-CH SYNC/ID EXTRACTOR
DESCRAMBLER
1 SYNC DELAY
SYNC PHASE SELECT
SYNC PATTERN DETECTOR
BIT ROTATE
ID CON-VERTER
279T DELAY
134T DELAY
3T DELAY
4T DELAY
LATCH
CMP
ID JUDGE
SYNC JUDGE
FLYWHELL CONTROLLER
SERIAL TO/FROM PARALLEL CONVERTER
WRITE ADDRESS GEN.
READ ADDRESS GEN.
RAM 48K BYTE
EXCLUSIVE OR
MULTI-PLEXER
DATA GEN. (ROM)
BLOCK ID LATCH
SECTOR ID LATCH
ERROR FLAG FLYWHEEL GEN.
TIMING CONT-ROLLER
CNT
F.F.
ERROR ADD GEN.
R/W CONTROL
SY-70 BOARD BLOCK DIAGRAM
BOARD NO.:620-920-11
DVPC-1000 (J) : #10001-11199
DVPC-1000 (U/C) : #10001-10999
DVPC-1000 (EK) : #10001-11099

**SY-70 BOARD**
SYNC/ID Extractor

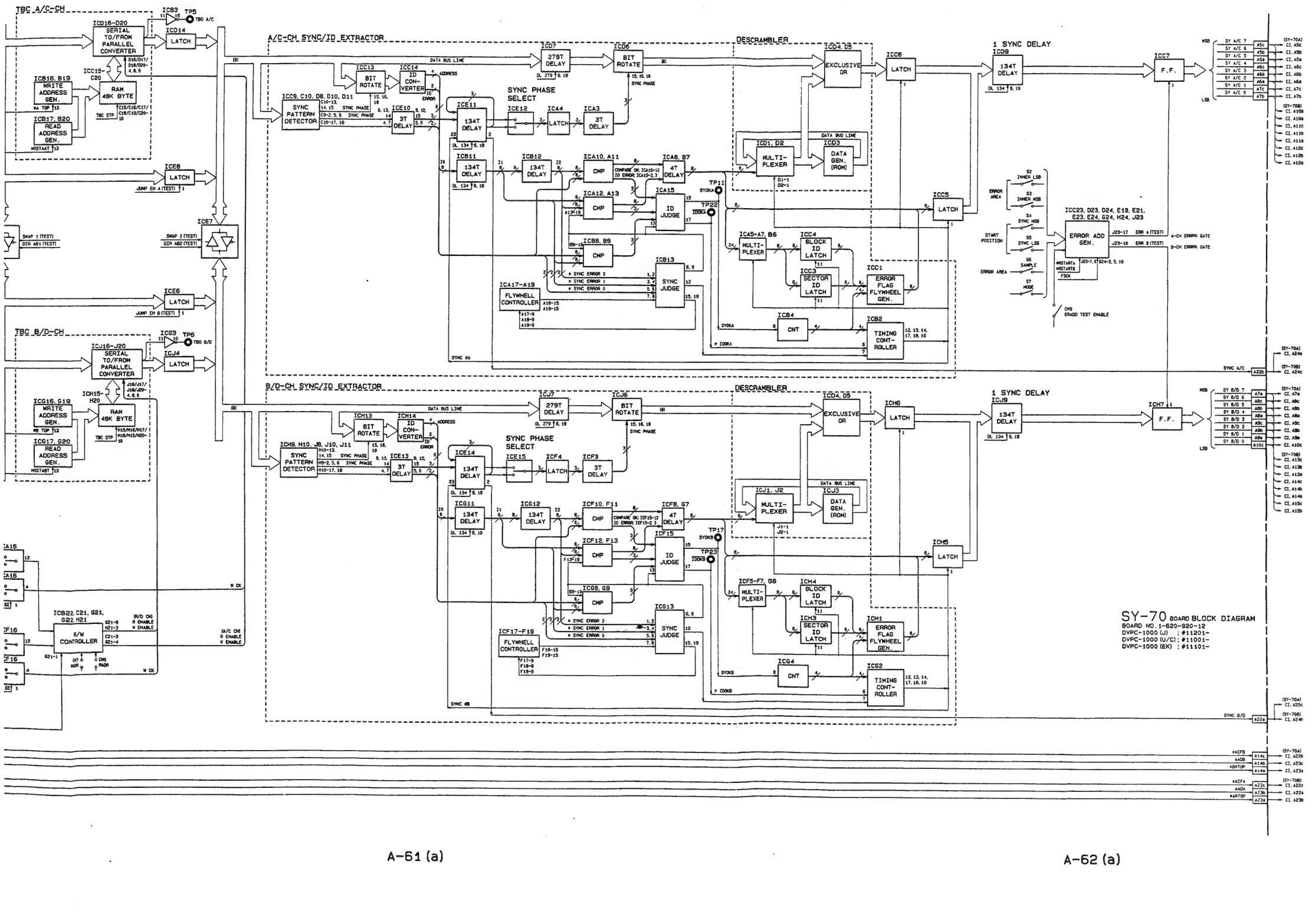
| |
|---|
| # 11201 & UP (J) |
| # 11001 & UP (UC) |
| # 11101 & UP (EK) |

BLOCK DIAGRAM **SY-70** [redacted] **SY-70** BLOCK DIAGRAM




A-59 (a)

A-60 (a)

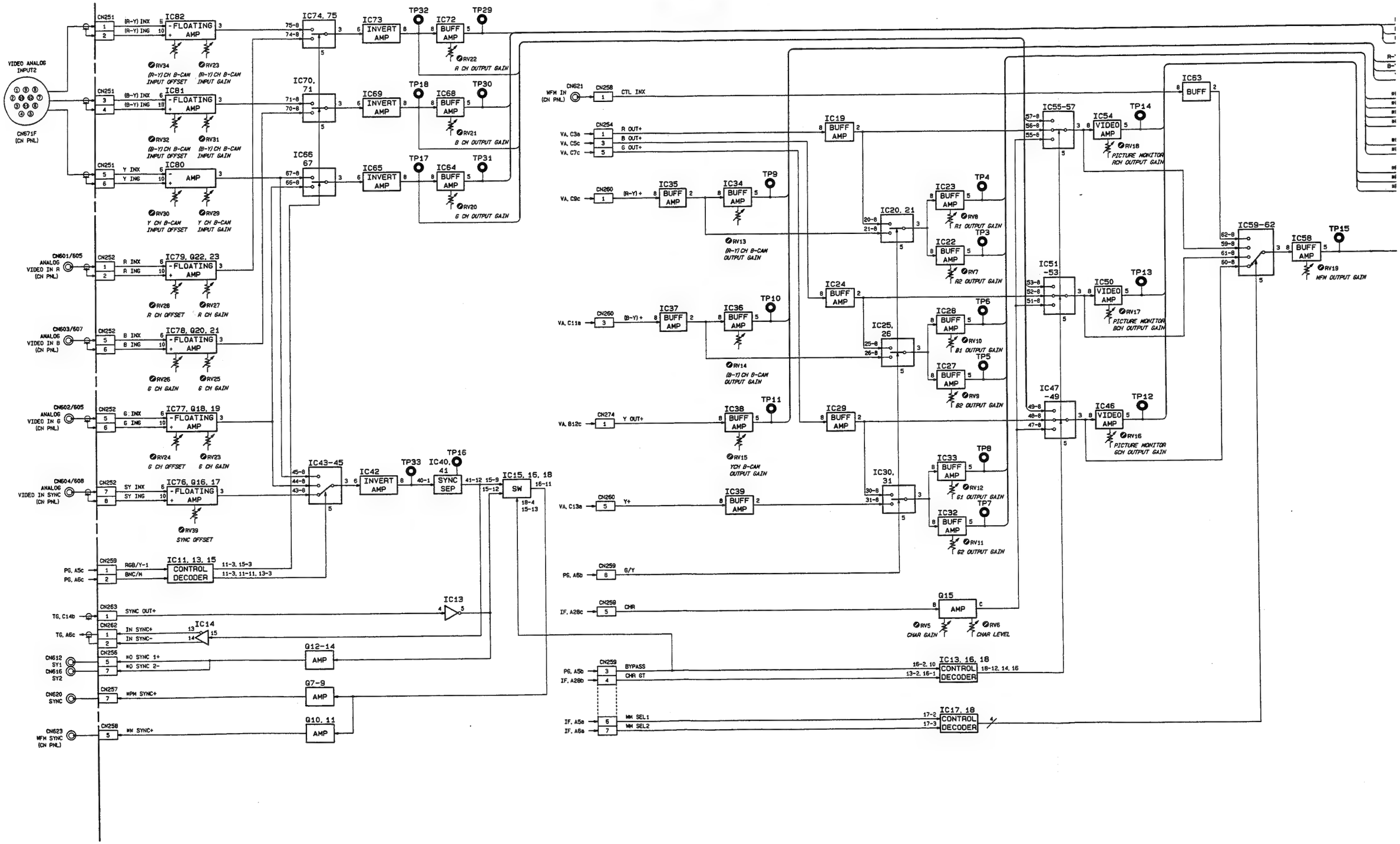

TBC A/C-CH
TBC B/D-CH
A/C-CH SYNC/ID EXTRACTOR
B/D-CH SYNC/ID EXTRACTOR
DESCRAMBLER
SYNC PHASE SELECT
1 SYNC DELAY
SERIAL TO/FROM PARALLEL CONVERTER
WRITE ADDRESS GEN.
READ ADDRESS GEN.
RAM 48K BYTE
LATCH
SYNC PATTERN DETECTOR
BIT ROTATE
ID CON-VERTER
279T DELAY
134T DELAY
3T DELAY
4T DELAY
CMP
ID JUDGE
SYNC JUDGE
FLYWHELL CONTROLLER
MULTI-PLEXER
BLOCK ID LATCH
SECTOR ID LATCH
ERROR FLAG FLYWHEEL GEN.
TIMING CONT-ROLLER
CNT
EXCLUSIVE OR
DATA GEN. (ROM)
F.F.
ERROR ADD GEN.
R/W CONTROLLER
SWAP 1 (TEST)
SWAP 2 (TEST)
JUMP EN A (TEST)
JUMP EN B (TEST)
SYNC A/C
SYNC B/D
SY-70 BOARD BLOCK DIAGRAM
BOARD NO. 1-620-920-12
DVPC-1000 (J) : #11201~
DVPC-1000 (U/C) : #11001~
DVPC-1000 (EK) : #11101~

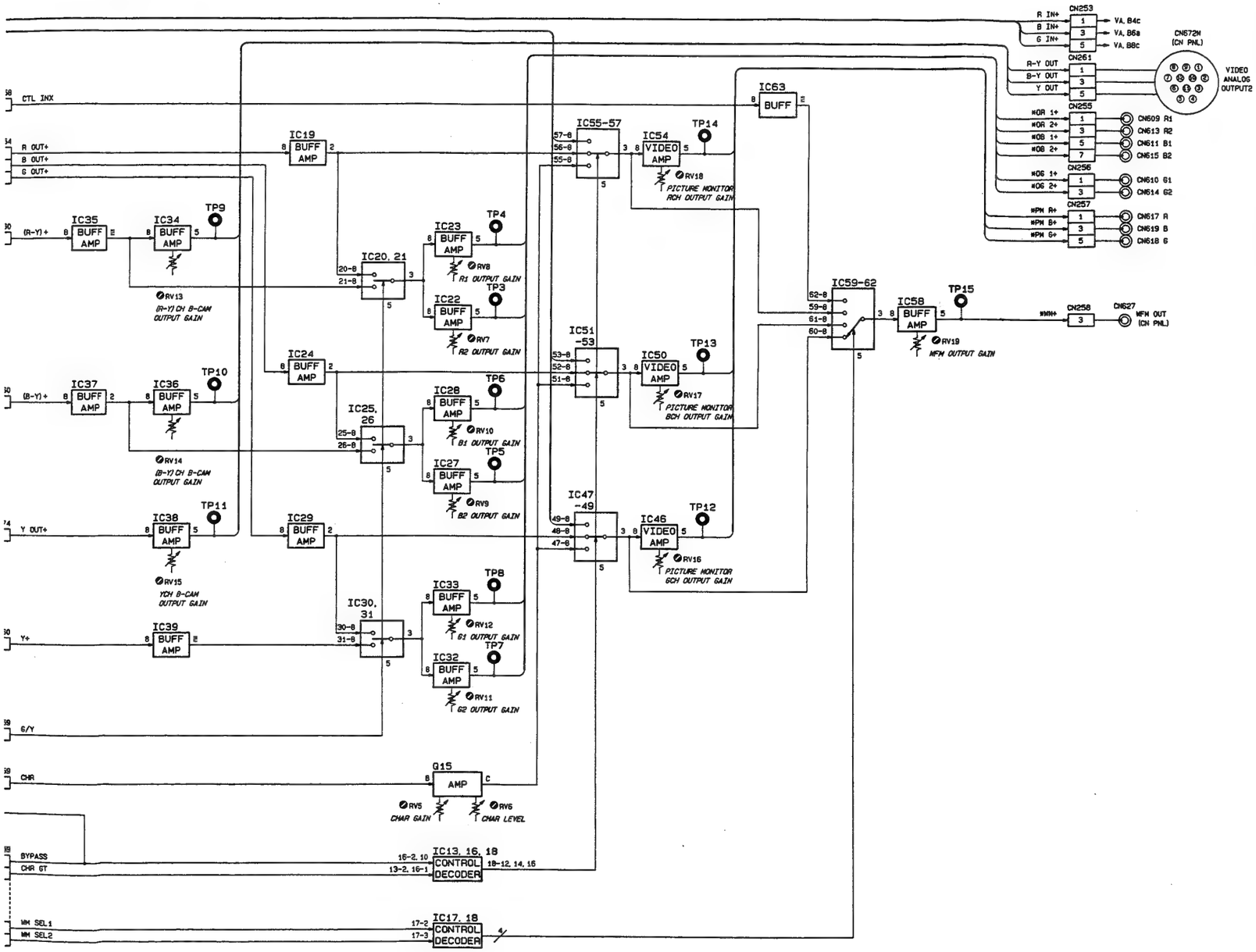
A-61 (a)

A-62 (a)

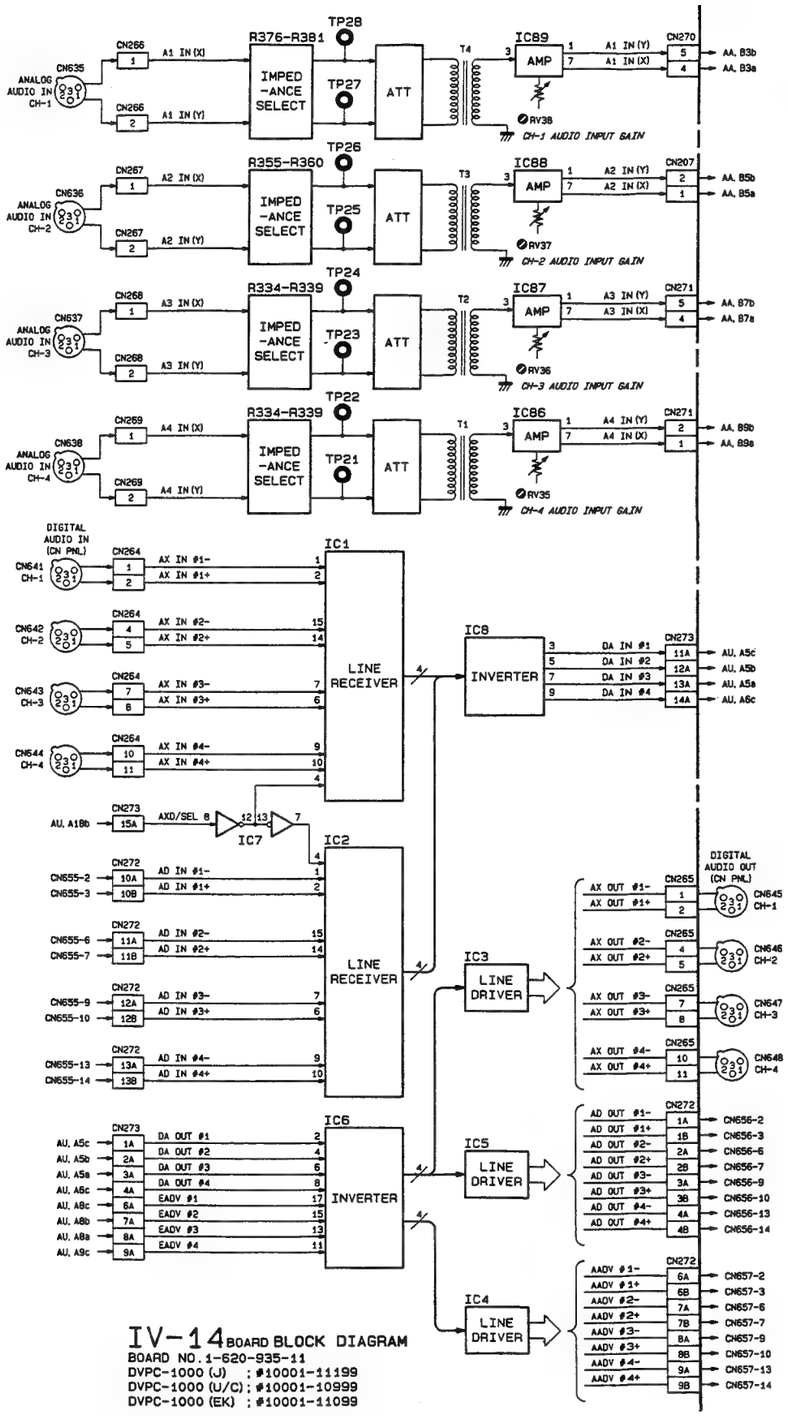
**IV-14** BOARD
Video & Audio I/O

| |
|---|
| #10001 TO 11199 (J) |
| #10001 TO 10999 (UC) |
| #10001 TO 11099 (EK) |







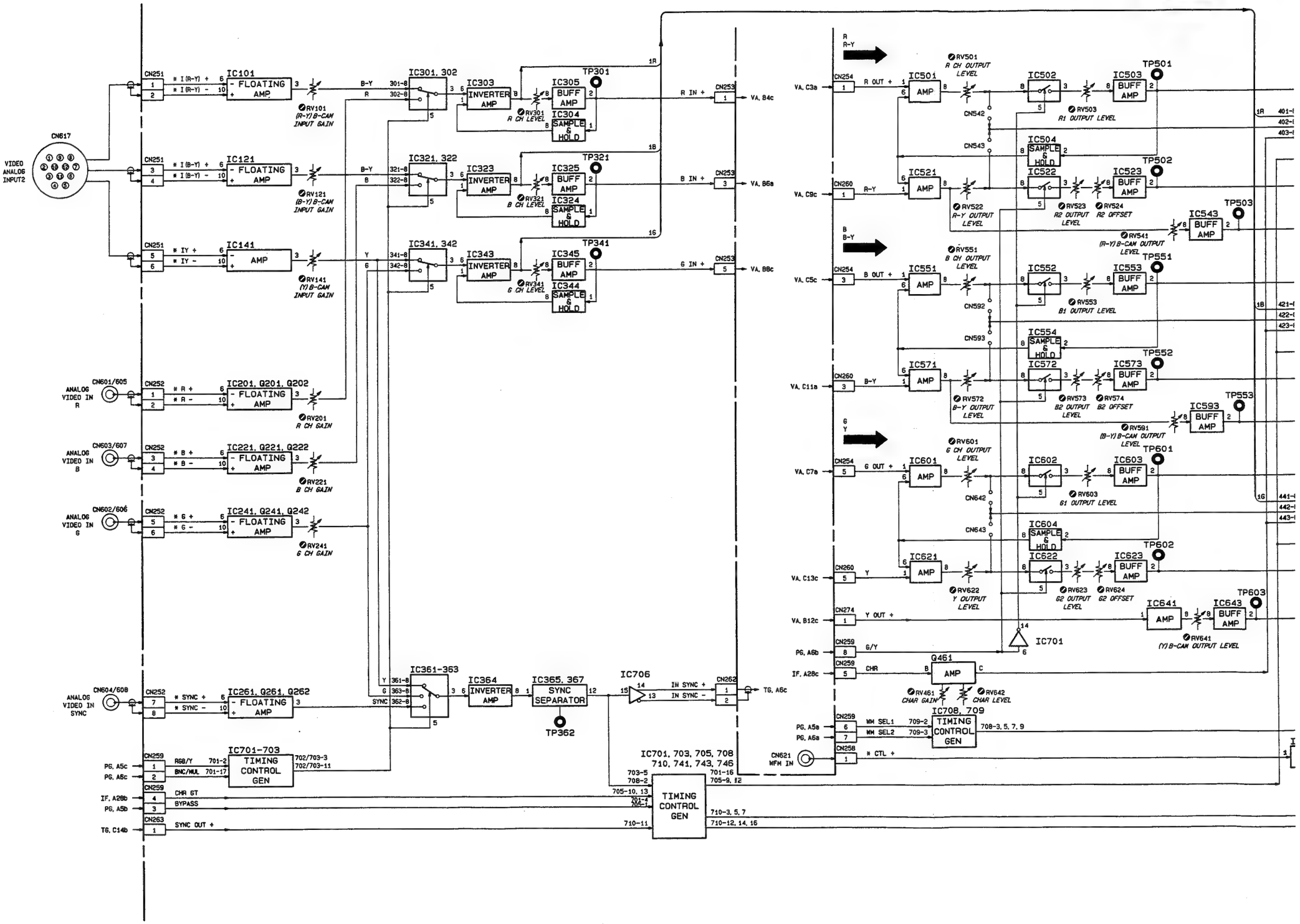

## IV-14 BOARD BLOCK DIAGRAM

BOARD NO.1-620-935-11
DVPC-1000 (J) : #10001-11199
DVPC-1000 (U/C) : #10001-10999
DVPC-1000 (EK) : #10001-11099

## IV-20 BOARD

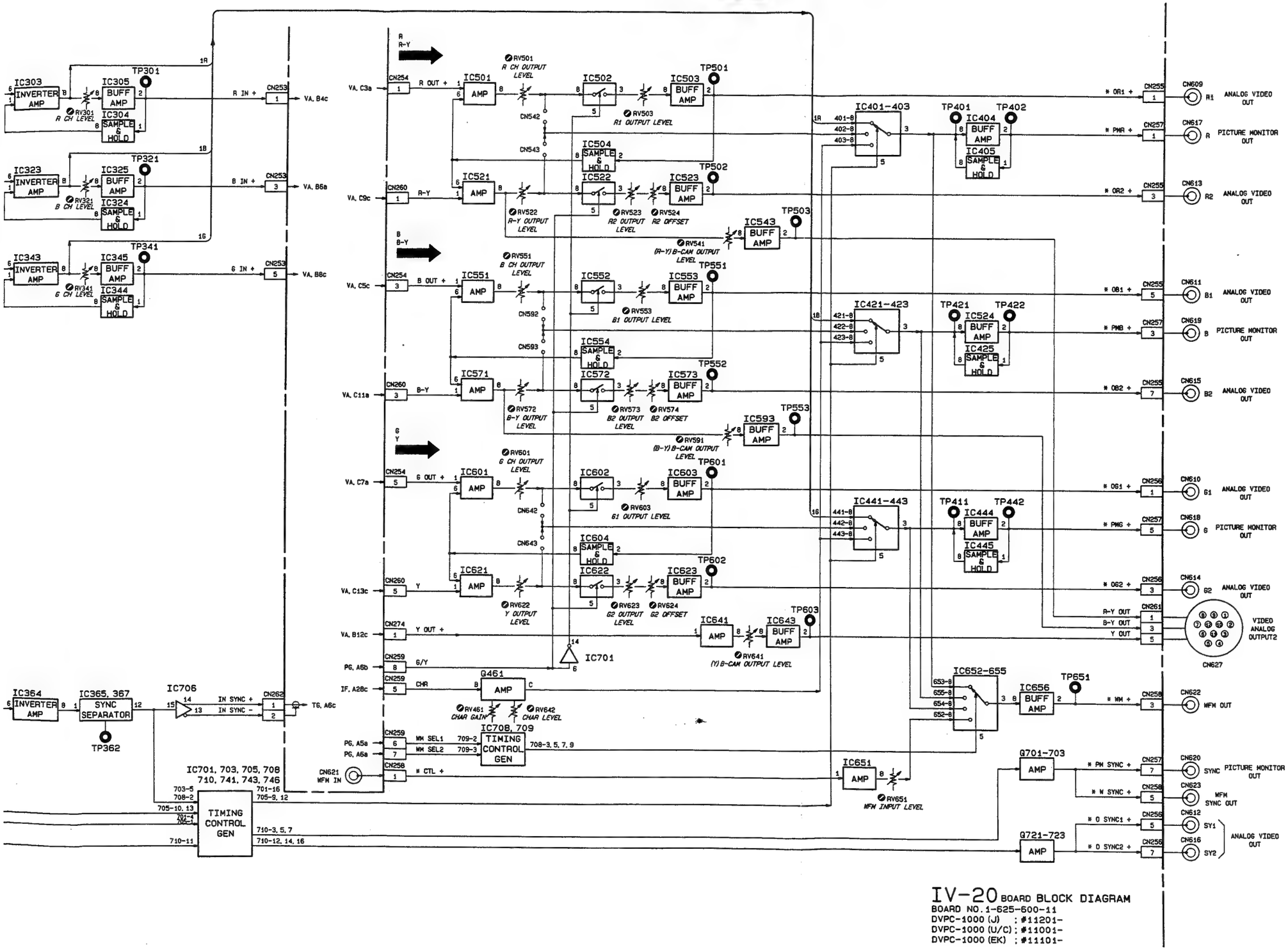
Video I/O

| |
|---|
| # 11201 & UP (J) |
| # 11001 & UP (UC) |
| # 11101 & UP (EK) |




A-63 (a)

A-64 (a)




## IV-20 BOARD BLOCK DIAGRAM

BOARD NO. 1-625-600-11
DVPC-1000 (J) : #11201-
DVPC-1000 (U/C) : #11001-
DVPC-1000 (EK) : #11101-

A-64 (a)

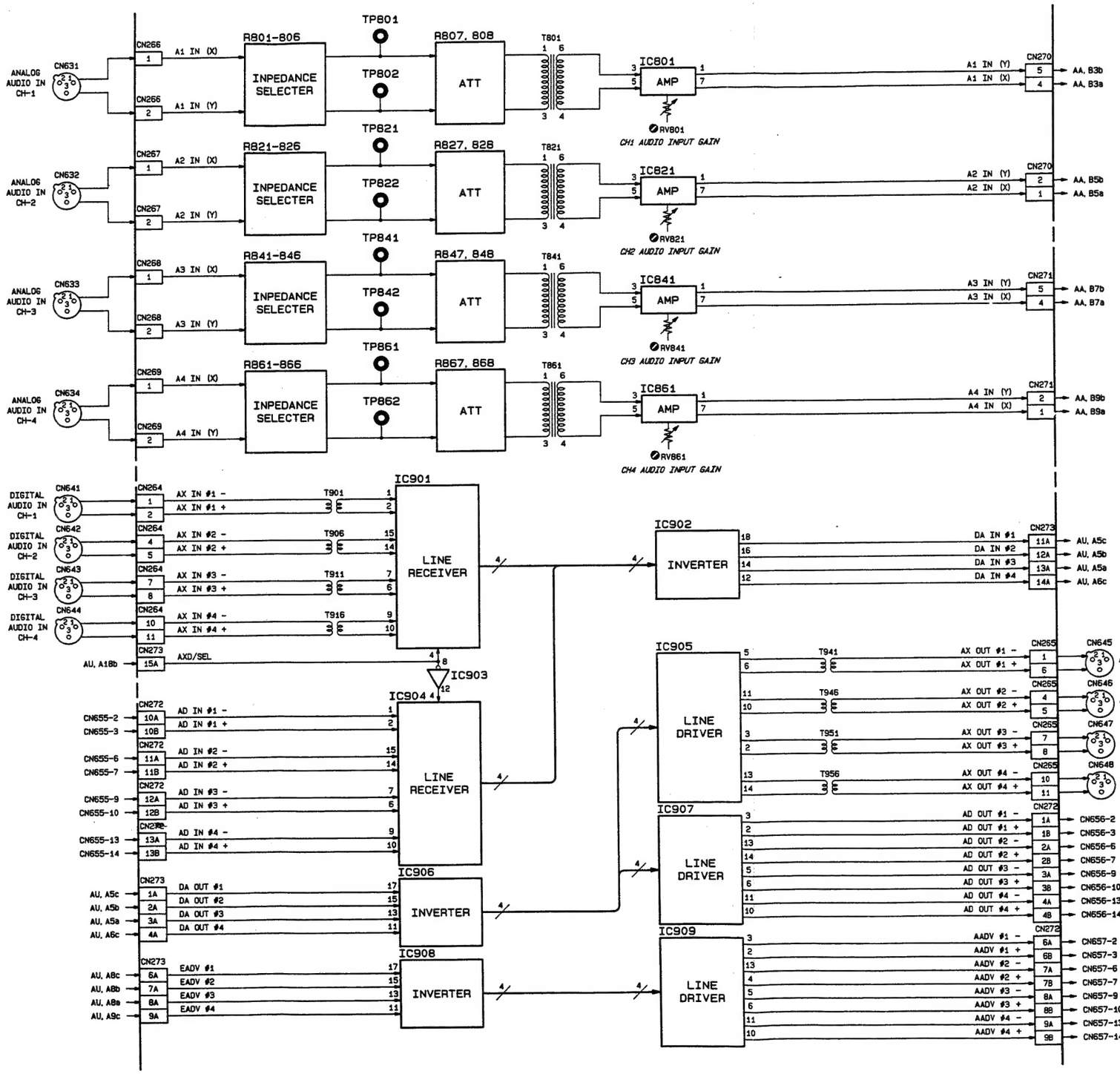
A-65 (a)

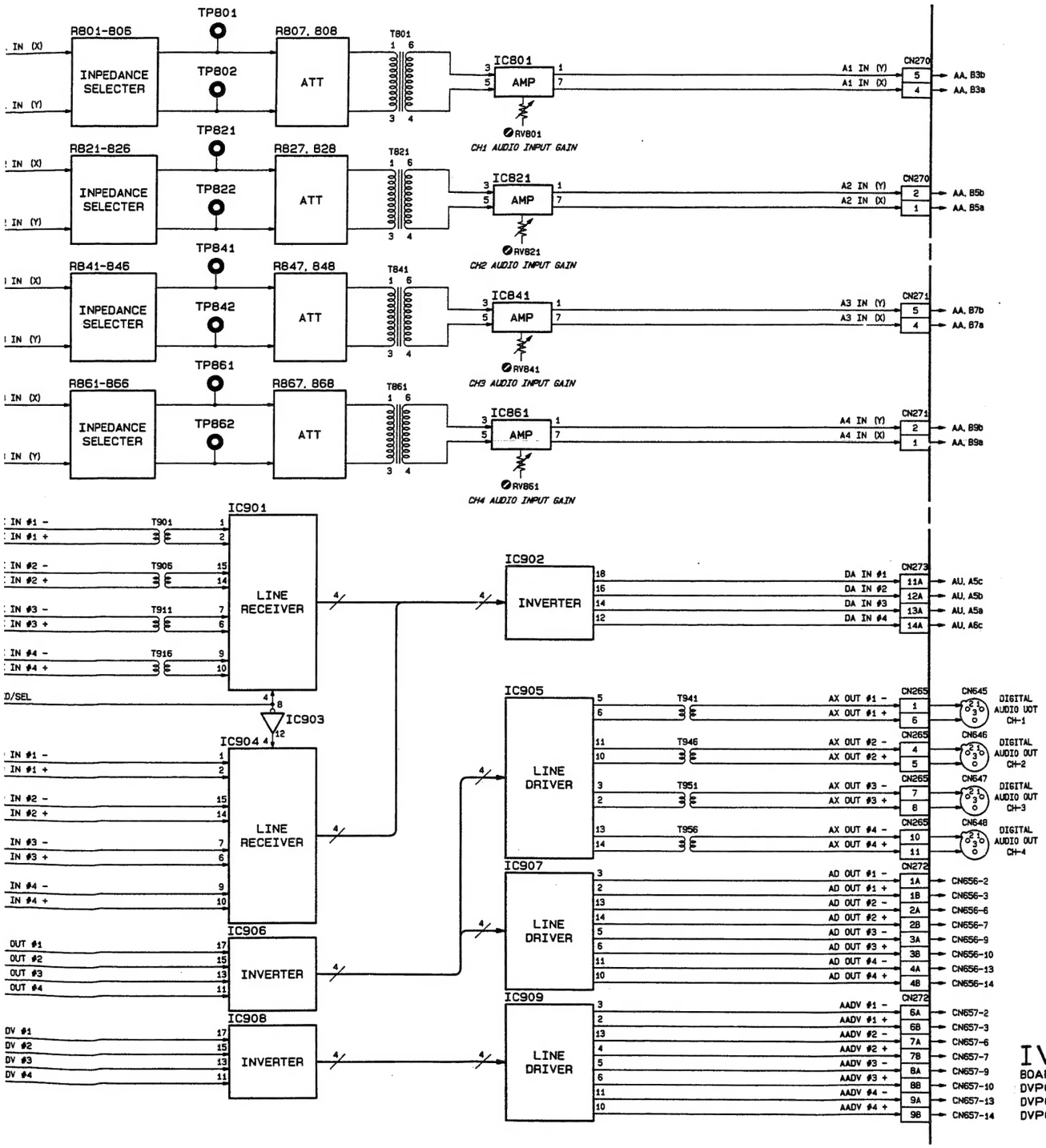
**IV-21** BOARD
Audio I/O

| |
|---|
| #11201 & UP (J) |
| #11001 & UP (UC) |
| #11101 & UP (EK) |

BLOCK DIAGRAM **IV-21**

**IV-21** BLOCK DIAGRAM



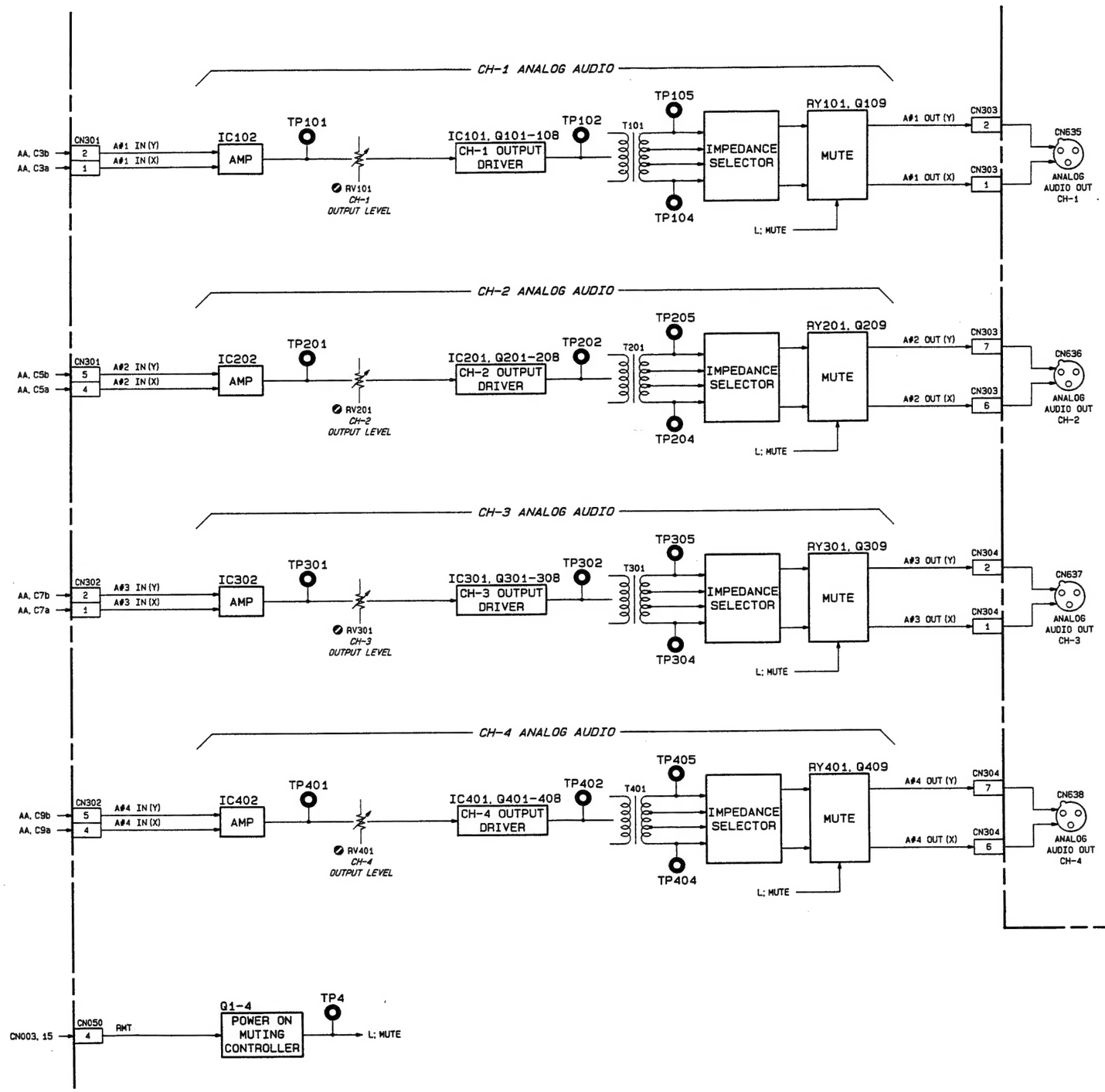


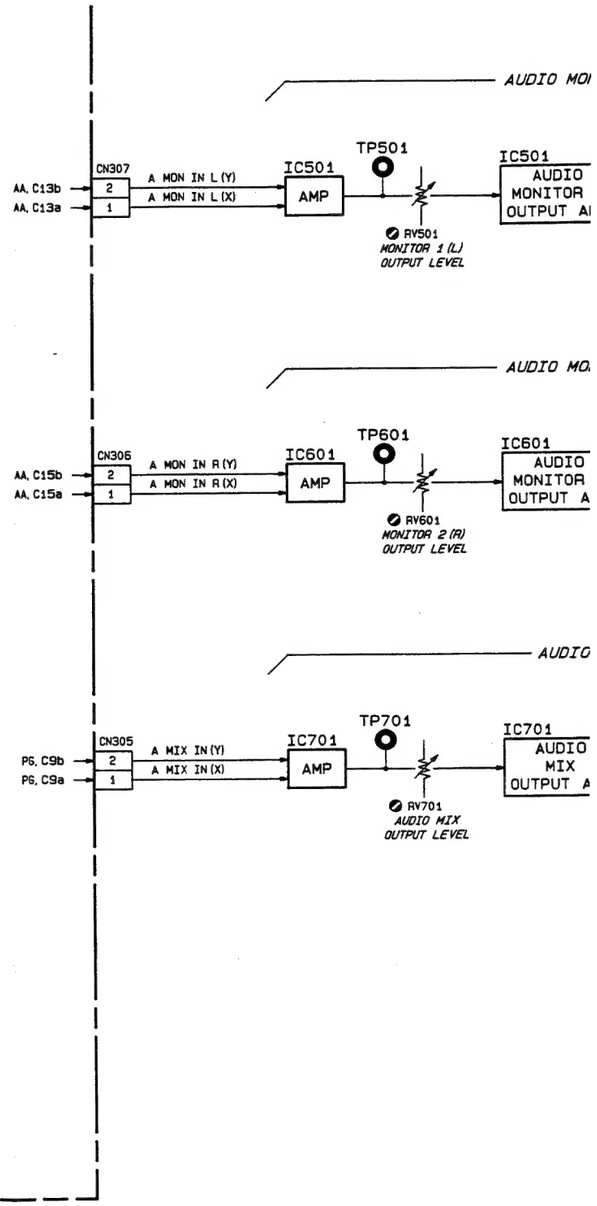

## IV-21 BOARD BLOCK DIAGRAM

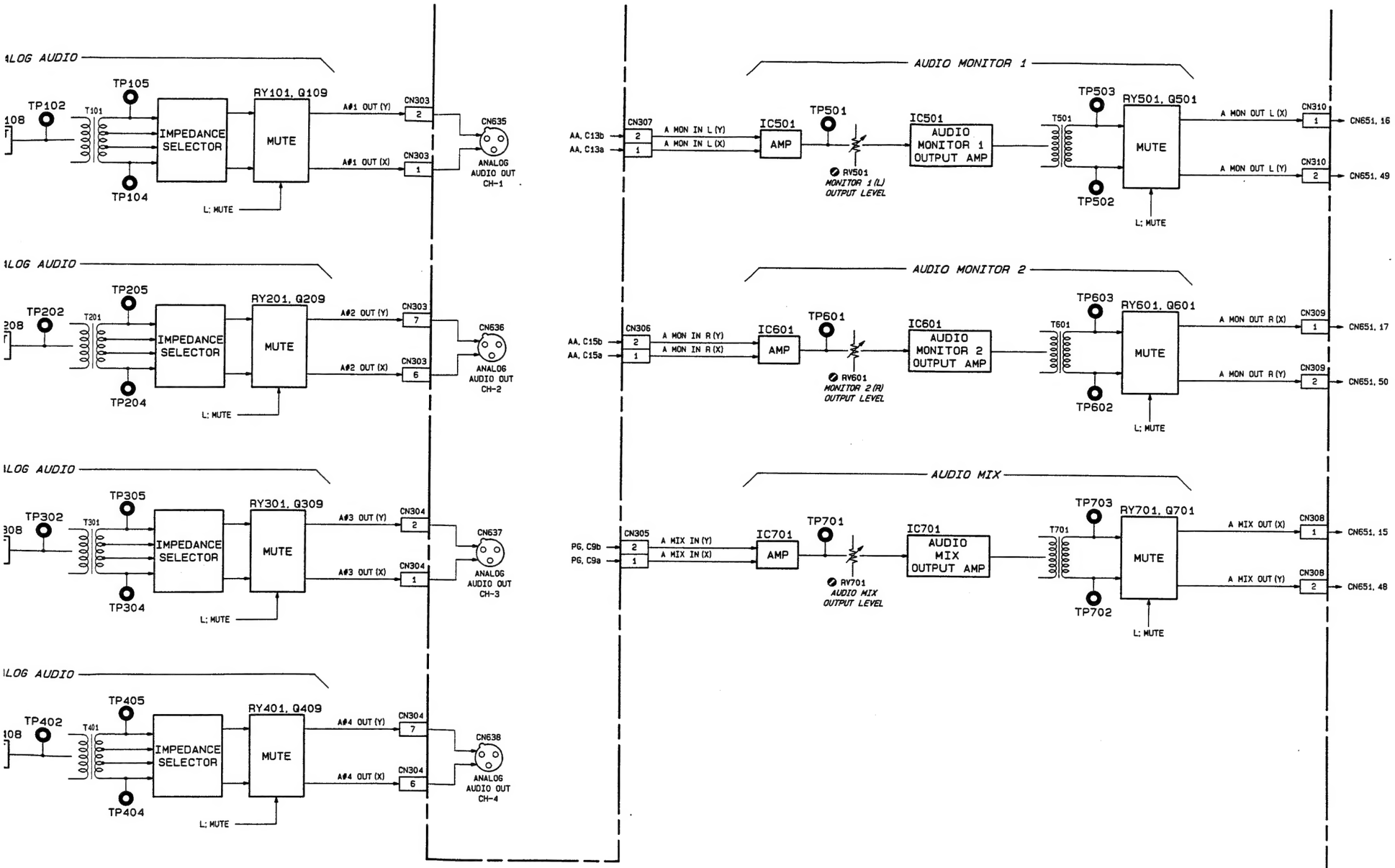
BOARD NO.1-620-601-11
DVPC-1000 (J) : #11201-
DVPC-1000 (UC) : #11001-
DVPC-1000 (EK) : #11101-

## AT-45 BOARD

Audio Line Amplifier






## AT-45 BOARD BLOCK DIAGRAM

BOARD NO. 1-620-937-11, 12
DVPC-1000 (J) : #10001-
DVPC-1000 (U/C) : #10001-
DVPC-1000 (EK) : #10001-